X1830

Smart Video Processor

Programming Manual

Release Date: Jun. 11, 2019

北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

X1830 Smart Video Processor

Programming Manual

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Section 1

OVERVIEW

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1 Overview

X1830 is a smart video application processor targeting for video devices like mobile camera, security survey, video talking, video analysis and so on. This SoC introduces a kind of innovative architecture to fulfill both high performance computing and high quality image and video encoding requirements addressed by mobile multimedia devices. X1830 provides high-speed CPU computing power, excellent image signal process, fluent 2688x2048 resolution video recording.

The CPU (Central Processing Unit) core, equipped with 32kB instruction and 32kB data L1 cache, and 128kB L2 cache, operating at 1.5GHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included. The MXU2.0(SIMD128) instruction set has been implemented by XBurst® engine, and is one part of the CPU.

With the powerful CPU, X1830 supports various computer vision applications, such as face detection, human detection, gesture recognition, and etc. Also people can develop new computer vision application using the MXU2.0 to accelerate it.

The VPU (Video Processing Unit) core is powered with another XBurst® processor engine. Together with the on chip video accelerating engine and post processing unit, X1830 delivers high video performance. The maximum resolution of 1560x1600 in the format of H.264 are supported in encoding. up to 50Mbit/s, 1080P@80fps.

The ISP (Image signal processor) core supports excellent image process with the image coming from raw sensors. It supports DVP MIPI CSI-2 interface. With the functions, such as 3A, 2D and 3D denoise, WDR/HDR, lens shading, it can supply maximum resolution 2688x2048 resolution image for view or encoding to store or transfer.

For more fast and easy to use X1830, one 1024Mbit DDR2 is integrated.

On-chip modules such as audio CODEC, multi-channel SAR-ADC controller and camera interface offer designers a economical suite of peripherals for video application. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. Other peripherals such as USB OTG, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications..

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1.1 Block Diagram

Figure 1-1 X1830 Diagram

1.2 Features

1.2.1 CPU

- XBurst®-1 core
  - XBurst® RISC instruction set
  - XBurst® SIMD128 instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 1.0GHz.
- MMU
  - 32-entry joint-TLB
  - 8 entry instruction TLB
  - 8 entry data TLB
- L1 Cache
  - 32KB instruction cache
  - 32KB data cache
- Hardware debug support
- 16KB tight coupled memory
- L2 Cache

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- 128KB unified cache

1.2.2 VPU

- Support H264 Encoder(I、P slices)
- Support H264 baseline main high profile encoding up to 50M Mbit/s, 1080P@80fps
- Support H264 maximum size up to 1560x1600 resolution
- Only support JZ-bitstream Decoder
- JPEG compressing/decompressing up to 70Mega-pixels per second（baseline）

1.2.3 ISP

- Output support two channel: FR is 2688x2048 @20fps, DS1 is 1080p @60fps
- The Module support Max input resolution 2688x2048 @20fps, 1080p @60fps,720p @120fps
- Input image up to 12bit RAW or Up to 24bit RGB. Both RGB and YCbCr are supported from sensor
- Up to 2 output channel. Image crop and downscaler
- 2-D and 3-D noise reduction filter lead to high levels of noise reduction with minimal effect on edges and textures
- Single frame and multi frame WDR/HDR provide high dynamic range in both still and video capture modes
- Advanced demosaic, color processing, lens shading, defog, glare, static/dynamic defect pixel and other modules provide high image quality
- 3A supported
- Flash timer

1.2.4 Image post processor(IPU)

- DMA mode for data transaction, Input format:
  - Input data format: ARGB,RGB,NV12/NV21
  - Output data format: ARGB,RGB,NV12/NV21,HSV
- Color conversion feature: input and output format can be chosen freely from input and output data format.
- Minimum input image size (pixel): 4x4
- Maximum input image size (pixel): 2592x2048
- Minimum output image size (pixel): 4x4
- Maximum output image size (pixel): 2592x2048
- Background channel OSD function:
  - Support 4 layers OSD
  - Support whole background picture into OSD process and partial picture into OSD process
  - Support 12 port-duff OSD modes

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- Support 5 input format in background channel: ARGB8888, ARGB1555, RGB888, NV12, NV21. RGB can be in following sequence: RGB, RBG, BRG, BGR, GRB, GBR. Specifically, RGB888 format data occupy 4 bytes when stored in memory, RGB occupy three bytes, and the forth byte can be any value.
- Output picture format must be the same with the input picture format of separated background channel.

1.2.5 Display (LCD)

- Layer feature
  - Support 2 layer DMA channel
  - Support input format：RGB8888/888/565/555,NV12/NV21
  - Support frame size 4x4~800x800
  - Support global alpha
- Composition feature
  - Support 2 layer Alpha Blending
  - Support frame size 4x4~800x800
- Display feature
  - Support TFT(RGB666)
  - Support SLCD(MIPI-DBI type A ,type B, type C)
  - Support 640x480@60hz

1.2.6 Video input

- Support 8/10/12 bit RGB Bayer input
- Support maximum：2688x2048 @20fps, 1080p @60fps,720p @120fps
- Support single-sensor input
- Support DVP/BT1120
- Support MIPI CSI2 2-lane

1.2.7 Audio

- Integrated Audio codec.
  - 24 bits DAC with 93dB SNR
  - 24 bits ADC with 92dB SNR
  - Support signal-ended and differential microphone input and line input
  - Automatic Level Control (ALC) for smooth audio recording
  - Pure logic process: no need for mixed signal layers and less mask cost
  - Programmable input and output analog gains
  - Digital interpolation and decimation filter integrated
  - Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K

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1.2.8 Memory Interface

- Integrated 1024Mbits DDR2
- Static memory interface
  - Support 6 external chip selection CS6~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

1.2.9 System Functions

- Clock generation and power management
  - On-chip 12/24/48MHZ oscillator circuit
  - External 32.768KHZ input
  - One four-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - SSI clock supports 50M clock
  - MSC clock supports 100M clock
  - Functional-unit clock gating
  - Shut down power supply for P0, ISP, VPU, IPU, LCD, LDC
- Timer and counter unit with PWM output and/or input edge counter
  - Provide eight separate channels, six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode

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  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
- PCLK, EXTAL and RTCCLK can be used as the clock for counter
- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SoC
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - 3 Channels
  - Resolution: 10-bit
  - Integral nonlinearity: ±1 LSB
  - Differential nonlinearity: ±0.5 LSB
  - Resolution/speed: up to 2MSPS
  - Max Frequency: 24MHz
  - Low power dissipation: 1.5mW(worst)
  - Support multi-touch detect
  - Support write control command by software
  - Single-end and Differential Conversion Mode
  - Support external touch screen controller
  - Pin Description
- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32k clock generation
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter
- OTP Slave Interface
  - Total 1024 bits. Lower 192bits are read only, other higher bits are read-able and write-able

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1.2.10 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 4 interrupts, each interrupt corresponds to the group, to INTC
- SMB Controller
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - 16-level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 3 independent SMB channels (SMB0, SMB1,SMB2)
- One High Speed Synchronous serial interfaces (SFC)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - transmit-only or receive-only operation
  - MSB first for command and data transfer, and LSB first for address transfer
  - 64 entries x 32 bits wide data FIFO
  - one device select
  - Configurable sampling point for reception
  - Configurable timing parameters: tSLCH, tCHSH and tSHSL
  - Configurable flash address wide are supported
  - 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
  - two data transfer mode: slave mode and DMA mode
  - Configurable 6 phases for software flow
- Two Normal Speed Synchronous serial interfaces (SSI0, SSI1)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode

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- Programmable clock phase and polarity for Motorola's SSI format
- Two slave select signal (SSI_CE_ / SSI_CE2_) supporting up to 2 slave devices
- Back-to-back character transmission/reception mode
- Loop back mode for testing

- Two UARTs (UART0, UART1)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification
- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit ,4bit and 8bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands
  - Support Command Completion Signal and interrupt to CPU
  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes
- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect

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- 16 Endpoints:
- Dedicate FIFO
- Supports control, interrupt, ISO and bulk transfer

- Digital True Random Number Generator（DTRNG）
  - Pure digital logic circuits
  - True random number
  - Interrupt mode and no interrupt mode

1.2.11 Bootrom

16kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	28nm CMOS low power
Power supply voltage	General purpose I/O: 1.5~3.6V DDR I/O for DDR2: 1.8V ± 0.1V RTC I/O: 1.5V~3.6V EFUSE programming: 1.5V ± 10% Analog power supply 1: 1.8V ± 10% Analog power supply 2: 3.3V ± 10% Core: 1.3V ± 0.1V
Package	BGA223 11mm x 11mm x 1.22mm, 0.65mm pitch
Operating frequency	1.5GHz

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Section 2

CORE FUNCTIONS

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2 CPU

2.1 Overview

The CPU of this X1830-SOC is a uni-core implementation has following features.

- Powerful SIMD implementation compliance with Ingenic's SIMD128 -ISA
- Enhanced FPU compliance with MIPS32-ISA
- 32KB L1-Icache, 32KB L1-Dcache for each core
- 128 KB unified L2 cache supporting WB and WT attribute with hardware prefetch

2.2 PRID of X1830-CPU

Processor ID register (CP0 Register 15, select 0) in XBurst CPUs is a read-only register being used to identify implementation detail of each SOC's CPU. Please refer to the programming manual of XBurst CPU for detail of the register. For X1830, its value is 0x00D00100.

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3 ISP

3.1 Overview

The ISP (Image Signal Processor) module is a complete camera subsystem which includes a variety of advanced image processing technologies to address the requirements of high-performance camera designs.

The ISP supports parallel input interfaces(DVP)、MIPI CSI-2、BT1120/BT656 and BT601 interface sensors. As shown in Figure 3-1，the red lines represent control flow，and the blue lines represent data flow.

Figure 3-1 ISP Typical Application

3.2 Features

3.2.1 System level

- Sensor Interface: DVP、MIPI CSI-2、BT1120/BT656 (8bit)、BT601(8bit)
- 32-bit AHB slave interface
- 64-bit AXI mater interface
- Total 28 interrupts

3.2.2 ISP features

- Max input resolution 2688x2048@20fps,1920x1080@60fps,1280x720@120fps.
- Input image up to 12bit RAW or Up to 24bit RGB. Both RGB and YCbCr are supported from sensor.
- Up to 2 output channel.

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- 2-D and 3-D noise reduction filter lead to high levels of noise reduction with minimal effect on edges and textures.
- Single frame and multi frame WDR/ HDR provide high dynamic range in both still and video capture modes.
- Advanced demosaic, color processing, lens shading, defog, glare, static/dynamic defect pixel and other modules provide high image quality.
- 3A supported.
- Flash timer

3.2.3 Image Format

- Input image up to 12bit RAW or up to 24bit RGB. Both RGB and YCbCr are supported from SoC sensors.
- Camera input interface supports.
  1) DVP: RAW8,RAW10,RAW12,YUV422(8bit IO)
  2) MIPI CSI-2: RAW8,RAW10,RAW12,RGB555,RGB565,RGB666,RGB888,YUV422
  3) LVDS：RAW8、RAW10、RAW12
- BT1120/BT656 (8 bit IO): YUV422
- BT601(8 bit IO): YUV422
- ISP output format(to DRAM)
  1) NV21, NV12, YUV422
  2) RGB555,RGB565,RGB888
  3) RAW8,RAW10,RAW12

3.2.4 Output Interface

- DMAOUT to DDR
- Output to NCU or MSCALER
  1) support eighter FR channel or DS1 channel output to NCU，the other channel to DMAOUT
  2) ISP will assert int when there is axi address or wlen errors occur which channel output to NCU or MSCALER.
  3) support software recovery and hardware recovery mode.
  4) software should reset NCU or MSCALER when errors occur at software recovery mode.
  5) NCU and MSCALER will recovery by hardware autoly at hardware recovery mode. ISP doesn't need recovery or reset，but it will loss 1 or 2 frames.

3.2.5 Performance

- Max input resolution 2688x2048.

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3.3 Block Diagram

Figure 3-2 ISP Diagram

VIC is video input controller. ISP pipeline is image processing pipeline, IRQ process the interrupts of VIC and ISP pipeline. At last, ISP output two channels include FR(full resolution) channel and DS1(downscaler) channel. the order of configuration is IRQ, ISP pipeline, VIC.

3.4 Function Details

Max pixel clock frequence is 150Mhz, assuming 20% overhead for video blanking times, max throughput up to 120MP/sec. Minimal AXI bus clock frequence is 2x pixel clock.

Input image can be up to RAW12, up toRGB888 or YUV 422.

Support function shows in Table 3-1. The functions can be bypass.

Table 3-1 ISP Function Details

Support functions	Defect pixel: static and dynamic RAW test pattern generator Green channel equalization Black level compensation HDR sensor decompanding E/W image flip (mirror) support intra-frame noise reduction and radial NR control for all supported resolutions Inter-frame (3D) noise reduction Gain and offset control (for white balance) Frame stitching WDR support (stitching block and AXI interface) Note, the stitching module does not include motion compensation. Thus, any movement (e.g. for a wearable product) will cause FS-WDR images to be smeared and likely unacceptable image quality. Lens shading (vignetting) correction: radial model and mesh-based

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	Dynamic range compression and local tone mapping Demosaic: moiré reduction and false color reduction Linear matrix color correction Anti-fog / anti-glare compensation block 3A statistics generator: 15x15 zones APB interface for ISP configuration LED flash timer block ISP interrupt event module 16 event outputs <u>ISP output 1:</u> - Full sensor resolution, - Max output resolution 2688x2048(frame rate locked to sensor frame rate) - Dither, crop and color-space convert support - Gamma correction - Logo - Output sharpening <u>ISP output 2:</u> - Down scaling modes from sensor input resolution to progressive output modes - Max output resolution 1920 x 1080 (frame rate locked to sensor frame rate) - Downscaler programmable, down to 1/16 of ISP input resolution - **Note**: Downscaling beyond 1/3 of the input resolution may produce visible aliasing artifacts. **- Note: when the ISP is in bypass mode, the downscaler can be used with an RGB input only! But can configure for RAW input!** - Dither, crop and color-space convert support - Gamma correction - Output sharpening

3.5 Pins Description

ISP pin list is shown as Table 3-2.

Table 3-2 Pin List

Pin	Location	Width	I/O	Description
Flash_in	PC08Function1	1	I	Flash strobe in
Flash_out	PC09Function1	1	O	Flash out
dvp_pclk_i	PA14Function1	1	I	Dvp pixel clock
dvp_mclk_o	PA15Function1	1	O	reference clock for sensor
dvp_hsync_i	PA16Function1	1	I	Dvp horizon sync
dvp_vsync_i	PA17Function1	1	I	Dvp vertical sync
dvp_d0_i	PA00Function1	1	I	Dvp pixel data bit0

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dvp_d1_i	PA01Function1	1	I	Dvp pixel data bit1
dvp_d2_i	PA02Function1	1	I	Dvp pixel data bit2
dvp_d3_i	PA03Function1	1	I	Dvp pixel data bit3
dvp_d4_i	PA04Function1	1	I	Dvp pixel data bit4
dvp_d5_i	PA05Function1	1	I	Dvp pixel data bit5
dvp_d6_i	PA06Function1	1	I	Dvp pixel data bit6
dvp_d7_i	PA07Function1	1	I	Dvp pixel data bit7
dvp_d8_i	PA08Function1	1	I	Dvp pixel data bit8
dvp_d9_i	PA09Function1	1	I	Dvp pixel data bit9
dvp_d10_i	PA10Function1	1	I	Dvp pixel data bit10
dvp_d11_i	PA11Function1	1	I	Dvp pixel data bit11

3.6 Interrupts

The ISP_core provides up to 16 events (interrupt_request[n]) that can be used to synchronize the firmware control of the ISP.

Each of the 16 events can be selected from any one of ~64 (note, not all locations are populated) using the 6-bit Index. (See Table 1 Interrupt event index schema below.)

Each event (to be handled by the customers interrupt controller) is a single pulse, synchronous with PCLK.

Each of the 16 output events are also mapped to a Status register (Interrupt_status[15:0]), within the configuration register space. The Status bits are “sticky”, i.e. they will be SET by the event pulse, and remain high until cleared.

There is also a matching Clear register (Interrupt_clear[15:0]), within the configuration register space, which when written allows each of the Status bits to be individually RESET.

Table 3-3 Interrupt event index schema

Select Index	Source module	Type
16	Input formatter	Frame_end
24		Frame_start
17	Defect pixel	Frame_end
25		Frame_start
18	Sinter	Frame_end
26		Frame_start
19	Temper	Frame_end
27		Frame_start
20	Iridix	Frame_end

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28		Frame_start
21	Demosaic	Frame_end
29		Frame_start
22	Sharpen on primary output	Frame_end
30		Frame_start
23	Primary video output formatter	Frame_end
31		Frame_start
48	Downscaler 1	Frame_end
56		Frame_start
49	Sharpen on DS1 output	Frame_end
57		Frame_start
50	DS1 video output formatter	Frame_end
58		Frame_start
51	Downscaler 2	Frame_end
59		Frame_start
52	Sharpen on DS2 output	Frame_end
60		Frame_start
53	DS2 video output formatter	Frame_end
61		Frame_start
8	Auto-exposure	Event
9	Auto white balance	Event
10	Auto-focus	Event
11	Auto-exposure histogram	Event
12	Motion vector estimator	Event
13	Temper frame buffer	Event
14	Full res DMA writer frame written	Event
15	DS1 DMA writer frame written	Event
1	DS2 DMA writer frame written	Event
6	Timer module strobe 6	Event
7	Timer module strobe 7	Event

Event Definitions

frame_end: indicates that the source module has entered vertical blanking, i.e. completed processing active video data.

frame_start: indicates that the source module has commenced outputting valid video data

event: 3A statistics blocks: valid statistics are ready to be read.

DMA writers: The last write transaction has now been posted.

Timer modules: These are triggered by programmable timers (see below)

Timer module

The LED flash timer contains multiple channels of highly configurable timers. Two timer channels are routed into/from the interrupt module to provide programmable interrupt events.

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Details of the LED flash timer can be found in the ISP_Guide.pdf.

3.7 Interface Timing

3.7.1 dvp

The DVP interface is a parallel video port which input video data from the sensor in raster-scan order, left-to-right, top-to-bottom, one pixel at a time, at the pixel clock rate.

In the ISP, DVP input interface supports 4 timing modes which are listed as following figures. The vsync and hsync polarity can be configured in VIC.

a）pulse sync

b）line valid

Figure 3-3 DVP mode0

As Figure 3-3 a) b) described, the mode0 is called pulse sync or line valid mode. For pulse sync, one vsync pulse indicate the frame start, and after the vsync pulse, the data is valid if hsync valid. For line valid, one vsync pulse indicate the frame start, and when the vsync pulse and hsync are valid, the data is valid.

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Figure 3-4 DVP mode1

As Figure 3-4 described, the mode1 is called vsync mode which one vsync pulse indicate the frame start. For the vsync and hsync there are a front porch and a back porch and the data is invalid when vsync and hsync is front and back porch.

3.7.2 mipi csi-2

When the VIC is working with MIPI CSI-IDI interface, there are four interface timing protocols. The following figures describe the detail content.

When the MIPI PHY slaver receiving data from 1 lane, the IDI interface protocol is described as Figure 3-5.

Figure 3-5 input data timing when 1lane phy

When the MIPI PHY slaver receiving data from 2 lane, the IDI interface protocol is described as Figure 3-6.

Figure 3-6 input data timing when 2lane phy

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3.8 Data Format

3.8.1 Input data

3.8.1.1 DVP input data

The width of input data from dvp interface can be 8bit or 16bit, and the data is uncompressed.

a) RAW

The RAW data sequence follows the generic dvp rule. It is described in Table 3-4

Table 3-4 RAW Data sequence

Sequence mode	First clock	Second clock	Third clock	Fourth clock
dvp_msb=0	dvp_data [n-1:0]	dvp_data [n-1:0]	dvp_data [n-1:0]	dvp_data [n-1:0]
dvp_msb=1	dvp_data [15:15-n+1]	dvp_data [15:15-n+1]	dvp_data [15:15-n+1]	dvp_data [15:15-n+1]

b) YUV422 8-bit

The YUV422 8-bit data sequence follows the generic dvp rule. It is described in Table 3-5.

Table 3-5 YUV422 8-bit Data sequence

Sequence mode	First clock	Second clock	Third clock	Fourth clock
YUV_data_order=0	V1[7:0]	Y1[7:0]	U2[7:0]	Y2[7:0]
YUV_data_order=1	U1[7:0]	Y1[7:0]	V2[7:0]	Y2[7:0]
YUV_data_order=2	Y1[7:0]	V1[7:0]	Y2[7:0]	U2[7:0]
YUV_data_order=3	Y1[7:0]	U1[7:0]	Y2[7:0]	V2[7:0]

Note: if input is YCbCr, U is replaced by Cb, V is repalced by Cr.

For the YCbCr 4:2:2 bypass mode above, the input sequence to the ISP shall be:

Table 3-6 YUV422 internal sequence

Pixel	DATA_IN[23:12]	DATA_IN[11:0]
0	Y0[7:0], Cb0[7:4]	Cb0[3:0], 8’b0
1	Y1[7:0], Cr0[7:4]	Cr0[3:0], 8’b0
2	Y2[7:0], Cb2[7:4]	Cb2[3:0], 8’b0
3	Y3[7:0], Cr2[7:4]	Cr2[3:0], 8’b0
4	Y4[7:0], Cb4[7:4]	Cb4[3:0], 8’b0
5	Y5[7:0], Cr4[7:4]	Cr4[3:0], 8’b0

c) RGB565

The rgb565 data sequence follows the generic dvp rule. It is described in Table 3-7.

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Table 3-7 RGB565 Data sequence

Sequence mode	First clock	Second clock	Third clock	Fourth clock
Dvp_rgb_order=0	{B1[4:0],G1[5:3]}	{G1[2:0],R1[4:0]}	{B2[4:0],G2[5:3]}	{G2[2:0],R2[4:0]}
Dvp_rgb_order=1	{R1[4:0],G1[5:3]}	{G1[2:0],B1[4:0]}	{R2[4:0],G2[5:3]}	{G2[2:0],B2[4:0]}
Dvp_rgb_order=2	{G1[5:0],R1[4:3]}	{R1[2:0],B1[4:0]}	{G2[5:0],R2[4:3]}	{R2[2:0],B2[4:0]}
Dvp_rgb_order=3	{B1[4:0],R1[4:2]}	{R1[1:0],G1[5:0]}	{B2[4:0],R2[4:2]}	{R2[1:0],G2[5:0]}
Dvp_rgb_order=4	{G1[5:0],B1[4:3]}	{B1[2:0],R1[4:0]}	{G2[5:0],B2[4:3]}	{B2[2:0],R2[4:0]}
Dvp_rgb_order=5	{R1[4:0],B1[4:2]}	{B1[1:0],G1[5:0]}	{R2[4:0],B2[4:2]}	{B2[1:0],G2[5:0]}

d) RGB555

The rgb555 data sequence follows the generic dvp rule. It is described in Table 3-8.

Table 3-8 RGB555 Data sequence

Sequence mode	First clock	Second clock	Third clock	Fourth clock
Dvp_rgb_order=0	{B1[4:0],G1[4:2]}	{G1[1:0],1'b0,R1[4:0]}	{B2[4:0],G2[4:2]}	{G2[1:0],1'b0,R2[4:0]}
Dvp_rgb_order=1	{R1[4:0],G1[4:2]}	{G1[1:0],1'b0,B1[4:0]}	{R2[4:0],G2[4:2]}	{G2[1:0],1'b0,B2[4:0]}
Dvp_rgb_order=2	{G1[4:0],1'b0,R1[4:3]}	{R1[2:0],B1[4:0]}	{G2[4:0],1'b0,R2[4:3]}	{R2[2:0],B2[4:0]}
Dvp_rgb_order=3	{B1[4:0],R1[4:2]}	{R1[1:0],G1[4:0],1'b0}	{B2[4:0],R2[4:2]}	{R2[1:0],G2[4:0],1'b0}
Dvp_rgb_order=4	{G1[4:0],1'b0,B1[4:3]}	{B1[2:0],R1[4:0]}	{G2[4:0],1'b0,B2[4:3]}	{B2[2:0],R2[4:0]}
Dvp_rgb_order=5	{R1[4:0],B1[4:2]}	{B1[1:0],G1[4:0],1'b0}	{R2[4:0],B2[4:2]}	{B2[1:0],G2[4:0],1'b0}

3.8.1.2 MIPI CSI Input data

When vic is working with mipi_csi, the input data format of vic is described as following Tables.

a) RAW8

The RAW8 data format follows the generic CSI-2 rule. It is described in Table 3-9.

Table 3-9 RAW8 Data Format Reception

MSB																															**LSB**
P4								P3								P2								P1							
d7	d6	d5	d4	d3	d2	d1	d0	c7	c6	c5	c4	c3	c2	c1	c0	b7	b6	b5	b4	b3	b2	b1	b0	a7	a6	a5	a4	a3	a2	a1	a0

b) RAW10

The RAW10 data format follows the generic CSI-2 rule. It is described in Table 3-10.

Table 3-10 RAW10 Data Format Reception

MSB																															**LSB**
P4[9:2]								P3[9:2]								P2[9:2]								P1[9:2]							
c8	c7	c6	c6	c5	c4	c3	c2	c9	c8	c7	c6	c5	c4	c3	c2	b9	b8	b7	b6	b5	b4	b3	b2	a9	a8	a7	a6	a5	a4	a3	a2
P7[9:2]								P6[9:2]								P5[9:2]								P4[1:0]		P3[1:0]		P2[1:0]		P1[1:0]	
g9	g8	g7	g6	g5	g4	g3	g2	f9	f8	f7	f6	f5	f4	f3	f2	e9	e8	e7	e6	e5	e4	e3	e2	d1	d0	c1	c0	b1	b0	a1	a0

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c) RAW12

The RAW12 data format follows the generic CSI-2 rule. It is described in Table 3-11.

Table 3-11 RAW12 Data Format Reception

MSB																																**LSB**
P3[11:4]								P2[3:0]				P1[3:0]				P2[11:4]								P1[11:4]							
c11	c10	c9	c8	c7	c6	c5	c4	b3	b2	b1	b0	a3	a2	a1	a0	b11	b10	b9	b8	b7	b6	b5	b4	a11	a10	a9	a8	a7	a6	a5	a4
P6[11:4]								P5[11:4]								P4[3:0]				P3[3:0]				P4[11:4]							
f11	f10	f9	f8	f7	f6	f5	f4	e11	e10	e9	e8	e7	e6	e5	e4	d3	d2	d1	d0	c3	c2	c1	c0	d11	d10	d9	d8	d7	d6	d5	d4

d) RGB888

The RGB888 data format follows the generic CSI-2 rule. It is described in Table 3-12.

Table 3-12 RGB888 Data Format Reception

MSB																																**LSB**
B2[7:0]								R1[7:0]								G1[7:0]								B1[7:0]							
d7	d6	d5	d4	d3	d2	d1	d0	c7	c6	c5	c4	c3	c2	c1	c0	b7	b6	b5	b4	b3	b2	b1	b0	a7	a6	a5	a4	a3	a2	a1	a0
G3[7:0]								B3[7:0]								R2[7:0]								G2[7:0]							
f11	f10	f9	f8	f7	f6	f5	f4	g7	g6	g5	g4	g3	g2	g1	g0	f7	f6	f5	f4	f3	f2	f1	f0	e7	e6	e5	e4	e3	e2	e1	e0

e) RGB565

The RGB565 data format follows the generic CSI-2 rule. It is described in Table 3-13.

Table 3-13 RGB565 Data Format Reception

MSB																																**LSB**
R2[4:0]					G2[5:0]						B2[4:0]					R1[4:0]					G1[5:0]						B1[4:0]				
f4	f3	f2	f1	f0	e5	e4	e3	e2	e1	e0	d4	d3	d2	d1	d0	c4	c3	c2	c1	c0	b5	b4	b3	b2	b1	b0	a4	a3	a2	a1	a0

f) RGB555

The RGB555 data format follows the generic CSI-2 rule. It is described in Table 3-14.

Table 3-14 RGB555 Data Format Reception

MSB																																**LSB**
R2[4:0]					G2[4:0]						B2[4:0]					R1[4:0]					G1[4:0]						B1[4:0]				
f4	f3	f2	f1	f0	e4	e3	e2	e1	e0	0	d4	d3	d2	d1	d0	c4	c3	c2	c1	c0	b4	b3	b2	b1	b0	0	a4	a3	a2	a1	a0

g) YUV422 8-bit

The YUV422 8bit data format follows the generic CSI-2 rule. It is described in Table 3-15.

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Table 3-15 YUV422 8bit Data Format Reception

MSB																															LSB
U1								Y1								V1								Y2							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0	c7	c6	c5	c4	c3	c2	c1	c0	d7	d6	d5	d4	d3	d2	d1	d0

3.8.2 Internal data

Table 3-16 Internal data sequence

Format	data_in[23:12]	data_in[11:0]
RAW6	12'b0	RAW[5:0],6'b0
RAW7	12'b0	RAW[6:0],5'b0
RAW8	12'b0	RAW[7:0],4'b0
RAW10	12'b0	RAW[9:0],2'b0
RAW12	12'b0	RAW[11:0]
RGB888	R[7:0],G[7:4]	G[3:0],B[7:0]
RGB666	R[5:0],2'b0,G[5:2]	G[1:0],2'b0,B[5:0],2'b0
RGB565	R[4:0],3'b0,G[5:2]	G[1:0],2'b0,B[4:0],3'b0
RGB555	R[4:0],3'b0,G[4:1]	G[0],3'b0,B[4:0],3'b0

For the YCbCr 4:2:2,the internal data sequence is as below.

Table 3-17 YUV422 internal sequence

Pixel	data_in[23:12]	data_in[11:0]
0	Y0[7:0], Cb0[7:4]	Cb0[3:0], 8’b0
1	Y1[7:0], Cr0[7:4]	Cr0[3:0], 8’b0
2	Y2[7:0], Cb2[7:4]	Cb2[3:0], 8’b0
3	Y3[7:0], Cr2[7:4]	Cr2[3:0], 8’b0
4	Y4[7:0], Cb4[7:4]	Cb4[3:0], 8’b0
5	Y5[7:0], Cr4[7:4]	Cr4[3:0], 8’b0

3.8.3 Output data

ISP output up to 2 individually channels image data to system DDR SRAM. There are multiple options of packing video data depending on the selected output format. Output format and data packing options are selected using the base mode & plane select parameters(configured in each DMA writer control register), A table of available formats are shown below.

Note:

FR DMA:0xB00;

FRUV DMA:0xB80;

DS1 DMA:0xC00;

DS1 UV DMA:0xC80;

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TEMPER DMA: 0xA00

WDR DMA:0xA40

Table 3-18 DMA Output Formats and Packing

Base	plane select	Colour Format	Packing Bit Number																															
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	DMA disabled																																
1	0	RGB32(also used for RGB666)	0	0	0	0	0	0	0	0	Red (7:0)								Green(7:0)								Blue(7:0)							
2	0	A2R10G10B10	0	0	Red (9:0)										Green(9:0)										Blue(9:0)									
3	0	RGB 565	Red (4:0)						Green(5:0)					Blue(4:0)					Red (4:0)					Green(5:0)						Blue(4:0)			
5	0	GEN32	Generic Data(31:0)																															
6	0	RAW16	RAW1(11:0)											0	0	0	0	RAW0(11:0)													0	0	0	0
7	0	RAW12	RAW2(7:0)								RAW1(11:0)												RAW0(11:0)											
			RAW5(3:0				RAW4(11:0)												RAW3(11:0)															RAW2(11:8
			RAW7(11:0)												RAW6(11:0)												RAW5(11:4)							
8	0	AYUV, 8 bit	0	0	0	0	0	0	0	0	Y(7:0)								U(7:0)								V(7:0)							
10	0	YUY2, 8 bit	V0(7:0)								Y1(7:0)								U0(7:0)								Y0(7:0)							
11	0	UYVY, 8 bit	Y1(7:0)								V0(7:0)								Y0(7:0)								U0(7:0)							
13	0	NV12/21 Y	Y3(7:0)								Y2(7:0)								Y1(7:0)								Y0(7:0)							
	1	NV12 U/V	V1(7:0)								U1(7:0)								V0(7:0)								U0(7:0)							
	2	NV21 U/V	U1(7:0)								V0(7:0)								U0(7:0)								V0(7:0)							
Notes		In Base mode 1, to support RGB666 the bottom 2 bits of each colour can be masked in 'Colour space conv ' block. Base mode 5 is for Temper Frame buffer only. In Base mode 6 & 7 to support 10&8 bit RAW the LSB's of ISP input need to be set to zero.																																

DMA Output Formats and Packi

3.9 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

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RCW - read and write, but clear to 0 by read
RSW - read and write, but set to 1 by read
RWC - read and write, clear to 0 by write 1, write 0 has no effect
RWS - read and write, set to 1 by write 1, write 0 has no effect
RC - read only, and clear to 0 by read
RS - read only, and set to 1 by read
SPEC - special access method, relate to its description

3. Reset Value
1 - reset to 1
0 - reset to 0
? - value unknown after reset

3.9.1 Register Memory Map

The ISP registers can be divided to 4 groups, such as registers of VIC, registers of ISP Pipeline and registers of IRQ. These register groups' base addresses be listed as Table 3-19.

Table 3-19 Registers Memory Map Base Address

Name	Base	Description
VIC_BA	0x13300000	Address base of VIC
DMA_BA	0x13310000	Address base of DMA
LFB_BA	0x13300200	Address base of LFB
IRQ_BA	0x13320000	Address base of IRQ
ISP Pipeline_BA	0x13380000	Address base of ISP Pipeline

3.9.2 VIC Registers

Table 3-20 VIC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
VIC_CTRL	RW	0x0000_0000	0x000	32
VIC_RES	RW	0x0000_0000	0x004	32
VIC_FRM_ECC	RW	0x0000_0000	0x008	32
VIC_IN_INTF	RW	0x0000_0000	0x00C	32
VIC_IN_DVP	RW	0x0000_0000	0x010	32
VIC_IN_CSI_LVDS_FMT	RW	0x0000_0000	0x014	32
VIC_IN_HOR_PARA0	RW	0x0000_0000	0x020	32
VIC_IN_HOR_PARA1	RW	0x0000_0000	0x024	32
VIC_IN_VER_PARA0	RW	0x0000_0000	0x030	32
VIC_IN_VER_PARA1	RW	0x0000_0000	0x034	32
VIC_IN_VER_PARA2	RW	0x0000_0000	0x038	32
VIC_IN_VER_PARA3	RW	0x0000_0000	0x03C	32
VIC_OUT_CFG	RW	0x0000_0000	0x050	32

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VIC_OUT_ABVAL	RW	0x0000_0000	0x054	32
VIC_OUT_HBLK	RW	0x0000_0000	0x058	32
VIC_OUT_VBLK	RW	0x0000_0000	0x05C	32
VIC_VLD_LINE_SAV	RW	0x0080_0800	0x060	32
VIC_VLD_LINE_EAV	RW	0x009D_09D0	0x064	32
VIC_INVLD_LINE_SAV	RW	0x00AB_0AB0	0x068	32
VIC_INVLD_LINE_EAV	RW	0x00B6_0B60	0x06C	32
VIC_VLD_FRM_SAV	RW	0x0000_6002	0x070	32
VIC_VLD_FRM_EAV	RW	0x0000_7003	0x074	32
VIC_WORK_STA	R	0x0000_0000	0x090	32
VIC_PIXEL_CNT	R	0x0000-0000	0x094	32
VIC_ROW_CNT	R	0x0000_0000	0x098	32
VIC_OFIFO_CNT	R	0x0000_0000	0x09C	32
VIC_FRT_CB_CTRL	RW	0x0000_0000	0x0A0	32
VIC_FRT_CB_BLK	RW	0x0000_0000	0x0A4	32
VIC_BK_CB_CTRL	RW	0x0000_0000	0x0B0	32
VIC_BK_CB_BLK	RW	0x0000_0000	0x0B4	32
VIC_CB_1ST	RW	0x00EB_8080	0x0C0	32
VIC_CB_2ND	RW	0x0010_8080	0x0C4	32
VIC_CB_3RD	RW	0x0029_F06E	0x0C8	32
VIC_CB_4TH	RW	0x0091_3622	0x0CC	32
VIC_CB_5TH	RW	0x0051_5AF0	0x0D0	32
VIC_CB_6TH	RW	0x00AA_A610	0x0D4	32
VIC_CB_7TH	RW	0x00D2_1092	0x0D8	32
VIC_CB_8TH	RW	0x006A_CADE	0x0DC	32
VIC_CB2_1ST	RW	0x00EB_8080	0x0E0	32
VIC_CB2_2ND	RW	0x0010_8080	0x0E4	32
VIC_CB2_3RD	RW	0x0029_F06E	0x0E8	32
VIC_CB2_4TH	RW	0x0091_3622	0x0EC	32
VIC_CB2_5TH	RW	0x0051_5AF0	0x0F0	32
VIC_CB2_6TH	RW	0x00AA_A610	0x0F4	32
VIC_CB2_7TH	RW	0x00D2_1092	0x0F8	32
VIC_CB2_8TH	RW	0x006A_CADE	0x0FC	32
ISP_FLASH_STRB	RW	0x0000_0000	0x100	32
ISP_FIFO_OVF_STA	RW	0x0000_0000	0x120	32
ISP_FIFO_OVF_MSK	RW	0x0000_0000	0x124	32
VIC_DVP_PAD_REUSE	RW	0x0000_0000	0x150	32

3.9.2.1 VIC_CTRL Register (VIC_CTRL,0x000)

The VIC_CTRL register is used to start VIC, reset VIC or reset ISP.

	VIC_CTRL	**VIC_BA+0x000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																											VIC_RST	GLB_STOP	GLB_RST	REG_EN	VIC_START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:5	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	R
4	VIC _RST	When this bit is set to 1，the VIC will be reset immediately.	RW
3	GLB_STOP	When this bit is set to 1，the VIC and ISP will be reset when the AXI bus has transited the current burst data.	RW
2	GLB_RST	When this bit is set to 1,the VIC and ISP will be reset immediately.	RW
1	REG_EN	When this bit is set to 1,it indicate the configure registers have been configures, VIC is initializing. When the VIC is already initialized, this bit will be set to 0 automatically.	RW
0	VIC_START	Start VIC, When this bit is 1 set to, the VIC will start working. This bit will be set to 0 automatically when the working space has been started.	RW

3.9.2.2 VIC_RES Register (VIC_RES,0x004)

The VIC_RES register is used to configure the resolution of image.

	VIC_RES																VIC_BA+0x004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	hor_res																ver_res															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	hor_res	Horizontal Size of resolution, maximum horizontal size of a frame is 2688 because of the maximum horizontal of ISP is 2688.	RW
15:0	ver_res	Vertical Size of resolution, maximum vertical size of a frame is 4096.	RW

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3.9.2.3 VIC_FRM_ECC Register (VIC_FRM_ECC,0x008)

The VIC_FRM_ECC register is used to enable VIC frame ecc function

	VIC_FRM_ECC																														VIC_BA+0x008	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																														frame_ecc_mode	frame_ecc_en
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
1	frame_ecc_mode	0=frame will be ecc either VIC enable or disable 1=frame will be ecc only when VIC enable	RW
0	frame_ecc_en	0=Disable frame ecc function 1=Enable frame ecc function	RW

3.9.2.4 VIC_IN_INTF Register (VIC_IN_INTF,0x00C)

The VIC_IN_INTF register is used to select the input interface of VIC.

	VIC_IN_INTF																														VIC_BA+0x00c		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																													INPUT_INTF		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:3	Reserved	Writing has no effect, read as zero.	R
2:0	INPUT_INTF	VIC input interface type. 3'b000：BT 656 3'b001：BT 601 3'b010：MIPI_CSI 3'b011：DVP 3'b100：BT 1120 3'b101：MIPI and DVP in turn 3'b110：LVDS **Note:** the interface timing protocol has been described in 1.7 section.	RW

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3.9.2.5 VIC_IN_DVP Register (VIC_IN_DVP,0x010)

The VIC_IN_DVP register is used to configure the DVP interface of VIC.

	VIC_IN_DVP																															VIC_BA+0x010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved			dvp_img_chk	dvp_bus_select				dvp_rgb_order			dvp_raw_align	dvp_data_format			dvp_mode	Reserved				bt_intf_wide	bt_lsav_eav	bt601_mode	Reserved			yuv_order		Reserved		hsync_porlar	vsync_polar
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	R
28	dvp_img_chk	1=check all vertical and horizon resolution When =1，0x70，0x74 should be configured as ver and hor res. 0=check valid vertical and horizon resolution	RW
27:24	dvp_bus_select	YUV422 or RGB565 or RGB555 pixel's data position in dvp_data[15:0]. (only dvp_data_type=6 or 7, this field is available.) 0000: dvp[7:0] 0001: dvp[8:1] 0010: dvp[9:2] 0011: dvp[10:3] 0100: dvp[11:4] 0101: dvp[12:5] 0110: dvp[13:6] 0111: dvp[14:7] 1000: dvp[15:8]	RW
23:21	dvp_rgb_order	RGB565/555 input sequence from dvp interface. (only dvp_data_type=7, this field is available.) 000：{b[4:0],g[5:3]}, {g[2:0],r[4:0]} 001：{r[4:0],g[5:3]}, {g[2:0],b[4:0]} 010：{g[5:0],r[4:2]}, {r[1:0],b[4:0]} 011：{b[4:0],r[4:2]}, {r[1:0],g[5:0]} 100：{g[5:0],b[4:3]}, {b[2:0],r[4:0]} 101：{r[4:0],b[4:2]}, {b[1:0],g[5:0]}	RW
20	dvp_raw_align	The alignment of raw data for dvp interface 0: low align 1:high align	RW
19:17	dvp_data_format	data type of pixel input from dvp interface. 000: RAW8	RW

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		001: RAW10 010: RAW12 011: YUV422 100: RGB565(16bit IO) 101: RGB888(16bit IO) 110: YUV422(8bit IO) 111: RGB565/555(8bit IO)	
16:15	dvp_timing_mode	dvp interface timing mode 00: href mode 01: hsync mode 10: sony mode 11: reserved **Note**: the dvp interface timing mode has been described in 3.7.1 section.	RW
14:12	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	RW
11	bt_intf_wide	bt 601/656/1120 interface width. 0:8bit 1:16bit	RW
10	bt_sav_eav	line mode indicates the position of EAV and SAV .. 0:EAV before SAV 1:SAV before EAV	RW
9	bt601_ mode	bt601 interface vertical timing mode 0: toggle mode 1:pulse mode	RW
8: 6	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	R
5:4	yuv_data_order	The YUV422 sequence, it is available when input interface is bt656/1120 bt601 or dvp_mode For 8bit interface width, the input yuv order(clock4<-clock0): 00: Y1, V0,Y0,U0 01: Y1, U0,Y0,V0 10: V0, Y1,U0,Y0 11: U0, Y1,V0,Y0 For 16bit interface width, the input yuv order(clock1<-clock0): 00: {Y1, V0}, {Y0,U0} 01: {Y1, U0}, {Y0,V0} 10: {V0, Y1}, {U0,Y0} 11: {U0, Y1}, {V0,Y0} **Note:** when data format is YCbCr, U replaced by Cb, V replaced by Cr	RW
3	start_field	When input interlace image, the first field type. 0:first field is odd. 1:first field is even	RW
2	interlace_en	input image is progress or interlace 0:progress 1:interlace	RW

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1	hsync_polar	external hsync polarity. 0:high active(hsync's posedge indicate one line start) 1:low active (hsync's negedge indicate one line start)	RW
0	vsync_polar	external vsync polarity. 0:high active (vsync's posedge indicate one frame start) 1:low active (vsync's negedge indicate one frame start)	RW

3.9.2.6 VIC_IN_CSI_LVDS_FMT Register (VIC_IN_CSI_LVDS_FMT,0x014)

The VIC_IN_CSI_LVDS_FMT register is used to configure MIPI-CSI interface of VIC.

	VIC_IN_CSI_LVDS_FMT																															VIC_BA+0x014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																							lvds_sensor_type	lvds_lane_num		pixel_format					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect. Read as zero.	R
8	lvds_sensor_type	Select sensor type 0:pansonic type 1:sony type	RW
7:6	lvds_lane_num	Configure the LVDS lane number 0:single lane 1:double lane	RW
5:0	pixel_format	Configure the data type for MIPI_CSI and LVDS input. 0:RAW8 1:RAW10 2:RAW12 3:RGB555 4:RGB565 5:RGB666 6:RGB888 7:YUV422 8:10 bit YUV422	RW

3.9.2.7 VIC_IN_HOR_PARA0 Register (VIC_IN_HOR_PARA0,0x020)

The VIC_IN_HOR_PARA0 register is used to configure horizon parameters for dvp mode.

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	VIC_IN_HOR_PARA0																															VIC_BA+0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	hfb_num																hact_num															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	hfb_num	Horizon front blanking time (unit is pixel clock) **Note**: This bit field be used for bt601、dvp hsync mode、dvp sony mode、lvds mode.	RW
15:0	hact_num	Horizon active time (unit is pixel clock) **Note**: This bit field be used for bt601、dvp hsync mode、dvp sony mode.	RW

3.9.2.8 VIC_IN_HOR_PARA1 Register (VIC_IN_HOR_PARA1,0x024)

The VIC_IN_HOR_PARA1 register is used to configure horizon parameters .

	VIC_IN_HOR_PARA1																															VIC_BA+0x024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserve																hbb_num															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserve	Writing has no effect. Read as zero.	RW
15:0	hbb_num	Horizon back blanking time (unit is pixel clock) **Note:** This bit field used for bt601 interface only	RW

3.9.2.9 VIC_IN_VER_PARA0 Register (VIC_IN_VER_PARA0,0x030)

The VIC_IN_VER_PARA0 register is used to configure odd frame VFB and VACT.

	VIC_IN_VER_PARA0																															VIC_BA+0x030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

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	odd_vfb																odd_vact															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	odd_vfb	Odd frame vertical front porch blanking. Unit is line **Note:** This bit field only be used for bt601、lvds mode.	RW
15:0	odd_vact	Odd frame vertical active line **Note:** This bit field only be used for bt601.	RW

3.9.2.10 VIC_IN_VER_PARA1 Register (VIC_IN_VER_PARA1,0x034)

The VIC_IN_VER_PARA1 register is used to configure odd frame VBB and even frame VFB

	VIC_IN_VER_PARA1																**VIC_BA+0x034**															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	odd_vbb																even_vfb															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	odd_vbb	Odd frame vertical back porch blanking. Unit is line **Note**: This bit field only be used for bt601.	RW
15:0	even_vfb	Even frame vertical front porch blanking. Unit is line **Note**: This bit field only be used for bt601.	RW

3.9.2.11 VIC_IN_VER_PARA2 Register (VIC_IN_VER_PARA2,0x038)

The VIC_IN_VER_PARA2 register is used to configure vertical parameters.

	VIC_IN_VER_PARA2																**VIC_BA+0x038**															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

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	even_vact																even_vbb															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	even_vact	Even frame vertical active line **Note**: This bit field only be used for bt601.	RW
15:0	even_vbb	Even frame vertical back porch blanking. Unit is line **Note**: This bit field only be used for bt601.	RW

3.9.2.12 VIC_IN_VER_PARA3 Register (VIC_IN_VER_PARA3,0x03C)

The VIC_IN_VER_PARA3 register is used to configure dvp vertical front blanking for dvp hsync mode.

	VIC_IN_VER_PARA3																															**VIC_BA+0x03C**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN_VPARA3																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	IN_VER_PARA3	DVP vertical sync front porch blanking. Unit is pixel clock. **Note**: This bit field be used for dvp hsync and sony mode.	RW

3.9.2.13 VIC_OUT_CFG Register (VIC_OUT_CFG,0x050)

The VIC_OUT_CFG register is used to configure the output ports protocol.

	VIC_OUT_CFG																															**VIC_BA+0x050**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									isp_port_mod		vcke_enable	blank_enable		ab_mode_sel	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W

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31:7	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	R
6:5	isp_port_mod	These bits indicate the isp input port preset mode. Isp_port_mode: 2'b00, preset mode1. 2'b01, preset mode2. 2'b10,preset mode3. **NOTE:** Isp_port_mode must be configured, when VIC is working.	RW
4	vcke_enable	Indicate the vic is working in vcke mode or not. When this bit is set to 1, vic is vcke mode. In vcke mode, the output signal of vic, vcke, will deassert when the output data of vic is invalid.	RW
3:2	blank_enable	Indicate the vertical blanking or horizontal blanking is constant or dynamic. Blank enable function just be used for preset mode2 of ISP. Blank enable[3:2]: 2'b00: horizontal blanking is dynamic and the vertical blanking is dynamic. 2'b01: horizontal blanking is constant and the vertical blanking is dynamic. 2'b10: horizontal blanking is dynamic and the vertical blanking is constant. 2'b11: horizontal blanking is constant and the vertical blanking is constant. **NOTES:** If Blank is enable, you must configure the blanking value.	RW
1:0	ab_mode_select	Indicate the relationship between vvalid and hvalid. ab mode select[1:0]: 2'b00:vvalid and hvalid is synchronized. 2'b01:vvalid rising edge is ahead of first line hvalid rising edge and the vvalid falling edge synchronized with hvalid falling edge. **Note**: When ISP is working in preset mode1,this configuration value indicate the vvalid pulse occurring after the last line hvalid falling edge b value cycle. 2'b10:vvalid rising edge is synchronized with first line hvalid rising edge and the vvalid falling edge is behind of last hvalid falling edge. 2'b11:vvalid rising edge is ahead of first line hvalid rising edge and the vvalid falling edge is behind of last line hvalid rising edge .	RW

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		NOTES: If ab mode is enable, you must configure the ab value. Referring to the isp's input preset mode.	

Note:

Preset mode 1 supports sensors with a short single clock cycle FV pulse which occurs at the end of the frame and a horizontal valid which encapsulates the video as shown in the timing diagram below.

Symbol	Definition	Min	Max	Units
A	HV falling edge of last line to FV rising edge	0	100	Pixel CLK cycles

Preset mode 2 supports typical sensor sync outputs with both FV and HV signals encapsulating the active video as shown below. The input port expects constant horizontal and vertical blanking periods with the active video encapsulated by the FV and HV pulse.

Symbol	Definition	Min	Max	Units
A	FV rising edge to HV rising edge of first line	0	Vertical blanking -1	Pixel CLK cycles
B	HV falling edge of last line to FV falling edge	0	100	Pixel CLK cycles

Preset Mode 3 supports sensor sync outputs with a continuous HV running during the vertical blanking period and both FV and HV signals exactly encapsulate the active video. This mode can also support variable horizontal blanking periods.

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Symbol	Definition	Min	Max	Units
A	FV rising edge to HV rising edge of first line	0	Horizontal blanking -1	Pixel CLK cycles
B	HV falling edge of last line to FV falling edge	0	100	Pixel CLK cycles

3.9.2.14 VIC_OUT_ABVAL Register (VIC_OUT_ABVAL,0x054)

The VIC_OUT_ABVAL register is used to configure the pixel clk cycles between vvalid edge and hvalid edge, when the VIC is working in ab mode.

	VIC_OUT_ABVAL																															VIC_BA+0x054
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	a_value																Reserved									b_value						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	a_value	The pixel clk cycles of vvalid rising edge to hvalid rising edge of first line. If the current ISP input port is working in a mode or ab mode, these bits must be set. In preset mode2,the maximum value is Vertical blanking-1'b1.In preset mode3,the maximum value is Horizontal blanking-1'b1.	RW
15:7	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	R
6:0	b_value	The pixel clk cycles of hvalid falling edge of last line to vvalid falling edge. If the current ISP input port is ab mode, these bits must be set.	RW

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3.9.2.15 VIC_OUT_HBLK Register (VIC_OUT_HBLK,0x058)

The VIC_OUT_HBLK register is used to configure the Horizontal blank number of output data, when VIC is working in preset mode2. If the VIC is working in preset mode1 or preset mode3, this register should not be configured.

	VIC_OUT_HBLK																															VIC_BA+0x058
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	vic_out_hblk																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	vic_output_hblk	The Horizontal blanking number of current transition. The minimum number is 32 pixel.	RW

3.9.2.16 VIC_OUT_VBLK Register (VIC_OUT_VBLK,0x05C)

The VIC_OUT_VBLK register is used to configure the Vertical blank number of output data, when VIC is working in preset mode2. If the VIC is working in preset mode1 or preset mode3, this register mustn't be configured.

	VIC_OUT_VBLK																															VIC_BA+0x05C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	vic_out_vblk																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	vic_out_vblk	The Vertical blanking number of current transition. The minimum number is 20 line*(Horizontal Size +Horizontal _blank).	RW

3.9.2.17 VIC_VLD_LINE_SAV Register (VIC_VLD_LINE_SAV,0x060)

The VIC_VLD_LINE_SAV register is used to configure the valid line sav for dvp sony mode and lvds mode.

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	VIC_VLD_LINE_SAV																															VIC_BA+0x060
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_vld_line_sav																							
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_vld_line_sav	The valid line sav for dvp sony mode and lvds mode, default 0x800800	R

3.9.2.18 VIC_VLD_LINE_EAV Register (VIC_VLD_LINE_EAV,0x064)

The VIC_VLD_LINE_EAV register is used to configure the valid line eav for dvp sony mode and lvds mode.

	VIC_VLD_LINE_EAV																															VIC_BA+0x064
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_vld_line_eav																							
RST	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_vld_line_eav	The valid line eav for dvp sony mode and lvds mode, default 0x9D09D0	R

3.9.2.19 VIC_INVLD_LINE_SAV Register (VIC_INVLD_LINE_SAV,0x068)

The VIC_INVLD_LINE_SAV register is used to configure invalid line sav for lvds mode.

	VIC_INVLD_LINE_SAV																															VIC_BA+0x068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_invld_line_sav																							
RST	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	0	0	0	1	0	1	0	1	0	1	1	0	0	0	0

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Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_invld_line_sav	The invalid line sav for lvds mode, default 0xAB0AB0	R

3.9.2.20 VIC_INVLD_LINE_EAV Register (VIC_INVLD_LINE_EAV,0x06C)

The VIC_INVLD_LINE_EAV register is used to configure invalid line eav for lvds mode.

	VIC_INVLD_LINE_EAV																															VIC_BA+0x06C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_invld_line_eav																							
RST	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	0	0	0	0	0	1	0	1	1	0	1	1	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_invld_line_eav	The invalid line eav for lvds mode, default 0xB60B60	R

3.9.2.21 VIC_VLD_FRM_SAV Register (VIC_VLD_FRM_SAV,0x070)

The VIC_VLD_FRM_SAV register is used to configure valid frame sav for lvds mode or vertical resolution for dvp mode .

	VIC_VLD_FRM_SAV																															VIC_BA+0x070
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_vld_frm_sav																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_vld_frm_sav	For lvds mode ,it means the valid frame sav, and for dvp mode, it means the valid vertical resolution , default 0x006002 (Only in mode pansonic)	R

3.9.2.22 VIC_VLD_FRM_EAV Register (VIC_VLD_FRM_EAV,0x074)

The VIC_VLD_FRM_EAV register is used to configure valid frame eav for lvds mode or horizon

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resolution for dvp mode .

	VIC_VLD_FRM_EAV																															VIC_BA+0x074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_vld_frm_eav																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_vld_frm_eav	For lvds mode ,it means the valid frame eav, and for dvp mode, it means the valid horizon resolution, default 0x007003 (Only in mode pansonic)	R

3.9.2.23 VIC_WORK_STA Register (VIC_WORK_STA,0x090)

The VIC_WORK_STA register is read only register, it indicates the working state of VIC.

	VIC_WORK_STA																															VIC_BA+0x090
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													work_sta		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:3	Reserved	Writing has no effect, read as zero.	R
2:0	WORK_STATE	It indicates the main control state machine states .when vic is working, it should be 1~5 states in turn. if vic is always a state without change, it may don't work. 0:idle state 1:a phase state 2:horiziontal valid state 3:horizontal blanking state 4:b phase state 5:vertical blanking states	R

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3.9.2.24 VIC_PIXEL_CNT Register (VIC_PIXEL_CNT,0x094)

The VIC_PIXEL_CNT register is a state register, it indicate the remain pixel number and the complete pixel number of the current line.

	VIC_ PIXEL_CNT																															VIC_BA+0x094
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				complete_pixel											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	COMPLETE_PIXEL	It indicate the pixel number of current line has been transited completely .	R

3.9.2.25 VIC_ROW_CNT Register (VIC_ROW_CNT,0x098)

The VIC_ROW_CNT register is a state register, it indicates the remain line number and the complete line number of the current frame.

	VIC_ ROW_CNT																															VIC_BA+0x098
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				complete_line											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	complete_line	It indicate the line number of current frame has been transited. **NOTE**: Complete line dosen't include the current transiting line.	R

3.9.2.26 VIC_OFIFO_CNT Register (VIC_OFIFO_CNT,0x09C)

The VIC_OFIFO_CNT register is a count state register, it indicates the storage usage of VIC out fifo.

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	VIC_OFIFO_CNT																															VIC_BA+0x09C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					used entry										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect. Read as zero.	R
10:0	USED_ ENTRY	The storage usage of VIC out fifo.	R

3.9.2.27 VIC_FRT_CB_CTRL Register (VIC_FRT_CB_CTRL, 0x0A0)

The VIC_FRT_CB_CTRL register is used to config the VIC's front color bar.

	VIC_FRT_CB_CTRL																															VIC_BA+0x0AC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	enable	replace	Reserved														frame_num															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	enable	Color bar mode1 enable	RW
30	replace	Replace input data for dvp href mode when Enable colorbar =0	RW
29:16	Reserved	Writing has no effect. Read as zero.	RW
15:0	frame_num	When frame_num[15:0]=16'h8000, frame number is infinite. When frame_num[15]=0, frame number is frame_num[14:0]	RW

Note: when use front colorbar, you should configure VIC_RESOLUTION(0x004), VIC_INPUT_DVP(0x010) dvp_msb & dvp_data_type field(only support raw8/10/12&yuv422).

3.9.2.28 VIC_FRT_CB_BLK Register (VIC_FRT_CB_BLK, 0x0A4)

The VIC_FRT_CB_BLK register is used to configure the VIC's front color bar blanking number.

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	VIC_FRT_CB_BLK																VIC_BA+0x0A4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HOR_ BLANK																VER_BLANK															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	HOR_BLANK	Horizon blank number(unit is work clock)	RW
15:0	VER_BLANK	Vertical blank number(unit is line)	RW

3.9.2.29 VIC_BK_CB_CTRL Register (VIC_BK_CB_CTRL, 0x0B0)

The VIC_BK_CB_CTRL register is used to configure the VIC' back color bar.

	VIC_BK_CB_CTRL																VIC_BA+0x0B0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	enable	incremenal_mode	direction	pixel_format	Reserved											color_bar_dir	frame_num															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	enable	Color bar mode0 enable	RW
30	incremetal_mode	Increase or constant value 1：increase in each line 0：each color bar is constant value（8 bars, each bar's value can be configure）	RW
29	direction	0：horizon color bar 1：vertical color bar(only available when bit30=0、bit26=0)	RW
28:27	pixel_format	0：raw format 1：yuv422 format 2：rgb format (only available when bit30=0)	RW
26	color_bar_dir	0：invalid 1：horizon color bar and vertical color bar each frame switch	RW
25:16	Reserved	Writing has no effect, read as zero.	RW
16	free_bar_blk	0: horizon blank and vertical blank according to 0x0B4 1: free horizon blank and vertical blank	

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15:0	frame_num	When frame_num=16'h8000, frame number is infinite, When frame_num[15]=0, frame number is frame_num[14:0]	RW

3.9.2.30 VIC_BK_CB_BLK Register (VIC_BK_CB_BLK, 0x0B4)

The VIC_BK_CB_BLK register is used to configure the VIC's front color bar blanking number.

	VIC_BK_CB_BLK																															VIC_BA+0x0B4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	hor_ blank																ver_blank															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	hor_blank	horizon blank number(unit is work clock)	RW
15:0	ver_blank	vertical blank number(unit is line)	RW

3.9.2.31 VIC_CB_1ST Register (VIC_CB_1ST,0x0C0)

The VIC_CB_1ST register is used to configure the first color bar's YUV

	VIC_CB_1ST																															VIC_BA+0x0C0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_ value								cb_ alue								cr_value							
RST	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	Y component value	RW
15:8	cb_value	Cb component value	RW
7:0	cr_ value	Cr component value	RW

3.9.2.32 VIC_CB_2ND Register (VIC_CB_2ND,0x0C4)

The VIC_CB_2ND register is used to configure the second color bar's YUV.

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	VIC_CB_2ND																															VIC_BA+0x0C4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_ value								cb_ value								cr_ value							
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect. Read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

3.9.2.33 VIC_CB_3RD Register (VIC_CB_3RD,0x0C8)

The VIC_CB_3RD register is used to configure the third color bar's YUV .

	VIC_CB_3RD																															VIC_BA+0x0C8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_value								cb_ value								cr_ value							
RST	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	1	1	0	1	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect Read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

3.9.2.34 VIC_CB_4TH Register (VIC_CB_4TH,0x0CC)

The VIC_CB_4TH register is used to configure the fourth color bar's YUV

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	VIC_CB_4TH																															VIC_BA+0x0CC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_value								cb_ value								cr_ value							
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	1	1	0	1	0	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

3.9.2.35 VIC_CB_5TH Register (VIC_CB_5TH,0x0D0)

The VIC_CB_5TH register is used to configure the fifth color bar's YUV

	VIC_CB_5TH																															VIC_BA+0x0D0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_ value								cb_ value								cr_ value							
RST	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	1	1	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

3.9.2.36 VIC_CB_6TH Register (VIC_CB_6TH,0x0D4)

The VIC_CB_6TH register is used to configure the sixth color bar's YUV

	VIC_CB_6TH																															VIC_BA+0x0D4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y__value								cb_value								cr_value							
RST	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0

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Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	Y component value	RW
15:8	cb_value	Cb component value	RW
7:0	cr_value	Cr component value	RW

3.9.2.37 VIC_CB_7TH Register (VIC_CB_7TH,0x0D8)

The VIC_CB_7TH register is used to configure the seventh color bar's YUV.

	VIC_SEVENTH_CB																															VIC_BA+0x0D8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_value								cb_value								cr_value							
RST	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

3.9.2.38 VIC_CB_8TH Register (VIC_CB_8TH,0x0DC)

The VIC_CB_8TH register is used to configure the eighth color bar's YUV.

	VIC_CB_8TH																															VIC_BA+0x0DC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_value								cb_value								cr_value							
RST	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	1	0	0	1	0	1	0	1	1	0	1	1	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

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3.9.2.39 VIC_CB2_1ST Register (VIC_CB2_1ST,0x0E0)

The VIC_CB2_1ST register is used to configure the first color bar's RAW line2

	VIC_CB2_1ST																															VIC_BA+0x0E0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value												raw22_value											
RST	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

3.9.2.40 VIC_CB2_2ND Register (VIC_CB2_2ND,0x0E4)

The VIC_CB2_2ND register is used to configure the second color bar's RAW line2

	VIC_CB2_2ND																															VIC_BA+0x0E4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved								raw21_value												raw22_value											
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

3.9.2.41 VIC_CB2_3RD Register (VIC_CB2_3RD,0x0E8)

The VIC_CB2_3RD register is used to configure the third color bar's RAW.

	VIC_CB2_3RD																															VIC_BA+0x0E8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved								raw21_value												raw22_value											
RST	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	1	1	0	1	1	1	0

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Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

3.9.2.42 VIC_CB2_4TH Register (VIC_CB2_4TH,0x0EC)

The VIC_CB2_4TH register is used to configure the fourth color bar's YUV

	VIC_CB2																															VIC_BA+0x0EC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value								raw22_value															
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	1	1	0	1	0	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

3.9.2.43 VIC_CB2_5TH Register (VIC_CB2_5TH,0x0F0)

The VIC_CB2_5TH register is used to configure the fifth color bar's RAW.

	VIC_CB2_5TH																															VIC_BA+0x0F0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value								raw22_value															
RST	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	1	1	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

3.9.2.44 VIC_CB2_6TH Register (VIC_CB2_6TH,0x0F4)

The VIC_CB2_6TH register is used to configure the sixth color bar's YUV

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	VIC_CB2_6TH																															VIC_BA+0x0F4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value								raw22_value															
RST	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

3.9.2.45 VIC_CB2_7TH Register (VIC_CB2_7TH,0x0F8)

The VIC_CB2_7TH register is used to configure the seventh color bar's RAW.

	VIC_CB2_7TH																															VIC_BA+0x0F8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value								raw22_value															
RST	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

3.9.2.46 VIC_CB2_8TH Register (VIC_CB2_8TH,0x0FC)

The VIC_CB2_8TH register is used to configure the eighth color bar's RAW.

	VIC_CB2_8TH																															VIC_BA+0x0FC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value								raw22_value															
RST	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	1	0	0	1	0	1	0	1	1	0	1	1	1	1	0

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Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect. Read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

3.9.2.47 ISP_FLASH_STRB Register(ISP_FLASH_STRB,0x100)

The ISP_FLASH_STRB register is used to control the isp flash strobe in1.

	ISP_FLASH_STRB																															VIC_BA+0x100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																															FLASH_STRB
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	FLASH_STRB	This bit is used to control the flash strobe. This bit is active high.	RW

3.9.2.48 ISP_FIFO_OVF_STA Register(ISP_FIFO_OVF_STA,0x120)

The ISP_FIFO_OVF_STA register is used to store the isp_core dmas' fifo full and empty fail status.

	ISP_FIFO_OVF_STA																															VIC_BA+0x120
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved												ds2 wfifo full	ds2 wfifo empty	ds2uv wfifo full	ds2uv wfifo empty	ds1 wfifo full	ds1 wfifo empty	ds1uv wfifo full	ds1uv wfifo empty	fr wfifo full	fr wfifo empty	fruv wfifo full	fruv wfifo empty	wdr wfifo full	wdr wfifo empty	wdr rfifo full	wdr rfifo empty	Temper wfifo full	Temper wfifo empty	Temper rfifo full	Temper rfifo empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	Reserved	Writing has no effect. Read as zero.	R
19	ds2 wfifo full fail	ds2 frame buffer wfifo full fail; Write 1 clear.	RW
18	ds2 wfifo empty fail	ds2 frame buffer wfifo empty fail; write 1 clear.	RW

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17	ds2uv wfifo full fail	ds2uv frame buffer wfifo full fail; write 1 clear.	RW
16	ds2uv wfifo empty fail	ds2uv frame buffer wfifo empty fail, Write 1 clear.	RW
15	ds1 wfifo full fail	ds1 frame buffer wfifo full fail, write 1 clear.	RW
14	ds1 wfifo empty fail	ds1 frame buffer wfifo empty fail, write 1 clear.	RW
13	ds1uv wfifo full fail	ds1uv frame buffer wfifo full fail, write 1 clear.	RW
12	ds1uv wfifo empty fail	ds1uv frame buffer wfifo empty fail, write 1 clear.	RW
11	fr w fifo full fail	fr frame buffer wfifo full fail, write 1 clear.	RW
10	fr wfifo empty fail	fr frame buffer wfifo empty fail, write 1 clear.	RW
9	fruv wfifo full fail	fruv frame buffer wfifo full fail, write 1 clear.	RW
8	fruv wfifo empty fail	fruv frame buffer wfifo empty fail, write 1 clear.	RW
7	wdr wfifo full fail	wdr frame buffer wfifo full fail, write 1 clear.	RW
6	wdr wfifo empty fail	wdr frame buffer wfifo empty fail, write 1 clear.	RW
5	wdr rfifo full fail	wdr frame buffer rfifo full fail, write 1 clear.	RW
4	wdr rfifo empty fail	wdr frame buffer rfifo empty fail, write 1 clear.	RW
3	temper wfifo full fail	temper frame buffer wfifo full fail, write 1 clear.	RW
2	temper wfifo empty fail	temper frame buffer wfifo empty fail, write 1 clear.	RW
1	temper rfifo full fail	temper frame buffer rfifo full fail, write 1 clear.	RW
0	temper rfifo empty fail	temper frame buffer rfifo empty fail, write 1 clear.	RW

3.9.2.49 ISP_FIFO_OVF_MSK Register(ISP_FIFO_OVF_MSK,0x124)

ISP_FIFO_OVF_MSK register is used to mask the isp_core dmas' fifo full and empty fail interrupt.

	ISP_FIFO_OVF_MSK																															VIC_BA+0x124
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												ds2 wfifo full msk	ds2 wfifo empty msk	ds2uv wfifo full msk	ds2uv wfifo empty msk	ds1 wfifo full msk	ds1 wfifo empty msk	ds1uv wfifo full msk	ds1uv wfifo empty msk	fr wfifo full msk	fr wfifo empty msk	fruv wfifo full msk	fruv wfifo empty msk	wdr wfifo full msk	wdr wfifo empty msk	wdr rfifo full msk	wdr rfifo empty msk	Temper wfifo full msk	Temper wfifo empty msk	Temper rfifo full msk	Temper rfifo empty msk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	Reserved	Writing has no effect, read as zero.	R
19	ds2 wfifo full fail msk	ds2 frame buffer wfifo full fail mask	RW
18	ds2 wfifo empty fail msk	ds2 frame buffer wfifo empty fail mask	RW
17	ds2uv wfifo full fail msk	ds2uv frame buffer wfifo full fail mask	RW
16	ds2uv wfifo empty fail msk	ds2uv frame buffer wfifo empty fail mask	RW
15	ds1 wfifo full fail msk	ds1 frame buffer wfifo full fail mask	RW
14	ds1 wfifo empty fail msk	ds1 frame buffer wfifo empty fail mask	RW
13	ds1uv wfifo full fail msk	ds1uv frame buffer wfifo full fail mask	RW

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12	ds1uv wfifo empty fail msk	ds1uv frame buffer wfifo empty fail mask	RW
11	fr wfifo full fail msk	fr frame buffer wfifo full fail mask	RW
10	fr wfifo empty fail msk	fr frame buffer wfifo empty fail mask	RW
9	fruv wfifo full fail msk	fruv frame buffer wfifo full fail mask	RW
8	fruv wfifo empty fail msk	fruv frame buffer wfifo empty fail mask	RW
7	wdr wfifo full fail msk	wdr frame buffer wfifo full fail mask	RW
6	wdr wfifo empty fail msk	wdr frame buffer wfifo empty fail mask	RW
5	wdr rfifo full fail msk	wdr frame buffer rfifo full fail mask, 1 is valid.	RW
4	wdr rfifo empty fail msk	wdr frame buffer rfifo empty fail mask, 1 is valid.	RW
3	temper wfifo full fail msk	temper frame buffer wfifo full fail mak, 1 is valid.	RW
2	temper wfifo empty fail msk	temper frame buffer wfifo empty fail mask, 1 is valid.	RW
1	temper rfifo full fail msk	temper frame buffer rfifo full fail mask, 1 is valid.	RW
0	temper rfifo empty fail msk	temper frame buffer rfifo empty fail mask, 1 is valid.	RW

3.9.2.50 VIC_DVP_PAD_REUSE Register (VIC_DVP_PAD_REUSE,0x150)

The VIC_DVP_PAD_REUSE register is used to enable dvp mode reuse the low 6 bits of mipi_phy data.

	VIC_DVP_PAD_REUSE																															VIC_BA+0x150	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														dvp_pad_reuse	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect, read as zero.	R
1	dvp_pad_reuse	When input interface of VIC is DVP ,this bit is set to 1	RW
0	Reserved	Writing has no effect, read as zero.	R

3.9.3 DMA registers

Table 3-21 DMA Registers Map

Name	RW	Reset Value	Address Offset	Access Size
DMA_CONFIGURE	RW	0x0000_0000	0x000	32
DMA_RESOLUTION	RW	0x0000_0000	0x004	32
DMA_RESET	RW	0x0000_0000	0x008	32
DMA_Y_CH_LINE_STRIDE	RW	0x0000_0000	0x014	32

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DMA_Y_CH_BUF0_ADDR	RW	0x0000_0000	0x018	32
DMA_Y_CH_BUF1_ADDR	RW	0x0000_0000	0x01C	32
DMA_Y_CH_BUF2_ADDR	RW	0x0000_0000	0x020	32
DMA_Y_CH_BUF3_ADDR	RW	0x0000_0000	0x024	32
DMA_Y_CH_BUF4_ADDR	RW	0x0000_0000	0x028	32
DMA_UV_CH_STRIDE	RW	0x0000_0000	0x034	32
DMA_UV_CH_BUF0_ADDR	RW	0x0000_0000	0x038	32
DMA_UV_CH_BUF1_ADDR	RW	0x0000_0000	0x03C	32
DMA_UV_CH_BUF2_ADDR	RW	0x0000_0000	0x040	32
DMA_UV_CH_BUF3_ADDR	RW	0x0000_0000	0x044	32
DMA_UV_CH_BUF4_ADDR	RW	0x0000_0000	0x048	32

3.9.3.1 DMA Configure Register(DMA_CONFIGURE,0x000)

The DMA_CONFIGURE register is used to control the DMA.

	DMA_CONFIGURE																																	DMA_BA+0x000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	dma en	Reserved																					yuv422_order		uv_sample	buffer_number				base_mode		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	dma en	enable DMA	RW
30:8	Reserved	Writing has no effect, read as zero.	R
9:8	yuv422_order	The order in ddr ram for YUV422 packet(base_mode=3) 0：Y2V1Y1U1 1：Y1U1Y2V1 2：V1Y2 U1Y1 3：U1Y1V1Y2	RW
7	uv_sample	0:sample yuv 422 odd line's uv to yuv420 1:sample yuv 422 even line's uv to yuv420	RW
6:3	Buffer_number	Output buffer number. Value(0~4) is actual buffer number(1~5) minus 1.	RW
2:0	base_mode	Dma output data format. 0: RAW8/10/12 1: RGB565 2: RGB888 3: YUV422 packet 4: YUV422 semi-plannar0	RW

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		5: YUV422 semi-plannar1 6: NV12 7: NV21 *For more details,please refer to "1.9.3 output data"*	

3.9.3.2 DMA Resolution Register (DMA_RESOLUTION,0x004)

The DMA_RES register is used to configure the resolution of image.

	DMA_RESOLUTION																DMA_BA+0x004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HORIZONTAL_RESOLUTION																VERTICAL_RESOLUTION															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	HORIZONTAL_ RESOLUTION	The Horizontal Size of resolution, maximum horizontal size of a frame is 2688 because of the maximum horizontal of ISP is 2688.	RW
15:0	VERTICAL_ RESOLUTION	The Vertical Size of resolution, the maximum vertical size of a frame is 4096.	RW

3.9.3.3 DMA RESET Register (DMA_RESET,0x008)

The DMA_RESET register is used to enable and disable DMA.

	DMA_RESET																DMA_BA+0x008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															DMA_RESET
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero. As default,please setting these bits 0.	R
0	DMA _RESET	When this bit is set to 1，the DMA will be reset immediately.	RW

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3.9.3.4 DMA Y Channel Line Stride Register (DMA_Y_CH_STRIDE,0x014)

The DMA_Y_CH_STRIDE register is used to gate the line stride for y channel buffer.

	DMA_Y_CH_STRIDE																															DMA_BA+0x014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_STRIDE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_Y_CH_STRIDE	the line stride for y channel buffer.uint is byte.	RW

3.9.3.5 DMA Y Channel Buffer0 Addres Register (DMA_Y_CH_BUF0_ADDR,0x018)

The DMA_Y_CH_BUF0 register is used to configure the Y channel buffer0 address.

	DMA_Y_CH_BUF0_ADDR																															DMA_BA+0x018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF0_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF0_ADDR	the Y channel buffer0 address.uint is byte.	RW

3.9.3.6 DMA Y Channel Buffer1 Addres Register (DMA_Y_CH_BUF1_ADDR,0x01C)

The DMA_Y_CH_BUF1 register is used to configure the Y channel buffer1 address.

	DMA_Y_CH_BUF1_ADDR																															DMA_BA+0x01C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF1_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF1_ADDR	the Y channel buffer1 address.uint is byte.	RW

3.9.3.7 DMA Y Channel Buffer2 Addres Register (DMA_Y_CH_BUF2_ADDR,0x020)

The DMA_Y_CH_BUF2 register is used to configure the Y channel buffer2 address.

	DMA_Y_CH_BUF2_ADDR																																DMA_BA+0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF2_ADDR																																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF2_ADDR	the Y channel buffer2 address.uint is byte.	RW

3.9.3.8 DMA Y Channel Buffer3 Addres Register (DMA_Y_CH_BUF3_ADDR,0x024)

The DMA_Y_CH_BUF3 register is used to configure the Y channel buffer3 address.

	DMA_Y_CH_BUF3_ADDR																																DMA_BA+0x024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF3_ADDR																																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF3_ADDR	the Y channel buffer3 address.uint is byte.	RW

3.9.3.9 DMA Y Channel Buffer4 Addres Register (DMA_Y_CH_BUF4_ADDR,0x028)

The DMA_Y_CH_BUF4 register is used to configure the Y channel buffer4 address.

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	DMA_Y_CH_BUF4_ADDR																															DMA_BA+0x028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF4_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF4_ADDR	the Y channel buffer4 address.uint is byte.	RW

3.9.3.10 DMA UV Channel Line Stride Register (DMA_UV_CH_STRIDE,0x034)

The DMA_UV_CH_STRIDE register is used to gate the line stride for y channel buffer.

	DMA_UV_CH_STRIDE																															DMA_BA+0x034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_STRIDE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_UV_CH_STRIDE	the line stride for y channel buffer.uint is byte.	RW

3.9.3.11 DMA UV Channel Buffer0 Addres Register (DMA_UV_CH_BUF0_ADDR,0x038)

The DMA_UV_CH_BUF0 register is used to configure the UV channel buffer0 address.

	DMA_UV_CH_BUF0_ADDR																															DMA_BA+0x038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF0_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF0_ADDR	the UV channel buffer0 address.uint is byte.	RW

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3.9.3.12 DMA UV Channel Buffer1 Addres Register (DMA_UV_CH_BUF1_ADDR,0x03C)

The DMA_UV_CH_BUF1 register is used to configure the UV channel buffer1 address.

	DMA_UV_CH_BUF1_ADDR																															DMA_BA+0x03C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF1_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF1_ADDR	the UV channel buffer1 address.uint is byte.	RW

3.9.3.13 DMA UV Channel Buffer2 Addres Register (DMA_UV_CH_BUF2_ADDR,0x040)

The DMA_UV_CH_BUF2 register is used to configure the UV channel buffer2 address.

	DMA_UV_CH_BUF2_ADDR																															DMA_BA+0x040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF2_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF2_ADDR	the UV channel buffer2 address.uint is byte.	RW

3.9.3.14 DMA UV Channel Buffer3 Addres Register (DMA_UV_CH_BUF3_ADDR,0x044)

The DMA_UV_CH_BUF3 register is used to configure the UV channel buffer3 address.

	DMA_UV_CH_BUF3_ADDR																															DMA_BA+0x044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF3_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF3_ADDR	the UV channel buffer3 address.uint is byte.	RW

3.9.3.15 DMA UV Channel Buffer4 Addres Register (DMA_UV_CH_BUF4_ADDR,0x048)

The DMA_UV_CH_BUF4 register is used to configure the UV channel buffer4 address.

	DMA_UV_CH_BUF4_ADDR																															
																																DMA_BA+0x048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF4_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF4_ADDR	the UV channel buffer4 address.uint is byte.	RW

3.9.4 LFB registers

Table 3-22 LFB Registers Map

Name	RW	Reset Value	Address Offset	Access Size
LFB_CTRL	RW	0x0012_0080	0x200	32
LFB_RESTART	RW	0x0000_0000	0x204	32
LFB_HBLK_CFG	RW	0x0000_0000	0x208	32
LFB_Y_CFG	RW	0x0000_0000	0x210	32
LFB_Y_RES	RW	0x0000_0000	0x214	32
LFB_Y_BUF0_ADDR	RW	0x0000_0000	0x218	32
LFB_Y_BUF1_ADDR	RW	0x0000_0000	0x21C	32
LFB_Y_BUF2_ADDR	RW	0x0000_0000	0x220	32
LFB_Y_BUF3_ADDR	RW	0x0000_0000	0x224	32
LFB_Y_BUF4_ADDR	RW	0x0000_0000	0x228	32
LFB_UV_CFG	RW	0x0000_0000	0x230	32
LFB_UV_RES	RW	0x0000_0000	0x234	32
LFB_UV_BUF0_ADDR	RW	0x0000_0000	0x238	32
LFB_UV_BUF1_ADDR	RW	0x0000_0000	0x23C	32
LFB_UV_BUF2_ADDR	RW	0x0000_0000	0x240	32
LFB_UV_BUF3_ADDR	RW	0x0000_0000	0x244	32
LFB_UV_BUF4_ADDR	RW	0x0000_0000	0x248	32
LFB_ERR	RW	0x0000_0000	0x24C	32
LFB_DEBUG0	R	0x0000_0000	0x260	32

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LFB_DEBUG1	R	0x0000_0000	0x264	32
LFB_DEBUG2	R	0x0000_0000	0x268	32
LFB_DEBUG3	R	0x0000_0000	0x26C	32
LFB_DEBUG4	R	0x0000_0000	0x270	32
LFB_DEBUG5	R	0x0000_0000	0x274	32
LFB_DEBUG6	R	0x0000_0000	0x278	32
LFB_DEBUG7	R	0x0000_0000	0x27C	32

3.9.4.1 LFB_CTRL Register(LFB_CTRL,0x200)

	LFB_CTRL																															LFB_BA+0x200
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									no_frame_chk	disable_msc	hsycn_dond	vsync_delay				bvalid_delay									out_sel	uv_switch	alwready_sel	ch_sel	Recov_mode	disable_check_err	lfb_en
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:23	Reserved	Writing has no effect, read as zero.	R
22	no_frame_chk	0=lfb count frame buffer number and order 1=lfb doesn't count frame buffer number and order **Note:** This bit default value is 0,and don't need configure generally.	RW
21	disable_msc	This bit should be configure to 1 when lfb output to NCU and NCU don't output to MSCALER, otherwise should be 0	RW
20	vsync_cond	0=lfb can transmit next frame who doesn't need wait NCU or MSCALER complete current frame. 1=lfb can transmit next frame until NCU or MSCALER complete current frame. **Note**: This bit default value is 1, and don't need configure generally.	RW
19:15	hsync_delay	The interval clock numbers between first hsync and vsync. It should be configure according NCU or MSCALE's requestion. **Note**: The field bits default value is 4, and don't need configure generally.	RW
14：7	bvalid_delay	The interval clock numbers between bvalid and wlast. **Note**: This field bits default is 1,and don't need configure generally.	RW
6	out_sel	0=output to NCU	RW

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		1=output to mscaler	
5	uv_switch	Input and output image format are not same. For example, input is NV12,output is NV21.it should be configure to 1. Otherwise it should be 0.	RW
4	awready_sel	Lfb's awready is always 1 or generate according lfb fifo status. 0=according lfb fifo status. 1=always 1. **Note**: This bit field default value is 0,and don't need configure generally.	RW
3	ch_sel	0= lfb input is from ISP's fr channel 1= lfb input is from ISP's ds1 channel	RW
2	recovery_mode	The recovery mode when axi address errors or fifo overflow occur. 0=software recovery, Ncu and Mscaler should be reset by software, then LFB_CONTROL.restart should be set to 1, and lfb will restart. 1=hardware recovery, LFB can reset NCU and MSCALER selfly, then restart selfly.	RW
1	disable_check_err	1=lfb don't care axi address error and just assert int when axi address error occurs, and it will transmit data normally. **Note**: This bit default value is 0，it don't need configure generally.	RW
0	lfb_enable	Lfb enable.	RW

3.9.4.2 LFB_RESTART Register(LFB_RESTART，0x204)

	LFB_RESTART																															LFB_BA+0x204
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															lfb_restart
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect. Read as zero.	R
0	lfb_restart	It should be set to 0 then set to1 when error occurs and lfb in software recovery mode.	RW

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3.9.4.3 LFB_HBLK_CFG Register(LFB_HBLK_CFG，0x208)

	LFB_HBLANK_CFG																															LFB_BA+0x208
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						uv_min_hblk_en	uv_min_hblk_num												y_min_hblk_en	y_min_hblk_num											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:26	Reserved	Writing has no effect. Read as zero.	R
25	uv_min_hblk_en	enable lfb uv channel output minimum blanking requestion.	RW
24:13	uv_min_hblk_num	lfb uv channel minimum blanking number.	RW
12	y_min_hblk_en	enable lfb y channel output minimum blanking requestion.	RW
11:0	y_min_hblk_num	lfb y channel minimum blanking number.	RW

3.9.4.4 LFB_Y_CFG Register(LFB_Y_CFG，0x210)

	LFB_Y_CFG																															LFB_BA+0x210
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													lfb_y_buf_num			lfb_y_stride															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	lfb_y_buf_num	The DMAOUT's y channel buffer number which is ISP output to LFB，set as real buffer number minus 1 .	RW
15:0	lfb_y_stride	The DMAOUT's y channel line stride which is ISP output to LFB.	RW

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3.9.4.5 LFB_Y_RES Register(LFB_Y_RES，0x214)

	LFB_Y_RES																															LFB_BA+0x214
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ver_res																hor_res															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	ver_res	The DMAOUT's y channel vertical resolution.	RW
15:0	hor_res	The DMAOUT's y channel horizontal resolution.	RW

3.9.4.6 LFB_Y_BUF0_ADDR Register(LFB_Y_BUF0_ADDR,0x218)

	LFB_Y_BUF0_ADDR																															LFB_BA+0x218
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_y_buf0_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	lfb_y_buf0_addr	The DMAOUT's y channel buffer0 address which is ISP output to LFB.	RW

3.9.4.7 LFB_Y_BUF1_ADDR Register(LFB_Y_BUF1_ADDR,0x21C)

	LFB_Y_BUF1_ADDR																															LFB_BA+0x21C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_y_buf1_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:0	lfb_y_buf1_addr	The DMAOUT's y channel buffer1 address which is ISP output to LFB.	RW

3.9.4.8 LFB_Y_BUF2_ADDR Register(LFB_Y_BUF2_ADDR,0x220)

	LFB_Y_BUF2_ADDR																															LFB_BA+0x220
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_y_buf2_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	lfb_y_buf2_addr	The DMAOUT's y channel buffer2 address which is ISP output to LFB.	RW

3.9.4.9 LFB_Y_BUF3_ADDR Register(LFB_Y_BUF3_ADDR,0x224)

	LFB_Y_BUF3_ADDR																															LFB_BA+0x224
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_y_buf3_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	lfb_y_buf3_addr	The DMAOUT's y channel buffer3 address which is ISP output to LFB.	RW

3.9.4.10 LFB_Y_BUF4_ADDR Register(LFB_Y_BUF4_ADDR,0x228)

	LFB_Y_BUF4_ADDR																															LFB_BA+0x228
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_y_buf1_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:0	lfb_y_buf4_addr	The DMAOUT's y channel buffer4 address which is ISP output to LFB.	RW

3.9.4.11 LFB_UV_CFG Register(LFB_UV_CFG，0x230)

	LFB_UV_CFG																															LFB_BA+0x230
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													lfb_uv_buf_num			lfb_uv_stride															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:19	Reserved	Writing has no effect, read as zero.	R
18：16	lfb_uv_buf_num	The DMAOUT's uv channel buffer number which is ISP output to LFB，set as real buffer number minus 1 .	RW
15:0	lfb_uv_stride	The DMAOUT's uv channel line stride which is ISP output to LFB.	RW

3.9.4.12 LFB_UV_RES Register(LFB_UV_RES，0x234)

	LFB_UV_RES																															LFB_BA+0x234
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ver_res																hor_res															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	ver_res	The DMAOUT's uv channel vertical resolution. It should be half of y channel resolution.	RW
15:0	hor_res	The DMAOUT's uv channel horizontal resolution. It should be half of y channel resolution.	RW

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3.9.4.13 LFB_UV_BUF0_ADDR Register(LFB_UV_BUF0_ADDR,0x238)

	LFB_UV_BUF0_ADDR																															LFB_BA+0x238
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_uv_buf0_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	lfb_uv_buf0_addr	The DMAOUT's uv channel buffer0 address which is ISP output to LFB.	RW

3.9.4.14 LFB_UV_BUF1_ADDR Register(LFB_UV_BUF1_ADDR,0x23C)

	LFB_UV_BUF1_ADDR																															LFB_BA+0x23C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_uv_buf1_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	fb_uv_buf1_addr	The DMAOUT's uv channel buffer1 address which is ISP output to LFB.	RW

3.9.4.15 LFB_UV_BUF2_ADDR Register(LFB_UV_BUF2_ADDR,0x240)

	LFB_UV_BUF2_ADDR																															LFB_BA+0x240
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_uv_buf2_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:0	lfb_uv_buf2_addr	The DMAOUT's uv channel buffer2 address which is ISP output to LFB.	RW

3.9.4.16 LFB_UV_BUF3_ADDR Register(LFB_UV_BUF3_ADDR,0x244)

	LFB_UV_BUF3_ADDR																															LFB_BA+0x244
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_uv_buf3_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	lfb_uv_buf3_addr	The DMAOUT's uv channel buffer3 address which is ISP output to LFB.	RW

3.9.4.17 LFB_UV_BUF4_ADDR Register(LFB_UV_BUF4_ADDR,0x248)

	LFB_UV_BUF4_ADDR																															LFB_BA+0x248
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	lfb_uv_buf4_addr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	lfb_uv_buf4_addr	The DMAOUT's uv channel buffer4 address which is ISP output to LFB.	RW

3.9.4.18 LFB_ERR Register(LFB_ERR,0x24C)

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	LFB_ERR																															LFB_BA+0x200
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																						isp_maout_uv_fifo_ovf	isp_maout_y_fifo_ovf	uv_frame_err	uv_line_err	uv_burst_err	uv_wlen_err	y_frame_err	y_line_err	y_burst_err	y_wlen_err
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:10	Reserved	Writing has no effect, read as zero.	R
9	isp_dmaout_uv _fifo_ovf	1=uv wfifo error occurs of ISP DMAOUT.	R
8	isp_dmaout_y_ fifo_ovf	1=y wfifo error occurs of ISP DMAOUT.	R
7	uv_frame_err	1=Frame address error occurs of ISP DMAOUT UV channel	R
6	uv_line_err	1=Line address error occurs of ISP DMAOUT UV channel	R
5	uv_burst_err	1=Burst address error occurs of ISP DMAOUT UV channel	R
4	uv_wlen_err	1=Wlen error occurs of ISP DMAOUT UV channel	R
3	y_frame_err	1=Frame address error occurs of ISP DMAOUT Y channel	R
2	y_line_err	1=Line address error occurs of ISP DMAOUT Y channel	R
1	y_burst_err	1=Burst address error occurs of ISP DMAOUT Y channel	R
0	y_wlen_err	1=Wlen error occurs of ISP DMAOUT Y channel	R

3.9.4.19 LFB_DEBUG0 Register(LFB_DEBUG0,0x260)

lfb_out debug0

	LFB_DEBUG0																															LFB_BA+0x260
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	y_line_cnt												y_pix_cnt												y_out_cs				Reserved			y_fifo_empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	y_line_cnt	Lfb y channel output line counter of current frame.	R
8:19	y_pix_cnt	Lfb y channel output pixel counter of current line.	R
4:7	y_out_cs	Lfb y channel FSM status.	R

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3:1	Reserved	Writing has no effect, read as zero.	R
0	y_fifo_empty	Y fifo empty status	R

3.9.4.20 LFB_DEBUG1 Register(LFB_DEBUG1,0x264)

lfb_out debug1

	LFB_DEBUG1																															LFB_BA+0x264
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	uv_line_cnt												uv_pix_cnt												uv_out_cs				Reserved			uv_fifo_empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	uv_line_cnt	Lfb uv channel output line counter of current frame.	R
8:19	uv_pix_cnt	Lfb uv channel output pixel counter of current line.	R
4:7	uv_out_cs	Lfb uv channel FSM status.	R
3:1	Reserved	Writing has no effect, read as zero.	R
0	uv_fifo_empty	UV fifo empty status	R

3.9.4.21 LFB_DEBUG2 Register(LFB_DEBUG2,0x268)

lfb_out debug2

	LFB_DEBUG2																															LFB_BA+0x268
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved			ncu_y_busy	Reserved			ncu_uv_busy	Reserved			msc_y_busy	Reserved			msc_uv_busy	Reserved			y_hsync	Reserved			y_hvalid	Reserved			uv_hsync	Reserved			uv_hvalid
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:29	Reserved	Writing has no effect, read as zero.	R
28	ncu_y_busy	ncu y channel busy	R
27:25	Reserved	Writing has no effect, read as zero.	R
24	ncu_uv_busy	ncu uv channel busy	R
23:21	Reserved	Writing has no effect, read as zero.	R
20	msc_y_busy	msc y channel busy	R
19:17	Reserved	Writing has no effect, read as zero.	R

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16	msc_uv_busy	msc uv channel busy	R
15:13	Reserved	Writing has no effect, read as zero.	R
12	y_hsync	y channel hsync	R
11:9	Reserved	Writing has no effect, read as zero.	R
8	y_hvalid	y channel hvalid	R
7:5	Reserved	Writing has no effect, read as zero.	R
4	uv_hsync	uv channel hsync	R
3:1	Reserved	Writing has no effect, read as zero.	R
0	uv_hvalid	uv channel hvalid	R

3.9.4.22 LFB_DEBUG3 Register(LFB_DEBUG3,0x26C)

lfb_out debug3

	LFB_DEBUG3																															LFB_BA+0x26C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	out_frame_cnt																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	out_frame_cnt	Lfb total output frame number. It will be cleared when lfb reset .	R

3.9.4.23 LFB_DEBUG4 Register(LFB_DEBUG4,0x270)

lfb_core_y debug0

	LFB_DEBUG4																															LFB_BA+0x270
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	y_fifo_empty				y_fifo_full				y_local_recov_end				y_ext_recov_end				y_soft_restart				y_hard_restart				msca_recov_ack				ncu_recov_ack			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:28	y_fifo_empty	y fifo empty	R
27:24	y_fifo_full	y fifo full	R
23:20	y_local_recov_end	y local recovery end	R

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19:16	y_ext_recov_end	y ext recovery end	R
15:12	y_soft_restart	y soft restart	R
11:8	y_hard_restart	y hard restart	R
7:4	msca_recov_ack	msclaer recovery ack	R
3:0	ncu_recov_ack	ncu recovery ack	R

3.9.4.24 LFB_DEBUG5 Register(LFB_DEBUG5,0x274)

lfb_core_y debug1

	LFB_DEBUG5																															LFB_BA+0x274
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	y_fsm_sta												y_frame_cnt				Reservecd				Exit_recov				Recov_req				Lfb_err			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	y_fsm_sta	y fsm status	R
19:16	y_frame_cnt	y frame counter	R
15:12	Reserved	reserved	R
11:8	exit_recov	exit recovery mode	R
7:4	recov_req	recovery request	R
3:0	lfb_err	lfb error	R

3.9.4.25 LFB_DEBUG6 Register(LFB_DEBUG6,0x278)

lfb_core_uv debug0

	LFB_DEBUG6																															LFB_BA+0x278
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	uv_fifo_empty				uv_fifo_full				uv_local_recov_end				uv_ext_recov_end				uv_soft_restart				uv_hard_restart				msca_recov_ack				ncu_recov_ack			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:28	uv_fifo_empty	UV fifo empty	R
27:24	uv_fifo_full	UV fifo full	R
23:20	uv_local_recov_end	UV local recovery end	R

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19:16	uv_ext_recov_end	UV ext recovery end	R
15:12	uv_soft_restart	UV soft restart	R
11:8	uv_hard_restart	UV hard restart	R
7:4	msclaer_recov_ack	Mscaler recovery ack	R
3:0	ncu_recov_ack	Ncu recovery ack	R

3.9.4.26 LFB_DEBUG7 Register(LFB_DEBUG7,0x27C)

lfb_core_uv debug1

	LFB_DEBUG7																LFB_BA+0x27C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	uv_fsm_sta												uv_frame_cnt				Reserved				exit_recov				recov_req				lfb_err			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	uv_fsm_sta	UV fsm status	R
19:16	uv_frame_cnt	UV frame counter	R
15:12	Reserved	Writing has no effect, read as zero.	R
11:8	exit_recov	Exit recovery mode	R
7:4	recov_req	Recovery request	R
3:0	lfb_err	Lfb error	R

3.9.5 IRQ Registers

Table 3-23 IRQ Registers Map

Name	RW	Reset Value	Address Offset	Access Size
IRQ_CNT0	R	0x0000_0000	0x00	32
IRQ_CNTC1	RW	0x0000_0000	0x04	32
IRQ_CNTCA	RW	0x0000_0000	0x08	32
IRQ_SRC	R	0x0000_0000	0x0c	32
IRQ_CNT_OVF	R	0x0000_0000	0x10	32
IRQ_EN	RW	0x0000_0000	0x14	32
IRQ_MASK	RW	0x0000_0000	0x1C	32
IRQ_CNT1	R	0x0000_0000	0x20	32
IRQ_CNT2	R	0x0000_0000	0x24	32
IRQ_CNT3	R	0x0000_0000	0x28	32

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3.9.5.1 IRQ Counter0 Register(IRQ_CNT0, 0x0)

The IRQ_CNT0 register is used for counting irq's number which has not been processed. When a irq occur, the irq's corresponding counter of IRQ_CNT0 will increase 1 if the irq enable. If response a irq, you should clear the corresponding counter. Write the corresponding bit of IRQ_CNTC1,the irq's counter will decrease 1. Write the corresponding bit of IRQ_CNTCA, the irq's counter will be 0. The register is readable only.

	IRQ_CNT0																IRQ_BA+0x0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	core_irq7				core_irq6				core_irq5				core_irq4				core_irq3				core_irq2				core_irq1				core_irq0			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:28	core_irq7	count the number of isp_core's irq7.	R
27:24	core_irq6	count the number of isp_core's irq6.	R
23:20	core_irq5	count the number of isp_core's irq5.	R
19:16	core_irq4	count the number of isp_core's irq4.	R
15:12	core_irq3	count the number of isp_core's irq3.	R
11:8	core_irq2	count the number of isp_core's irq2.	R
7:4	core_irq1	count the number of isp_core's irq1.	R
3:0	core_irq0	count the number of isp_core's irq0.	R

3.9.5.2 IRQ Counter Clear 1 Register(IRQ_CNTC1,0x4)

The IRQ_CNTC1 register is used for clearing counters of IRQ_CNTx's(x=0,1,2). Write any bit of IRQ_CNTC1,the corresponding counter of IRQ_CNTx(x=0,1,2) will decrease one. Write 0 has no effect. The register is writable and readable.

	IRQ_CNTC1																IRQ_BA+0x04															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved				dma_fifo_ovf	dma_frd	isp_fifo_ovf	lfb_err	lfb_frd	vic_hvf_err	vic_vres_err	vic_hres_err	vic_fifo_ovf	vic_frm_rst	vic_frm_start		vic_frd	core_irq15	core_irq14	core_irq13	core_irq12	core_irq11	core_irq10	core_irq9	core_irq8	core_irq7	core_irq6	core_irq5	core_irq4	core_irq3	core_irq2	core_irq1	core_irq0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value of Bit	Description
0	Write 0 has no effect.
1	Write 1,the corresponding irq's counter will decrease 1.

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3.9.5.3 IRQ Counter Clear All Register(IRQ_CNTCA,0x8)

The IRQ_CNTCA register is used for clearing counters of IRQ_CNTx's(x=0,1,2). Write any one bit of IRQ_CNTCA,the corresponding counter of IRQ_CNTx will be 0. Write 0 has no effect. The register is writable and readable.

	IRQ_CNTCA																															IRQ_BA+0x08
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved				dma_fifo_ovf	dma_frd	isp_fifo_ovf	lfb_err	lfb_frd	vic_hvf_err	vic_vres_err	vic_hres_err	vic_fifo_ovf	vic_frm_rst	vic_frm_start	vic_frd	core_irq15	core_irq14	core_irq13	core_irq12	core_irq11	core_irq10	core_irq9	core_irq8	core_irq7	core_irq6	core_irq5	core_irq4	core_irq3	core_irq2	core_irq1	core_irq0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value of Bit	Description
0	Write 0 has no effect.
1	Write 1 the corresponding irq's counter will be 0.

3.9.5.4 IRQ Source Register(IRQ_SRC ,0x0C)

The IRQ_SRC register is used for indicating the irq's source. If the irq enable, the corresponging bit of IRQ_SRC assert when a interrupt occur. If disable the irq, the IRQ_SRC will be always 0. The register is readable only.

	IRQ_SRC																															IRQ_BA+0x0C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved				dma_fifo_ovf	dma_frd	isp_fifo_ovf	lfb_err	lfb_frd	vic_hvf_err	vic_vres_err	vic_hres_err	vic_fifo_ovf	vic_frm_rst	vic_frm_start	vic_frd	core_irq15	core_irq14	core_irq13	core_irq12	core_irq11	core_irq10	core_irq9	core_irq8	core_irq7	core_irq6	core_irq5	core_irq4	core_irq3	core_irq2	core_irq1	core_irq0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:28	Reserved	Writing has no effect, read as zero.	R
27	dma_dvp_ovf	DMA's async fifo overflow error occurs.	R
26	dma_frd	DMA frame done	R
25	isp_fifo_ovf	ISP_core dma fifo empty fail or full fail occurs.	R
24	lfb_err	Error is checked in LFB.	R
23	lfb_frd	LFB finish one frame	R
22	vic_hvf_err	VIC BT656/1120 hvf error occurs.	R
21	vic_vres_err	VIC image vertical error，it indicates that the received line number	R

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		of one frame doesn't equal to vertical resolution).This bit is valid when input interface is DVP or MIPI CSI or switch mode.	
20	vic_hres_err	VIC image horizon error, it indicates that the received pixel number of one line doesn't equal to horizon resolution. This bit is valid when input interface is DVP or MIPI CSI or switch mode.	R
19	vic_fifo_ovf	VIC async FIFO overflow	R
18	vic_frm_rst	VIC frame reset	R
17	vic_frm_start	VIC frame start	R
16	vic_frd	VIC frame done	R
15	core_irq15	ISP_core's irq15	R
14	core_irq14	ISP_core's irq14	R
13	core_irq13	ISP_core's irq13	R
12	core_irq12	ISP_core's irq12	R
11	core_irq11	ISP_core's irq11	R
10	core_irq10	ISP_core's irq10	R
9	core_irq9	ISP_core's irq9	R
8	core_irq8	ISP_core's irq8	R
7	core_irq7	ISP_core's irq7	R
6	core_irq6	ISP_core's irq6	R
5	core_irq5	ISP_core's irq5	R
4	core_irq4	ISP_core's irq4	R
3	core_irq3	ISP_core's irq3	R
2	core_irq2	ISP_core's irq2	R
1	core_irq1	ISP_core's irq1	R
0	core_irq0	ISP_core's irq0	R

3.9.5.5 IRQ Counter Overflow Register(IRQ_CNT_OVF, 0x10)

The IRQ_CNT_OVF register is used for indicating whether the corresponding irq's counter overflow or not. If any bit of IRQ_CNT_OVF assert, it represents that the corresponding unprocessed irq's number has been more than 15.There is no effect when overflow occur, the register just used as a sign for software. The register is read only.

	IRQ_CNT_OVF																															IRQ_BA+0x10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved				dma_fifo_ovf	dma_frd	isp_fifo_ovf	lfb_err	lfb_frd	vic_hvf_err	vic_vres_err	vic_hres_err	vic_fifo_ovf	vic_frm_rst	vic_frm_start	vic_frd	core_irq15	core_irq14	core_irq13	core_irq12	core_irq11	core_irq10	core_irq9	core_irq8	core_irq7	core_irq6	core_irq5	core_irq4	core_irq3	core_irq2	core_irq1	core_irq0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Value of Bit	Description
0	The corresponding irq has no more than 15 unprocessed.
1	The corresponding irq has more than 15 unprocessed and the counter has overflow.

3.9.5.6 IRQ Enable Rregister(IRQ_EN,0x14)

The IRQ_EN register is used for enabling irq. Only if the corresponding IRQ_STAEN bit set to 1, the IRQ_SRC bit will assert when a irq occur. If disable a irq, the corresponding IRQ_SRC will be always 0.The register is readable and writable.

	IRQ_EN																															IRQ_BA+0x14
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved				dma_fifo_ovf	dma_frd	isp_fifo_ovf	lfb_err	lfb_frd	vic_hvf_err	vic_vres_err	vic_hres_err	vic_fifo_ovf	vic_frm_rst	vic_frm_start	vic_frd	core_irq15	core_irq14	core_irq13	core_irq12	core_irq11	core_irq10	core_irq9	core_irq8	core_irq7	core_irq6	core_irq5	core_irq4	core_irq3	core_irq2	core_irq1	core_irq0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value of Bit	Description
0	The corresponding irq source are disabled.
1	The corresponding irq source are enabled.

3.9.5.7 IRQ Mask Register(IRQ_MASK,0x1C)

The IRQ_MASK register is used for masking irqs. When any bit of the register is set to 1. the corresponding irq will not be seen by CPU.If a irq be output to CPU, the corresponding bit of IRQ_SRC must be 1 and the corresponding bit of IRQ_MSK must be 0. The register is readable and writable.

	IRQ_MASK																															IRQ_BA+0x1C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved				dma_fifo_ovf	dma_frd	isp_fifo_ovf	lfb_err	lfb_frd	vic_hvf_err	vic_vres_err	vic_hres_err	vic_fifo_ovf	vic_frm_rst	vic_frm_start	vic_frd	core_irq15	core_irq14	core_irq13	core_irq12	core_irq11	core_irq10	core_irq9	core_irq8	core_irq7	core_irq6	core_irq5	core_irq4	core_irq3	core_irq2	core_irq1	core_irq0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value of Bit	Description
0	The corresponding irq source are unmasked.
1	The corresponding irq source are masked. The irq source will not be see by CPU.

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3.9.5.8 IRQ Counter1 Register(IRQ_CNT1,0x20)

The IRQ_CNT1 register is used for counting irq's number which has not been processed. When a irq occur, the irq's corresponding counter of IRQ_CNT1 will increase 1 if the irq enable. When software response a irq, it should clear(or reduce 1) the corresponding counter. Write the corresponding bit of IRQ_CNTC1,the irq's counter will decrease 1. Write the corresponding bit of IRQ_CNTCA, the irq's counter will be 0. The register is readable only.

	IRQ_CNT1																IRQ_BA+0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Core_IRQ15				Core_IRQ14				Core_IRQ13				Core_IRQ12				Core_IRQ11				Core_IRQ10				Core_IRQ9				Core_IRQ8			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:28	Core_IRQ15	Count the number of isp_core's irq15.	RW
27:24	Core_IRQ14	Count the number of isp_core's irq14.	RW
23:20	Core_IRQ13	Count the number of isp_core's irq13.	RW
19:16	Core_IRQ12	Count the number of isp_core's irq12.	RW
15:12	Core_IRQ11	Count the number of isp_core's irq11.	RW
11:8	Core_IRQ10	Count the number of isp_core's irq10.	RW
7:4	Core_IRQ9	Count the number of isp_core's irq9.	RW
3:0	Core_IRQ8	Count the number of isp_core's irq8.	RW

3.9.5.9 IRQ Counter2 Register(IRQ_CNT2,0x24)

The IRQ_CNT2 register is used for counting irq's number which has not been processed. When a irq occur, the irq's corresponding counter of IRQ_CNT2 will increase 1 if the irq enable. When software response a irq, it should clear(or reduce 1) the corresponding counter. When write the corresponding bit of IRQ_CNTC1,the irq's counter will decrease 1. When write the corresponding bit of IRQ_CNTCA, the irq's counter will be 0. The register is readable only.

	IRQ_CNT2																IRQ_BA+0x24															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LFB_FRD				ISP_FIFO_OVF				VIC_HVF_ERR				VIC_VRES_ERR				VIC_HRES_ERR				VIC_MIPI_OVF				VIC_DVP_OVF				VIC_FRD			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:28	LFB_FRD	Count the number of LFB_FRD	RW
27:24	ISP_FIFO_OVF	Count the number of core fifo fail	RW
23:20	VIC_HVF_ERR	Count the number of bt hfv error	RW
19:16	VIC_VRES_ERR	Count the number of VIC_VRES_ERR	RW
15:12	VIC_HRES_ERR	Count the number of VIC_HRES_ERR	RW
11:8	VIC_MIPI_OVF	Count the number of VIC_MIPI_OVF	RW
7:4	VIC_DVP_OVF	Count the number of VIC_DVP_OVF	RW
3:0	VIC_FRD	Count the number of VIC_FRD	RW

3.9.5.10 IRQ Counter3 Register(IRQ_CNT3,0x28)

The IRQ_CNT3 register is used for counting irq's number which has not been processed. When a irq occur, the irq's corresponding counter of IRQ_CNT3 will increase 1 if the irq enable. When software response a irq, it should clear(or reduce 1) the corresponding counter. When write the corresponding bit of IRQ_CNTC1,the irq's counter will decrease 1. When write the corresponding bit of IRQ_CNTCA, the irq's counter will be 0. The register is readable only.

	IRQ_CNT3																															IRQ_BA+0x28
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																				DMA_FIFO_OVF				DMA_FRD				LFB_ERR			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	reserved	Writing has no effect, read as zero.	R
11:8	DMA _FIFO_OVF	Count the number of DMA _FIFO_OVF	R
7:4	DMA _FRD	Count the number of DMA _Y_FRD	R
3:0	LFB_ERR	Count the number of LFB_ERR	R

3.9.6 ISP Pipeline Registers

Table 3-24 ISP Pipeline Registers Map

Register Name	Module Name	Address Offset	
		Start	End
ISP	IP_CONFIG	0x00000	0x01FFF
FLASH_TIMER	FLASH_TIMER	0x02000	0x021FF
GAMMA_FE0_MEM	GAMMA_FE0_MEM	0x02800	0x028FF
GAMMA_FE1_MEM	GAMMA_FE1_MEM	0x03000	0x037FF

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RADIAL_SHADING_MEM	RADIAL_SHADING_MEM	0x03800	0x03BFF
SHADING_MEM	SHADING_MEM	0x04000	0x07FFF
METERING_MEM	METERING_MEM	0x08000	0x0BFFF
DEFECT_PIXEL_MEM	DEFECT_PIXEL_MEM	0x0C000	0x0FFFF
HISTOGRAM_MEM	HISTOGRAM_MEM	0x10000	0x103FF
FR_GAMMA_RGB_MEM	GAMMA_RGB_MEM	0x10400	0x107FF
FR_SHARPEN_MEM	SHARPEN_MEM	0x10800	0x10FFF
DS1_GAMMA_RGB_MEM	GAMMA_RGB_MEM	0x11000	0x113FF
DS1_SHARPEN_MEM	SHARPEN_MEM	0x11800	0x11FFF
DS2_GAMMA_RGB_MEM	GAMMA_RGB_MEM	0x12000	0x123FF
DS2_SHARPEN_MEM	SHARPEN_MEM	0x12800	0x12FFF
I_HFILT1_MEM	SCALER_HFILT_MEM	0x14000	0x14FFF
I_VFILT1_MEM	SCALER_VFILT_MEM	0x16000	0x16FFF
I_HFILT2_MEM	SCALER_HFILT_MEM	0x18000	0x18FFF
I_VFILT2_MEM	SCALER_VFILT_MEM	0x1A000	0x1AFFF

The following is ISP_Pipeline Top Control registers description. For more details, please contact with ingenic.

3.9.6.1 ISP_TOP Active Width(TOP_AW,0x10)

	TOP_AW																ISP_PIPELINE_BA+0x10															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Active Width															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	Active Width	Active video width in pixels	RW

3.9.6.2 ISP_TOP Active Height(TOP_AH,0x14)

	TOP_AH																ISP_PIPELINE_BA+0x14															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Active Height															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0

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Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	Active Height	Active video height in lines	RW

3.9.6.3 ISP_TOP RGGB(TOP_RGGB,0x18)

	TOP_RGGB																ISP_PIPELINE_BA+0x18															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														RGGB start	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect, read as zero.	R
1:0	RGGB start	Starting color of the rggb pattern 0 = R Gr 1 = Gr R Gb B B Gb 2 = Gb B 3 = B Gb R Gr Gr R	RW

3.9.6.4 ISP_TOP Flush Hblank(TOP_FSHBLK, 0x28)

	TOP_FSHBLK																ISP_PIPELINE_BA+0x28															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Flush hblank															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	Flush hblank	Horizontal blanking interval during regeneration (0=measured input interval)	RW

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3.9.6.5 ISP_TOP Buffer Mode(TOP_BFMODE,0x30)

	TOP_BFMODE																ISP_PIPELINE_BA+0x30															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														Config Buffer Mode	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect. Read as zero.	R
1:0	Config Buffer Mode	Select ISP configuration double-buffering mode 0 = Disabled (config updates immediately) 1 = Blocked (config never updates) 2 = Local (module config updates during local vertical blanking) 3 = Global (all module config updated during ISP vertical blanking)	RW

3.9.6.6 ISP_TOP Enable0(TOP_EN0,0x40)

	TOP_EN0																ISP_PIPELINE_BA+0x40															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	DS1 DMAsource	Bypass ds1 cs conv	Bypass ds1 logo	Bypass ds1 sharpen	Bypass ds1 gamma RGB	Bypass ds1 scaler	Bypass ds1 crop	Reserved	Bypass fr cs conv	Bypass fr logo	Bypass fr sharpen	Bypass fr gamma RGB	Bypass fr crop	Bypass color matrix	Bypass mosaic	Bypass iridix	Bypass mesh shading	Bypass radial shading	Bypass white balance	Order Sinter Temper	Bypass temper	Bypass sinter	Gamma fe position	Bypass frame stitch	Bypass defect pixel	Bypass RAW frontend	Bypass gamma fe	Bypass digital gain	Bypass sensor offset	Bypass mirror	Bypass video test gen
RST	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0	0	1	0

Bits	Name	Description	R/W
31	Reserved	Writing has no effect. Read as zero.	R
30	DS1 DMA source	Source for DS1 DMA data	RW

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		0 = Color space convertor 1 = Input	
29	Bypass ds1 cs conv	Bypass Colour Space Conversion (down scaled output 1)	RW
28	Bypass ds1 logo	Bypass Logo (down scaled output 1)	RW
27	Bypass ds1 sharpen	Bypass sharpen(down scaled output 1)	RW
26	Bypass ds1 gamma RGB	Bypass gamma table (down scaled output 1)	RW
25	Bypass ds1 scaler	Bypass Down Scaler 1	RW
24	Bypass ds1 crop	Bypass crop (down scaled output 1)	RW
23	Reserved	Writing has no effect, read as zero.	RW
22	Bypass fr cs conv	Bypass Colour Space Conversion (full resolution)	RW
21	Bypass fr logo	Bypass Logo (full resolution)	RW
20	Bypass fr sharpen	Bypass sharpen (full resolution)	RW
19	Bypass fr gamma RGB	Bypass gamma table (full resolution)	RW
18	Bypass fr crop	Bypass crop (full resolution)	RW
17	Bypass color matrix	Bypass color matrix	RW
16	Bypass demosaic	Bypass demosaic module (output RAW data)	RW
15	Bypass iridix	Bypass Iridix	RW
14	Bypass mesh shading	Bypass Mesh Shading	RW
13	Bypass radial shading	Bypass Radial Shading	RW
12	Bypass white balance	Bypass static white balance	RW
11	Order Sinter Temper	0 = sinter before temper 1 = sinter after temper	RW
10	Bypass temper	Bypass temper	RW
9	Bypass sinter	Bypass sinter	RW
8	Bypass frame stitch	Bypass frame stitching logic	RW
7	Bypass mirror	Bypass horizontal mirror	RW
6	Bypass defect pixel	Bypass static defect pixel	RW
5	Bypass RAW frontend	Bypass RAW frontend (green equalization and dynamic defect pixel)	RW
4	Bypass gamma fe	Bypass WDR companded frontend lookup table	RW
3	Bypass digital gain	Bypass digital gain module	RW
2	Bypass sensor offset	Bypass frontend black level adjustment	RW
1	Bypass mirror	Bypass horizontal mirror	RW
0	Bypass video test gen	Bypass video test generator	RW

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3.9.6.7 ISP_TOP Enbale1(TOP_EN1,0x44)

	TOP_EN1																ISP_PIPELINE_BA+0x44															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	ISP processing bypass mode		Reserved	ISP debug select		ISPRAWbypass	Reserved	Reserved	Bypass ds2cs conv	Bypass ds2 logo	Bypass ds2 sharpen	Bypass ds2 gamma RGB	Bypass ds2 scaler	Bypass ds2 crop	DS2 scaler source
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	R/W
31:15	Reserved	Writing has no effect. Read as zero.	R
14:13	ISP processing bypass mode	ISP bypass modes. For debug purposes only. Should be set to 0 during normal operation. Used to bypass entire ISP after input port. Data is sent to input of full resolution DMA Writer. 0 = Full processing 1= Bypass entire ISP processing and output most significant bits of raw sensor data in all channels 2 = Bypass entire ISP processing and output raw sensor data in channel 1 and most significant bits of channel 2 3 = Bypass entire ISP processing and output 8 bit RGB input as 10 bit RGB data	RW
12	Reserved	Writing has no effect. Read as zero.	R
11:10	ISP debug select	Debug port source select. 0 = Down scaled streamed video 1 1 = Down scaled streamed video 2 2 = Full resolution streamed video (after bypass mux) 3 = Input Video (into Input Port)	RW
9	ISP RAW bypass	Used to select between sensor raw input or RGB888 or YUV422 input 0 = Select processed. Normal ISP processing with image sensor raw data. 1 = Bypass ISP RAW processing for RGB888 or YUV422 inputs(Pass input RGB or YUV data to backend). Data is reinserted into pipeline after demosaic block. Crop,	RW

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		Scaling, Gamma and color space conversion are available for RGB888 input only.	
8:7	Reserved	Writing has no effect. Read as zero.	RW
6	Bypass ds2 cs conv	Bypass Color Space Conversion (down scaled output 2)	RW
5	Bypass ds2 logo	Bypass Logo (down scaled output 2)	RW
4	Bypass ds2 sharpen	Bypass sharpen (down scaled output 2)	RW
3	Bypass ds2 gamma RGB	Bypass gamma table (down scaled output 2)	RW
2	Bypass ds2 scaler	Bypass Down Scaler 2	RW
1	Bypass ds2 crop	Bypass crop (down scaled output 2)	RW
0	DS2 scaler source	Source selector for DS2 scaler 0 = Color matrix 1 = DS1 scaler output (chaining)	RW

3.9.6.8 ISP_TOP AE Switch(TOP_AES,0x48)

	TOP_AES																ISP_PIPELINE_BA+0x48															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													AE switch		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:3	Reserved	Writing has no effect. Read as zero.	R
2:0	AE switch	AE tap in the pipeline. Location of AE statistic collection. 0 = After static white balance 1 = After TPG 2 = After shading 3 = After frontend lookup table 4 = Long exposure 5 = Short exposure 6 = Before Temper 7 = Disabled	RW

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3.9.6.9 ISP_TOP AWB Switch(TOP_AWBS,0x4C)

	TOP_AWBS																ISP_PIPELINE_BA+0x4C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														AWB switch	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect. Read as zero.	R
1:0	AWB switch	AWB tap in the pipeline. Location of AWB statistics collection. 0 = Immediately before color matrix 1 = Immediately after color Matrix 2 = Disabled 3 = Disabled3	RW

3.9.6.10 ISP_TOP AF Switch(TOP_AFS,0x50)

	TOP_AFS																ISP_PIPELINE_BA+0x50															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														AF switch	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect. Read as zero.	R
1:0	AF switch	AF tap in the pipeline 0 = Demosaic 1 = Sharpen 2 = Disabled 3 = Disabled3	RW

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3.9.6.11 ISP_TOP MVE Switch(TOP_MVES,0x54)

	TOP_MVES																ISP_PIPELINE_BA+0x54															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														MVE switch	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect. Read as zero.	R
1:0	MVE switch	MVE tap in the pipeline. Location of DIS correlation value calculations 0 = End of pipeline 1 = Before Demosaic 2 = Before Defect pixel 3 = Disabled	RW

3.9.6.12 ISP_TOP Hist(TOP_HST,0x58)

	TOP_HST																ISP_PIPELINE_BA+0x58															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														Histogram switch	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:3	Reserved	Writing has no effect. Read as zero.	R
2:0	Histogram switch	AE global histogram tap in the pipeline. Location of statistics gathering for 256 bin global histogram 0 = Same as AE 1 = After TPG 2 = After shading	RW

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		3 = After frontend lookup table 4 = Long exposure 5 = Short exposure 6 = Before Temper 7 = Disabled	

3.9.6.13 ISP_TOP Field State(TOP_FLD_STA,0x7C)

	TOP_FLD_STA																ISP_PIPELINE_BA+0x7C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															Field
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:3	Reserved	Writing has no effect. Read as zero.	R
2:0	Field Status	Status of field signal	R

3.9.6.14 ISP_TOP Reset(TOP_RST,0x78)

	TOP_RST																ISP_PIPELINE_BA+0x78															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														VCKE override	Global FSM reset
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31：2	Reserved	Writing has no effect. Read as zero.	R
1	Global FSM reset	1= synchronous reset of FSMs in design (faster recovery after broken frame)	RW
0	VCKE override	1= override VCKE to flush the pipeline (recovery after broken frame)	RW

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3.10 Operation Flow

3.10.1 Overview

The system startup operation flow is described in Figure 3-7.

Figure 3-7 System startup Operation Flow

The startup steps are as follows:

1.Configure ISP Pipeline to star the working state.

2.Configure VIC.

3.Waiting VIC initialized completely. If it is finished, the VIC can be started.

4.Starting Sensor.

The system shut down operation flow is described in Figure 3-8.

Figure 3-8 System Shut Down Operation Flow

3.10.2 Configure VIC

3.10.2.1 Normal Mode

a) VIC_INPUT_INTF:

1) Select the input interface

2) If interface is mipi_csi, VIC_INPUT_MIPI should be configure,

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3) else if interface is dvp, VIC_INPUT_DVP should be configure,

b) VIC_INPUT_DVP: the following bit field should be configured
   1) vsyn_polar
   2) hsyn_polar
   3) dvp_timing_mode
   4) dvp_data_type
   5) dvp rgb orders（this bit need only configure when input data is rgb565/555）
   6) dvp_raw_alignment（this bit need only configure when input data is raw8/10/12）
   7) yuv_data_order（this bit need only configure when input data is yuv422）

c) VIC_INPUT_MIPI.

d) VIC_INPUT_HPARA0（this reg need configure when dvp is hsync or sony mode)

e) VIC_INPUT_VPARA3（this reg need configure when dvp is hsync or sony mode)
   1.when dvp hsync mode, configure VIC_INPUT_VPARA3[31:0], uint is pixel clock
   2.when dvp sony mode, configure VIC_INPUT_VPARA3[15:0], unit is line.

f) VIC_RESOLUTION（0x04)

g) VIC_OUTPUT_CFG(0x50).
   1) If you select the Blanking model, configure the Blanking value register.
   2) If you select the ab mode, configure the VIC_OUTPUT_ABVAL register(0x54).

h) Write VIC_CONTROL 0x02, then read it until be 0.

i) Write 0x01 to control register to start VIC,

3.10.2.2 Dual sensor Mode

a) VIC_SWITCH_MODE:

b) VIC_INPUT_DVP: the following bit field should be configured
   1) vsyn_polar
   2) hsyn_polar
   3) dvp_timing_mode
   4) dvp_data_type
   5) dvp rgb orders（this bit need only configure when input data is rgb565/555）
   6) dvp_raw_alignment（this bit need only configure when input data is raw8/10/12）
   7) yuv_data_order（this bit need only configure when input data is yuv422）

c) VIC_INPUT_MIPI.

d) VIC_INPUT_HPARA0（this reg need only configure when dvp is hsync mode)
   1) VIC_INPUT_VPARA0（this reg need only configure when dvp is hsync mode)

e) VIC_RESOLUTION（0x04)

f) VIC_OUTPUT_CFG(0x50).
   1) If you select the Blanking model, configure the Blanking value register.
   2) If you select the ab mode, configure the VIC_OUTPUT_ABVAL register(0x54).

g) Write VIC_CONTROL 0x02, then read it until be 0.

h) Write 0x01 to control register to start VIC,

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3.10.2.3 Back Color Bar Mode

Back Color bar is after VIC's asynchronize fifo，and support 8 color bars in one frame，each frame color can be configure。

a) configure bar's color value ,please refer tables as below.
b) configure back color bar blanking reg(0xB4);
c) configure back color bar control reg(0xB0);
d) configure control register to start VIC.

RAW(RGGB)	black	white	red	green	blue	yellow	purple	cyan
0xC0~0xDC	0x000000	0xFFFFFF	0x000FFF	0xFFF000	0x000000	0xFFFFFF	0x0007FF	0xFFF000
0xE0~0xFC	0x000000	0xFFFFFF	0x000000	0x000FFF	0xFFF000	0x000FFF	0x7FF000	0xFFFFFF

RGB888	black	white	red	green	blue	yellow	purple	cyan
0xC0~0xDC	0x000000	0xFFFFFF	0xFF0000	0x00FF00	0x0000FF	0xFFFF00	0x800080	0x00FFFF
0xE0~0xFC	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care

3.10.2.4 Front Color Bar Self Mode

Front Color bar is before asynchronize fifo，it supports raw8/10/12 or yuv422 format image, the pixel's value can be configure by VIC's 0xC0~0xFF。

a) configure VIC_FRT_CB_BLK(0xA4);
b) configure VIC_FRT_CB_CTRL(0xA0);
    1) if frame is always be transfered: frame_num=16'h8000
    else if frame is finite: frame_num="you want to transmit"
c) configure VIC_INPUT_DVP(0x10):
d) dvp_timing_mode=0,
e) dvp_data_type=0/1/2/3（RAW8/10/12,YUV422)
f) configure VIC_CONTROL to start VIC(0x00).

3.10.2.5 Front Color Bar Replace Mode

when at this mode, front color bar module use hsybc&vsync from sensor to generate raw8/10/12 or yuv422 format color bar image, the pixel's value can be configure by VIC's 0xC0~0xFF。

a) configure VIC_FRT_CB_BLK(0xA4);
b) configure VIC_ FRT_CB_CTRL (0xA0);
    a) if frame is always be transfered: frame_num=16'h8000
    else if frame is finite: frame_num="you want to transmit"'
    b) replace_data =1;
c) configure VIC_INPUT_DVP(0x10)：
        i. dvp_timing_mode=0，
        ii. dvp_data_type=0/1/2/3（RAW8/10/12,YUV422)
d) configure VIC_CONTROL to start VIC(0x00).

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3.10.3 Configure ISP Pipeline

Note: The ISP Pipeline controlled by Ingenic's firmware.

3.11 Index

Table 3-25 Description of Proprietary Vocabulary

Name	Description
3A	Auto focus, Auto exposure, Auto white balance
AXI	Advanced Extensible Interface
FS-WDR	Frame Stitch WDR
ISP	Image Signal Processor
LUT	Look Up Table
MSB	Most Significant Bit
VIC	Video Input Controller
WDR/HDR	Wide/High Dynamic Range

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4 Image Process Unit

4.1 Overview

Image Process Unit, which takes IPU as abbreviation, is used for image post processing. It contains image color space conversion(CSC), and 4 layers OSD functions.

4.2 Features

- AXI Bus for data transaction
- Input data format:
  - ARGB, RGB, NV12/NV21
- Output data format:
  - ARGB, RGB
  - NV12/NV21
  - HSV
- Color conversion feature: input and output format can be chosen freely from input and output data format.
- Minimum input image size (pixel): 4x4
- Maximum input image size (pixel): 2592x2048
- Minimum output image size (pixel): 4x4
- Maximum output image size (pixel): 2592x2048
- Background channel OSD function:
  - Support 4 layers OSD
  - Support whole background picture into OSD process and partial picture into OSD process
  - Support 12 port-duff OSD modes
  - Support 5 input format in background channel: ARGB8888, ARGB1555, RGB888, NV12, NV21. RGB can be in following sequence: RGB, RBG, BRG, BGR, GRB, GBR. Specifically, RGB888 format data occupy 4 bytes when stored in memory, RGB occupy three bytes, and the forth byte can be any value, as it will never be used in IPU.
  - Output picture format must be the same with the input picture format of separated background channel.

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4.3 Block Diagram

Figure 4-1 Block Diagram of IPU data flow

Figure 4-1 shows the block diagram of IPU data flow. There are 5 DAM in channels: 4 OSD DMA in channels and 1 OSD background DMA in channel. OSD background DMA in channel read data as background picture for OSD or CSC operation. 4 OSD DMA in channels are used to read data as overlapping pictures in OSD function, and can be enable freely depends on you need. The background DMA channel data can be output to or bypass OSD module to do CSC or NV/ARGB format conversion. Finally, the result data will be output to external memory through DMA out module. In OSD mode, CSC function can't be enable for color space conversion, as the output format must be the same with the background input picture format, after OSD operation, the data will pass through ARGB format module or NV format module in Figure 4-1.

4.4 Functional Description

IPU is the module which can support OSD and CSC function in high performance. At one time, at most 4 layers can be overlapped on background channel. Table 4-1 shows the main function points of IPU.

Table 4-1 IPU Main Function Points

Main Function	Input Format Support	Output Format Support	Output Destination
OSD	ARGB/RGB/NV12/NV21	ARGB/RGB/NV12/NV21	DDR
CSC	ARGB	ARGB/RGB/NV12/NV21/HSV	DDR
	RGB	ARGB/RGB/NV12/NV21/HSV	DDR

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	NV12	ARGB/RGB/NV12/NV21/HSV	DDR
	NV21	ARGB/RGB/NV12/NV21/HSV	DDR

4.4.1 Source picture and buffer

To the IPU, it needs to know where the picture stored and what format the picture is. People can use Data format register(0x08) to tell IPU what format it is.

Figure 4-2 Picture Parameters

Besides the format, the IPU has to know the address, where store the picture, through input Y Data or ARGB data Address(0xC), input UV Data Address (0x10). The address must be 64 Byte align. For one picture stored in memory, it also has some other feature, just like width, height, and stride. The width and height can be configured by the input geometric size register(0x18). And the stride will be configured by the input Y/ARGB data line stride(0x1C) and input UV data line stride(0x20). The relationship about the three actors is shown in the following Figure 4-2 .Figure 4-3 shows the NV data format parameters relationship.

Figure 4-3 NV Picture Parameters

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4.4.2 Color conversion

The IPU supports color conversion function. You can choose input format from ARGB, RGB, NV12, NV21 format, and output format support ARGB, RGB. NV12, NV21 and HSV format. The following conversion should set CSC parameters of channel 0(As CSC and OSD can not be enable at the same time, the CSC calculation module of channel 0 can be shared by background channel CSC operation for saving hardware cost):

- ARGB/RGB to NV21/NV21
- NV12/NV21 to ARGB/RGB
- NV12/NV21 to HSV

The commended values of this parameters will be described in the section of Channel 0 CSC registers.

4.4.3 Result picture and buffer

Just like the source picture and buffer, the result picture also has width, height and buffer stride.
As the picture size will not change, the output picture height, width, and stride will keep the same with input picture buffer.

Figure 4-4 Result Picture Parameters

4.4.4 Run the IPU

After people set the necessary register in IPU, it need to tell IPU which register has be re-configured. People can set the correspond bit in register configure enable control register (0x64) to tell IPU. If one register has no correspond bit in 0x64 register, it will act immediately when it has been changed.
After set the 0x64 register, people just need to write 1 to the IPU trigger register (0x74) to run the IPU. When value 1 has been write to 0x74, it will record it to record register first. Then IPU check the record register when it is free. If the record register is 1, IPU will start one new frame operation. The IPU will

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check the 0x64 register at the start time of each frame operation, clear the record register, and the 0x64 register.

4.4.5 IPU work finish and free

IPU gives the IPU status register (0x4) to let people know his inner status. If IPU has finish one frame, and it is on free, the MSTATUS bits in the IPU status register (0x4) will turn to 0. There are 2 case which will make IPU turn to free.

1. IPU finish one frame work and no new frame work again.
2. People stop the IPU and no new frame work again.

4.4.6 STOP, reset the IPU

If it needs the IPU stop as soon as possible, people need to stop , not reset IPU. Reset IPU may result some critical consequence. The stop bit in IPU trigger register (0x74) written to 1 will trigger the stop mechanism, and then people just needs wait IPU to turn to free.

The reset to IPU can be used only when IPU is free. All the register in IPU will be set to reset value when reset.

4.4.7 Interrupt

The IPU can trigger the interrupt to the system. People needs enable the interrupt by set the IRQ_EN bit of the IPU global control (0x7C) to 1. There is 1 case which will generate the interrupt.

1. IPU turn to free from the busy.

4.4.8 OSD function

IPU support at most 4 layers OSD function, the background picture come form OSD background channel in Figure 4-1, the input data type can be chosen from the following 4 types: ARGB, RGB, NV12, NV21. The output data type should be the same with input picture type.

When do the OSD operation, the following items should be paid attentions to:

1. The parameters of every channel can be set independently.
2. OSD can support whole background picture into OSD or only overlapped picture into OSD, if background picture comes form OSD background channel, the mode of overlapped picture into OSD will save bandwidth because only the overlapped picture are fetched by DMA.
3. 4 OSD channels can also support RGB to YUV and YUV to RGB conversion.
4. 4 OSD channels can support mask function, alpha choose function that you can choose alpha from pixel alpha, global alpha and (pixel alpha) * (global alpha).
5. If all of 4 OSD layer channels is disabled, then the separated background channel can be used as data moving function without changing data values.

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4.4.9 Read arbiter function

There are at most 5 DMA in channels running at the same time in IPU, a read arbiter is needed to make the read in sequence. This read arbiter is very simple, it has two mode: fixed priority mode and round-robin mode. you can set register 0x1A8 to set the mode and priority.

4.5 Pins Description

IPU has no IO pins.

4.6 Data Format Description

4.6.1 Input data flow

- Background channel input format: ARGB, RGB, NV12, NV21. RGB data can be grouped into 6 types: RGB, RBG, GRB, GBR, BRG, BGR. Picture data would be fetched from external memory by DMA burst read operation.
- 4 OSD channel input format: ARGB, RGB, NV12, NV21, RGB data can be grouped into 6 types: RGB, RBG, GRB, GBR, BRG, BGR. 4 OSD channel data would be fetched from external memory by DMA burst read operation.

4.6.2 Output data flow

- If IPU is used to do OSD function, the output data format must be the same with input data format. output data would be stored to the external memory by DMA burst write operation.
- If IPU is used to do CSC function, the output data format can be ARGB, RGB, NV12, NV21, HSV. output data would be stored to the external memory by DMA burst write operation.

4.6.3 ARGB/RGB format

Format	Stored sequence
ARGB	

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4.6.4 NV data format

NV12	Bit-31	23	16 15	8 7 0
	Y3	Y2	Y1	Y0
	Y data			
	Bit-31	23	16 15	8 7 0
	V1	U1	V0	U0
	UV data			
NV21	Bit-31	23	16 15	8 7 0
	Y3	Y2	Y1	Y0
	Y data			
	Bit-31	23	16 15	8 7 0
	U1	V1	U0	V0
	UV data			

4.6.5 HSV data format

HSV	Bit-31	23	16 15	8 7 0
	H1		H0	
	H data			
	Bit-31	23	16 15	8 7 0
	S3	S2	S1	S0
	S data			
	Bit-31	23	16 15	8 7 0
	V3	V2	V1	V0
	V data			

4.7 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   - R- Read only
   - W- Write only
   - RW- Read and Write
   - RCW- Read and Write, but Clear to 0 by Read
   - RSW- Read and Write, but Set to 1 by Read
   - RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   - RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   - RC- Read only, and Clear to 0 by read
   - RS- Read only, and Set to 1 by read
3. Reset Value

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1 - reset to 1
0 - reset to 0
? - value unknown after reset

4.7.1 Register Memory Map

Table 4-2 Registers Memory Map Base Address

Name	Base	Description
IPU	0x13080000	Address base of IPU

The IPU is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 4-3 IPU Registers Map

Name	RW	Reset Value	Address Offset	Access Size
IPU_FM_CONTROL	RW	0x0000_0001	0x0000	32
IPU_STATUS	RW	0x8001_0001	0x0004	32
D_FMT	RW	0x0000_0000	0x0008	32
Y_ADDR	RW	0x0000_0000	0x000C	32
U_ADDR	RW	0x0000_0000	0x0010	32
IN_FM_GS	RW	0x0000_0000	0x0018	32
Y_STRIDE	RW	0x0000_0000	0x001C	32
UV_STRIDE	RW	0x0000_0000	0x0020	32
OUT_ADDR	RW	0x0000_0000	0x0024	32
OUT_V_ADDR	RW	0x0000_0000	0x0030	32
OUT_V_STRIDE	RW	0x0000_0000	0x0034	32
IPU_REG_CTRL	RW	0x0000_0000	0x0064	32
IPU_TRIGGER	RW	0x0000_0000	0x0074	32
GLB_CTRL	RW	0x0000_0000	0x007C	32
NV_OUT_ADDR	RW	0x0000_0000	0x00B4	32
NV_OUT_STRIDE	RW	0x0000_0000	0x00B8	32
OSD_IN_CH0_Y_ADDR	RW	0x0000_0000	0x00BC	32
OSD_IN_CH0_Y_STRIDE	RW	0x0000_0000	0x00C0	32
OSD_IN_CH0_UV_ADDR	RW	0x0000_0000	0x00C4	32
OSD_IN_CH0_UV_STRIDE	RW	0x0000_0000	0x00C8	32
OSD_IN_CH1_Y_ADDR	RW	0x0000_0000	0x00CC	32
OSD_IN_CH1_Y_STRIDE	RW	0x0000_0000	0x00D0	32
OSD_IN_CH1_UV_ADDR	RW	0x0000_0000	0x00D4	32
OSD_IN_CH1_UV_STRIDE	RW	0x0000_0000	0x00D8	32
OSD_IN_CH2_Y_ADDR	RW	0x0000_0000	0x00DC	32
OSD_IN_CH2_Y_STRIDE	RW	0x0000_0000	0x00E0	32

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OSD_IN_CH2_UV_ADDR	RW	0x0000_0000	0x00E4	32
OSD_IN_CH2_UV_STRIDE	RW	0x0000_0000	0x00E8	32
OSD_IN_CH3_Y_ADDR	RW	0x0000_0000	0x00EC	32
OSD_IN_CH3_Y_STRIDE	RW	0x0000_0000	0x00F0	32
OSD_IN_CH3_UV_ADDR	RW	0x0000_0000	0x00F4	32
OSD_IN_CH3_UV_STRIDE	RW	0x0000_0000	0x00F8	32
OSD_CH0_GS	RW	0x0000_0000	0x00FC	32
OSD_CH1_GS	RW	0x0000_0000	0x0100	32
OSD_CH2_GS	RW	0x0000_0000	0x0104	32
OSD_CH3_GS	RW	0x0000_0000	0x0108	32
OSD_CH0_POS	RW	0x0000_0000	0x010C	32
OSD_CH1_POS	RW	0x0000_0000	0x0110	32
OSD_CH2_POS	RW	0x0000_0000	0x0114	32
OSD_CH3_POS	RW	0x0000_0000	0x0118	32
OSD_CH0_PARA	RW	0x0000_0000	0x011C	32
OSD_CH1_PARA	RW	0x0000_0000	0x0120	32
OSD_CH2_PARA	RW	0x0000_0000	0x0124	32
OSD_CH3_PARA	RW	0x0000_0000	0x0128	32
OSD_CH_BK_PARA	RW	0x0000_0000	0x012C	32
OSD_CH0_BAK_ARGB	RW	0x0000_0000	0x0130	32
OSD_CH1_BAK_ARGB	RW	0x0000_0000	0x0134	32
OSD_CH2_BAK_ARGB	RW	0x0000_0000	0x0138	32
OSD_CH3_BAK_ARGB	RW	0x0000_0000	0x013C	32
OSD_CH_B_BAK_ARGB	RW	0x0000_0000	0x0140	32
CH0_CSC_C0_COEF	RW	0x0000_0000	0x0148	32
CH0_CSC_C1_COEF	RW	0x0000_0000	0x014C	32
CH0_CSC_C2_COEF	RW	0x0000_0000	0x0150	32
CH0_CSC_C3_COEF	RW	0x0000_0000	0x0154	32
CH0_CSC_C4_COEF	RW	0x0000_0000	0x0158	32
CH0_CSC_OFSET_PARA	RW	0x0000_0000	0x015C	32
CH1_CSC_C0_COEF	RW	0x0000_0000	0x0160	32
CH1_CSC_C1_COEF	RW	0x0000_0000	0x0164	32
CH1_CSC_C2_COEF	RW	0x0000_0000	0x0168	32
CH1_CSC_C3_COEF	RW	0x0000_0000	0x016C	32
CH1_CSC_C4_COEF	RW	0x0000_0000	0x0170	32
CH1_CSC_OFSET_PARA	RW	0x0000_0000	0x0174	32
CH2_CSC_C0_COEF	RW	0x0000_0000	0x0178	32
CH2_CSC_C1_COEF	RW	0x0000_0000	0x017C	32
CH2_CSC_C2_COEF	RW	0x0000_0000	0x0180	32
CH2_CSC_C3_COEF	RW	0x0000_0000	0x0184	32
CH2_CSC_C4_COEF	RW	0x0000_0000	0x0188	32
CH2_CSC_OFSET_PARA	RW	0x0000_0000	0x018C	32

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CH3_CSC_C0_COEF	RW	0x0000_0000	0x0190	32
CH3_CSC_C1_COEF	RW	0x0000_0000	0x0194	32
CH3_CSC_C2_COEF	RW	0x0000_0000	0x0198	32
CH3_CSC_C3_COEF	RW	0x0000_0000	0x019C	32
CH3_CSC_C4_COEF	RW	0x0000_0000	0x01A0	32
CH3_CSC_OFSET_PARA	RW	0x0000_0000	0x01A4	32
RD_ARB_CTL	RW	0x0000_0000	0x01A8	32
CYC_NUM_ONE_FRA	R	0x0000_0000	0x01AC	32
OSD_LAY_PADDING_ARGB	RW	0x0000_0000	0x01B0	32
DEBUG_INFO_SIGNALS	R	0x0000_0000	0x01B4	32

4.7.2 Register and Fields Description

4.7.2.1 IPU Frame Control Register (IPU_FM_CONTROL, 0x0000)

	IPU_FM_CONTROL																															BASE + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															IPU_CHIP_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	IPU_CHIP_EN	IPU module enable flag. This bit will keep 1 after reset. Thus Writing to this bit has no effect, Read as constant value 0x1.	RW

4.7.2.2 IPU Status Register (IPU_STATUS, 0x0004)

The IPU_STATUS register includes the status of some IPU operations.

	IPU_STATUS																															BASE + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ID																Reserved										MSTATUS		Reserved	SIZE_ERR	Reserved	OUT_END
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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Bits	Name	Description	RW
31:16	ID	IPU version number. Writing has no effect. Read as 0x8001.	R
15:7	Reserved	Writing has no effect. Read as zero.	R
6:4	MSTATUS	IPU main status. 000: IPU is free Other value: IPU is running now	R
3	Reserved	Writing has no effect. Read as zero.	R
2	SIZE_ERR	Size error flag. 0: Size ok 1: Size error	R
1	Reserved	Writing has no effect. Read as zero.	R
0	OUT_END	Output termination flag. 0: output termination not finished 1: output termination finished	RW

NOTE:

1. If GLB_CTRL.IRQ_EN has been set 1, once OUT_END is set value 1 which denotes a frame's post process done, an low level active interrupt request will be issued until corresponding software handler read IPU_STATUS and clean end flag.

4.7.2.3 Date Format Register (D_FMT, 0x0008)

The D_FMT register is used to set the format of input and output data.

	D_FMT																															BASE + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									OUT_ARGB_OFT				OUT_FMT		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6:3	OUT_ARGB_OFT	argb type. 4'b0000: ARGB 4'b0001: ARBG 4'b0010: AGRB 4'b0011: AGBR 4'b0100: ABRG 4'b0101: ABGR	RW

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		4'b1000: RGBA 4'b1001: RBGA 4'b1010: GRBA 4'b1011: GBRA 4'b1100: BRGA 4'b1101: BGRA	
2:0	OUT_FMT	Pic type. 3'b000: ARGB 3'b001: RGB(per pixel occupy 4 byte in memory storage) 3'b010: NV12 3'b011: NV21 3'b100: HSV	RW

4.7.2.4 Input Y Data Address Register (Y_ADDR, 0x000C)

The Y_ADDR register is used to indicate the Y start data address in DRAM.

	Y_ADDR																															BASE + 0x000c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Y_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	Y_ADDR	1. In ARGB/RGB format, it indicates the ARGB/RGB data buffer's start address 2. In NV format, it indicates the start address of Y data. 3.Bit[1:0] are always 0	RW

NOTE:

1. Y_ADDR should be 64 bytes aligned.

4.7.2.5 Input U Data Address Register (U_ADDR, 0x0010)

The U_ADDR register is used to indicate the U start data address in DRAM.

	U_ADDR																															BASE + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	U_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	U_ADDR	1. It indicates the UV data buffer's start address in NV format. 2. Bit[1:0] are always 0	RW

NOTE:

1. U_ADDR should be 64 bytes aligned.

4.7.2.6 Input Geometric Size Register (IN_FM_GS, 0x0018)

The IN_FM_GS register is used to indicate the geometric size of input picture.

	IN_FM_GS																															BASE + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN_FM_W																IN_FM_H															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	IN_FM_W	The width of the input frame (unit: byte). In NV format, this value is equals to pixel number, however, in ARGB/RGB format, this value is four times of pixel number. i.e, it equals pixel number left shift 2 bits.	RW
15:0	IN_FM_H	The height of the input frame	RW

4.7.2.7 Input Y Data Line Stride Register (Y_STRIDE, 0x001C)

The Y_STRIDE register is used to indicate the line stride of Y source data.

	Y_STRIDE																															BASE + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								Y_STRIDE																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect. Read as zero.	R
23:0	Y_STRIDE	1. The line stride of the source Y data in the external memory (Unit: byte).	RW

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		2. Bit[1:0] are always 0	

NOTE:

1. Y_STRIDE should be 64 byte aligned.

4.7.2.8 Input UV Data Line Stride Register (UV_STRIDE, 0x0020)

The UV_STRIDE register is used to indicate the line stride of UV source data.

	UV_STRIDE																															BASE + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	U_STRIDE																Reserved															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	U_STRIDE	1. The line stride of the source U data in the external memory. 2. Bit[17:16] are always 0.	RW
15:0	Reserved	Writing has no effect. Read as zero.	RW

NOTE:

1. If in NV mode, U_STRIDE should set for UV data, the should be 64 bytes aligned.

4.7.2.9 Output Frame Start Address Register (OUT_ADDR, 0x0024)

The OUT_ADDR register is used to indicate the start address of output buffer in external memory..

	OUT_ADDR																															BASE + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OUT_ADDR	1. The output buffer's start address. 2. Bit[1:0] are always 0	RW

NOTE:

1. It should be 64 bytes aligned.
2. If in NV mode, this register is used to set Y start address.

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4.7.2.10 Output Data Line Stride Register (OUT_STRIDE, 0x002C)

The OUT_STRIDE register is used to indicate the line stride of output picture.

	OUT_STRIDE																															BASE + 0x002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OUT_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	OUT_STRIDE	1. The line stride of the destination data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0	RW

NOTE:

1. It should be 64 bytes align when separated background channel is enable.
2. In NV mode, this register is used to set Y stride.

4.7.2.11 Output V Start Address Register (OUT_V_ADDR, 0x0030)

The OUT_V_ADDR register is used to indicate the V data start address of output buffer in external memory.

	OUT_UV_ADDR																															BASE + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT_V_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OUT_V_ADDR	1. The output buffer's start address of V data in HSV data format. 2. Bit[1:0] are always 0	RW

NOTE:

1. It should be 64 bytes align.

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4.7.2.12 Output V Data Line Stride Register (OUT_V_STRIDE, 0x0034)

The OUT_V_STRIDE register is used to indicate the V data line stride of output picture.

	OUT_UV_STRIDE																															BASE + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OUT_V_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	OUT_V_STRIDE	1. The line stride of the V(HSV) destination data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0	RW

NOTE:

1. It should be 64 bytes aligned.

4.7.2.13 Register Configure Enable Control Register (IPU_REG_CTRL, 0x0064)

The IPU_REG_CTRL register is used to enable the registers you configure to work.

	IPU_REG_CTRL																															BASE + 0x0064
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				OSD_BK_RY	RD_ARB_RY	Reserved	OSD_CH3_RY	OSD_CH2_RY	OSD_CH1_RY	OSD_CH0_RY	NVD_STR_RY	NV_D_RY	OSD_RY	OFT_RY		Reserved			DSTR_RY	Reserved	CSTR_RY	YSTR_RY	IGS_RY	DF_RY	CTRL_RY	Reserved	Reserved	D_RY	V_RY	U_RY	Y_RY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect. Read as zero.	R
27	OSD_BK_RY	OSD background channel globa A, enable ready	RW
26	RD_ARB_RY	Read arbiter mode and priority ready	RW
25	Reserved	Writing has no effect. Read as zero.	RW
24	OSD_CH3_RY	OSD channel 3 addr, stride, width, height, pic_type, enable, xpos, ypos, globe A, ready	RW
23	OSD_CH2_RY	OSD channel 2 addr, stride, width, height, pic_type, enable, xpos, ypos, globe A, ready	RW
22	OSD_CH1_RY	OSD channel 1 addr, stride, width, height, pic_type, enable, xpos, ypos, globe A, ready	RW

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21	OSD_CH0_RY	OSD channel 0 addr, stride, width, height, pic_type, enable, xpos, ypos, globe A, ready	RW
20	NV_STR_RY	New destination NV frame stride ready.	RW
19	NV_D_RY	New destination NV frame start address ready	RW
18	NV_STR_RY	New destination V frame stride ready.	RW
17	NV_D_RY	New destination V frame start address ready	RW
16:13	Reserved	Writing has no effect. Read as zero.	R
12	DSTR_RY	New destination stride (OUT_STRIDE) ready.	RW
11	Reserved	Writing has no effect. Read as zero.	RW
10	CSTR_RY	New UV stride (UV_STRIDE) ready	RW
9	YSTR_RY	New Y stride (Y_STRIDE) ready	RW
8	IGS_RY	New input geometric size (IN_FM_GS) ready.	RW
7	DF_RY	New output data format (OUT_D_FMT) ready.	RW
6	CTRL_RY	New frame control (IPU_FM_CONTROL) ready	RW
5	Reserved	Writing has no effect. Read as zero.	RW
4	Reserved	Writing has no effect. Read as zero.	RW
3	D_RY	New destination address ready.	RW
2	V_RY	New source V address ready.	RW
1	U_RY	New source U address ready.	RW
0	Y_RY	New source Y address ready.	RW

NOTE:

1. When the xx_RY bit has been set 1, the IPU will use the new corresponding register in the next frame, and use the old address value whose corresponding bit in **IPU_REG_CTRL** is 0.

4.7.2.14 IPU trigger Register (IPU_TRIGGER, 0x0074)

The IPU_TRIGGER register is control the run/stop status of IPU.

	IPU_TRIGGER																															BASE + 0x0074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							DEBUG_SEL			Reserved		RESET	Reserved	STOP	RUN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:9	Reserved	Writing has no effect.	R

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		Read as zero.	
8:6	DEBUG_SEL	Choose debug signals from IPU, the debug signals should read from register 0x1b4	RW
5:4	Reserved	Writing has no effect. Read as zero.	R
3	RESET	reset	W
2	Reserved	Writing has no effect. Read as zero.	R
1	STOP	Stop ipu, ipu will stop immediately in safe	W
0	RUN	New fame configurable need run.	RW

4.7.2.15 IPU Global Control Register (GLB_CTRL, 0x007C)

The GLB_CTRL register is used to configure global signals of IPU, such as IRQ enable, etc

	GLB_CTRL																															BASE + 0x007C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															IRQ_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	IRQ_EN	Interrupt enable 0: disable 1: enable	R/W

4.7.2.16 Output UV Frame Start Address Register (NV_OUT_ADDR, 0x00B4)

The NV_OUT_ADDR register is used to set UV start address.

	NV_OUT_ADDR																															BASE + 0x00B4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NV_OUT_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	NV_OUT_ ADDR	1. The NV output buffer's start address. 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be 64 bytes aligned.
2. NV_OUT_ADDR only used in the case that the output format is NV12 or NV21.

4.7.2.17 NV Output Data Line Stride Register (NV_OUT_STRIDE, 0x00B8)

The NV_OUT_STRIDE register is used to set the line stride for NV output format.

	NV_OUT_STRIDE																															BASE + 0x00B8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																NV_OUT_S															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	NV_OUT_S	1. The line stride of the destination NV data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be 64 bytes aligned.
2. The NV_OUT_STRIDE is only used in the case that the output format is NV12 or NV21.

4.7.2.18 OSD Dma In Channel 0 Y Frame Start Address Register (OSD_IN_CH0_Y_ADDR, 0x00BC)

The OSD_IN_CH0_Y_ADDR register is used to set Y start address for OSD channel 0.

	OSD_IN_CH0_Y_ADDR																															BASE + 0x00BC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_IN_CH0_Y_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	OSD_IN_CH0_Y_ADDR	1. OSD channel 0 Y start address 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be dual-word align in ARGB, RGB, or NV mode.
2. If in ARGB/RGB mode, this register is used to set ARGB/RGB start address

4.7.2.19 OSD Dma In Channel 0 Y Line Stride Register (OSD_IN_CH0_Y_STRIDE, 0x00C0)

The OSD_IN_CH0_Y_STRIDE register is used to set Y line stride for OSD channel 0.

	OSD_IN_CH0_Y_STRIDE																															BASE + 0x00C0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSD_IN_CH0_Y_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	OSD_IN_CH0_Y_STRIDE	1. The Y line stride of the OSD dma in channel 0 data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be dual-word align in ARGB, RGB, or NV mode.
2. If in ARGB/RGB mode, this register is used to set ARGB/RGB stride

4.7.2.20 OSD Dma In Channel 0 UV Frame Start Address Register (OSD_IN_CH0_UV_ADDR, 0x00C4)

The OSD_IN_CH0_UV_ADDR register is used to set UV start address for OSD channel 0.

	OSD_IN_CH0_UV_ADDR																															BASE + 0x00C4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_IN_CH0_UV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	OSD_IN_CH0_UV_ADDR	1. OSD channel 0 UV start address 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be dual-word align.

4.7.2.21 OSD Dma In Channel 0 UV Line Stride Register (OSD_IN_CH0_UV_STRIDE, 0x00C8)

The OSD_IN_CH0_UV_STRIDE register is used to set UV line stride for OSD channel 0.

	OSD_IN_CH0_UV_STRIDE																															BASE + 0x00C8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSD_IN_CH0_UV_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	OSD_IN_CH0_UV_STRIDE	1. The UV line stride of the OSD dma in channel 0 data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be dual-word align.

4.7.2.22 OSD Dma In Channel 1 Y Frame Start Address Register (OSD_IN_CH1_Y_ADDR, 0x00CC)

The OSD_IN_CH1_Y_ADDR register is used to set Y start address for OSD channel 1.

	OSD_IN_CH1_Y_ADDR																															BASE + 0x00CC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_IN_CH1_Y_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_IN_CH1_Y_ADDR	1. OSD channel 1 Y start address.	RW

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		2. Bit[1:0] are always 0.	

NOTE:

1. It should be dual-word align in ARGB, RGB, or NV mode.
2. If in ARGB/RGB mode, this register is used to set ARGB/RGB start address

4.7.2.23 OSD Dma In Channel 1 Y Line Stride Register (OSD_IN_CH1_Y_STRIDE, 0x00D0)

The OSD_IN_CH1_Y_STRIDE register is used to set Y line stride for OSD channel 1.

	OSD_IN_CH1_Y_STRIDE																															BASE + 0x00D0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSD_IN_CH1_Y_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	OSD_IN_CH1_Y_STRIDE	1. The Y line stride of the OSD dma in channel 1 data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be dual-word align in ARGB, RGB, or NV mode.
2. If in ARGB/RGB mode, this register is used to set ARGB/RGB stride

4.7.2.24 OSD Dma In Channel 1 UV Frame Start Address Register (OSD_IN_CH1_UV_ADDR, 0x00D4)

The OSD_IN_CH1_UV_ADDR register is used to set UV start address for OSD channel 1.

	OSD_IN_CH1_UV_ADDR																															BASE + 0x00D4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_IN_CH1_UV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_IN_CH1_UV_ADDR	1. OSD channel 1 UV start address.	RW

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		2. Bit[1:0] are always 0.	

NOTE:

1. It should be dual-word align.

4.7.2.25 OSD Dma In Channel 1 UV Line Stride Register (OSD_IN_CH1_UV_STRIDE, 0x00D8)

The OSD_IN_CH1_UV_STRIDE register is used to set UV line stride for OSD channel 1.

	OSD_IN_CH1_UV_STRIDE																															BASE + 0x00D8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSD_IN_CH1_UV_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	OSD_IN_CH1_UV_STRIDE	1. The UV line stride of the OSD dma in channel 1 data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0.	RW

NOTE:

- It should be dual-word align.

4.7.2.26 OSD Dma In Channel 2 Y Frame Start Address Register (OSD_IN_CH2_Y_ADDR, 0x00BC)

The OSD_IN_CH2_Y_ADDR register is used to set Y start address for OSD channel 2.

	OSD_IN_CH2_Y_ADDR																															BASE + 0x00DC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_IN_CH2_Y_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_IN_CH2_Y_ADDR	1. OSD channel 2 Y start address. 2. Bit[1:0] are always 0.	RW

NOTE:

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1. It should be dual-word align in ARGB, RGB, or NV mode.
2. If in ARGB/RGB mode, this register is used to set ARGB/RGB start address

4.7.2.27 OSD Dma In Channel 2 Y Line Stride Register (OSD_IN_CH2_Y_STRIDE, 0x00E0)

The OSD_IN_CH2_Y_STRIDE register is used to set Y line stride for OSD channel 2.

	OSD_IN_CH2_Y_STRIDE																															BASE + 0x00E0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSD_IN_CH2_Y_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	OSD_IN_CH2_Y_STRIDE	1. The Y line stride of the OSD dma in channel 2 data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be dual-word align in ARGB, RGB, or NV mode.
2. If in ARGB/RGB mode, this register is used to set ARGB/RGB stride

4.7.2.28 OSD Dma In Channel 2 UV Frame Start Address Register (OSD_IN_CH2_UV_ADDR, 0x00E4)

The OSD_IN_CH2_UV_ADDR register is used to set UV start address for OSD channel 2.

	OSD_IN_CH2_UV_ADDR																															BASE + 0x00E4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_IN_CH2_UV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_IN_CH2_UV_ADDR	1. OSD channel 2 UV start address. 2. Bit[1:0] are always 0.	RW

NOTE:

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1. It should be dual-word align.

4.7.2.29 OSD Dma In Channel 2 UV Line Stride Register (OSD_IN_CH2_UV_STRIDE, 0x00E8)

The OSD_IN_CH2_UV_STRIDE register is used to set UV line stride for OSD channel 2.

	OSD_IN_CH2_UV_STRIDE																															BASE + 0x00E8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSD_IN_CH2_UV_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	OSD_IN_CH2_UV_STRIDE	1. The UV line stride of the OSD dma in channel 2 data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be dual-word align.

4.7.2.30 OSD Dma In Channel 3 Y Frame Start Address Register (OSD_IN_CH3_Y_ADDR, 0x00EC)

The OSD_IN_CH3_Y_ADDR register is used to set Y start address for OSD channel 3.

	OSD_IN_CH3_Y_ADDR																															BASE + 0x00EC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_IN_CH3_Y_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_IN_CH3_Y_ADDR	1. OSD channel 3 Y start address. 2. Bit[1:0] are always 0.	RW

NOTE:

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1. It should be dual-word align in ARGB, RGB, or NV mode.
2. If in ARGB/RGB mode, this register is used to set ARGB/RGB start address

4.7.2.31 OSD Dma In Channel 3 Y Line Stride Register (OSD_IN_CH3_Y_STRIDE, 0x00F0)

The OSD_IN_CH3_Y_STRIDE register is used to set Y line stride for OSD channel 3.

	OSD_IN_CH3_Y_STRIDE																															BASE + 0x00F0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSD_IN_CH3_Y_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	OSD_IN_CH3_Y_STRIDE	1. The Y line stride of the OSD dma in channel 3 data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be dual-word align in ARGB, RGB, or NV mode.
2. If in ARGB/RGB mode, this register is used to set ARGB/RGB stride

4.7.2.32 OSD Dma In Channel 3 UV Frame Start Address Register (OSD_IN_CH3_UV_ADDR, 0x00F4)

The OSD_IN_CH3_UV_ADDR register is used to set UV start address for OSD channel 3.

	OSD_IN_CH3_UV_ADDR																															BASE + 0x00F4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_IN_CH3_UV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_IN_CH3_UV_ADDR	1. OSD channel 3 UV start address. 2. Bit[1:0] are always 0.	RW

NOTE:

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1. It should be dual-word align.

4.7.2.33 OSD Dma In Channel 3 UV Line Stride Register (OSD_IN_CH3_UV_STRIDE, 0x00F8)

The OSD_IN_CH3_UV_STRIDE register is used to set UV line stride for OSD channel 3.

	OSD_IN_CH3_UV_STRIDE																															BASE + 0x00F8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSD_IN_CH3_UV_STRIDE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	OSD_IN_CH3_UV_STRIDE	1. The UV line stride of the OSD dma in channel 3 data buffer in the external memory(Unit: byte). 2. Bit[1:0] are always 0.	RW

NOTE:

1. It should be dual-word align.

4.7.2.34 OSD Dma In Channel 0 Gemetric Size Register (OSD_CH0_GS, 0x00FC)

The OSD_CH0_GS register is used to indicate the geometric size of channel 0 picture.

	OSD_CH0_GS																															BASE + 0x00FC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH0_FM_W																Reserved			OSD_CH0_FM_H												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	OSD_CH0_FM_W	The width of the OSD in channel 0 frame (unit: byte).	RW
15:13	Reserved	Writing has no effect. Read as zero.	R

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12:0	OSD_CH0_FM_H	The height of the OSD in channel 0 frame (unit: byte).	RW

NOTE:

1. If NV mode, OSD_CH0_FM_W is pixel number in a line.
2. If ARGB/RGB mode, OSD_CH0_FM_W is pixel_number * 4.
3. The size of channel 0 picture must be smaller than the size of background picture.

4.7.2.35 OSD Dma In Channel 1 Gemetric Size Register (OSD_CH1_GS, 0x00100)

The OSD_CH1_GS register is used to indicate the geometric size of channel 1 picture.

	OSD_CH1_GS																															BASE + 0x0100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH1_FM_W																Reserved			OSD_CH1_FM_H												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	OSD_CH1_FM_W	The width of the OSD in channel 1 frame (unit: byte).	RW
15:13	Reserved	Writing has no effect. Read as zero.	R
12:0	OSD_CH1_FM_H	The height of the OSD in channel 1 frame (unit: byte).	RW

NOTE:

1. If NV mode, OSD_CH1_FM_W is pixel number in a line.
2. If ARGB/RGB mode, OSD_CH1_FM_W is pixel_number * 4.
3. The size of channel 1 picture must be smaller than the size of background picture.

4.7.2.36 OSD Dma In Channel 2 Gemetric Size Register (OSD_CH2_GS, 0x00104)

The OSD_CH2_GS register is used to indicate the geometric size of channel 2 picture.

	OSD_CH2_GS																															BASE + 0x0104
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH2_FM_W																Reserved			OSD_CH2_FM_H												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	OSD_CH2_FM_W	The width of the OSD in channel 2 frame (unit: byte).	RW

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15:13	Reserved	Writing has no effect. Read as zero.	R
12:0	OSD_CH2_FM_H	The height of the OSD in channel 2 frame (unit: byte).	RW

NOTE:

1. If NV mode, OSD_CH2_FM_W is pixel number in a line.
2. If ARGB/RGB mode, OSD_CH2_FM_W is pixel_number * 4.
3. The size of channel 2 picture must be smaller than the size of background picture.

4.7.2.37 OSD Dma In Channel 3 Gemetric Size Register (OSD_CH3_GS, 0x0108)

The OSD_CH3_GS register is used to indicate the geometric size of channel 0 picture.

	OSD_CH3_GS																															BASE + 0x0108
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH3_FM_W																Reserved			OSD_CH3_FM_H												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	OSD_CH3_FM_W	The width of the OSD in channel 3 frame (unit: byte).	RW
15:13	Reserved	Writing has no effect. Read as zero.	R
12:0	OSD_CH3_FM_H	The height of the OSD in channel 3 frame (unit: byte).	RW

NOTE:

1. If NV mode, OSD_CH3_FM_W is pixel number in a line.
2. If ARGB/RGB mode, OSD_CH3_FM_W is pixel_number * 4.
3. The size of channel 3 picture must be smaller than the size of background picture.

4.7.2.38 OSD Dma In Channel 0 Position Register (OSD_CH0_POS, 0x010C)

The OSD_CH0_POS register is used to indicate the OSD position in background for channel 0 picture.

	OSD_CH0_POS																															BASE + 0x010C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH0_XPOS																Reserved			OSD_CH0_YPOS												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:16	OSD_CH0_XPOS	The x start position of channel 0 picture on background (unit: pixel).	RW
15:13	Reserved	Writing has no effect. Read as zero.	R
12:0	OSD_CH0_YPOS	The y start position of channel 0 picture on background (unit: pixel).	RW

4.7.2.39 OSD Dma In Channel 1 Position Register (OSD_CH1_POS, 0x0110)

The OSD_CH1_POS register is used to indicate the OSD position in background for channel 1 picture.

	OSD_CH1_POS																															BASE + 0x0110
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH1_XPOS																Reserved			OSD_CH1_YPOS												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	OSD_CH1_XPOS	The x start position of channel 1 picture on background (unit: pixel).	RW
15:13	Reserved	Writing has no effect. Read as zero.	R
12:0	OSD_CH1_YPOS	The y start position of channel 1 picture on background (unit: pixel).	RW

4.7.2.40 OSD Dma In Channel 2 Position Register (OSD_CH2_POS, 0x0114)

The OSD_CH2_POS register is used to indicate the OSD position in background for channel 2 picture.

	OSD_CH2_POS																															BASE + 0x0114
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH2_XPOS																Reserved			OSD_CH2_YPOS												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	OSD_CH2_XPOS	The x start position of channel 2 picture on background (unit:	RW

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		pixel).	
15:13	Reserved	Writing has no effect. Read as zero.	R
12:0	OSD_CH2_YPOS	The y start position of channel 2 picture on background (unit: pixel).	RW

4.7.2.41 OSD Dma In Channel 3 Position Register (OSD_CH3_POS, 0x0118)

The OSD_CH3_POS register is used to indicate the OSD position in background for channel 3 picture.

	OSD_CH3_POS																															BASE + 0x0118
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH3_XPOS																Reserved			OSD_CH3_YPOS												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	OSD_CH3_XPOS	The x start position of channel 3 picture on background (unit: pixel).	RW
15:13	Reserved	Writing has no effect. Read as zero.	R
12:0	OSD_CH3_YPOS	The y start position of channel 3 picture on background (unit: pixel).	RW

4.7.2.42 OSD Dma In Channel 0 Parameters Register (OSD_CH0_PARA, 0x011C)

The OSD_CH0_PARA register is used to set controls signals for Channel 0 OSD function.

	OSD_CH0_PARA																															BASE + 0x011C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CH0_CSC_CTL		CH0_MASK_EN	CH0_OSDM				CH0_PREM	CH0_ARGB_TYPE				CH0_PIC_TYPE			CH0_GLO_A								CH0_ALPHA_SEL		CH0_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect. Read as zero.	R

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25:24	CH0_CSC_CTL	Channel 0 color space conversion control. 2'b00: no color conversion 2'b01: YUV to RGB conversion 2'b10: RGB to YUV conversion	RW
23	CH0_MASK_EN	Channel 0 mask enable. If this bit is set to 1, the pixel values of this channel will always be the value in OSD_CH0_BAK_ARGB 0: Mask disable. 1: Mask enable	RW
22:19	CH0_OSDM	Channel 0 OSD mode. 4'd0: source over 4'd1: src 4'd2: dst 4'd3: clear 4'd4: dst over 4'd5: src in 4'd6: dst in 4'd7: src out 4'd8: dst out 4'd9: src at top 4'd10: dst at top 4'd11: XOR	RW
18	CH0_PREM	Channel 0 OSD pre multiplier. If this bit is set to 0, then the pixel values for OSD calculation is: OSD_R = Alpha x R OSD_G = Alpha x G OSD_B = Alpha x B If this bit is set to 1, the pixel values for OSD calculation will not change. 0: not pre multiplier 1: pre multiplied	RW
17:14	CH0_ARGB_TYPE	Channel 0 ARGB type. 4'b0000: ARGB 4'b0001: ARBG 4'b0010: AGRB 4'b0011: AGBR 4'b0100: ABRG 4'b0101: ABGR 4'b1000: RGBA 4'b1001: RBGA 4'b1010: GRBA 4'b1011: GBRA 4'b1100: BRGA 4'b1101: BGRA	RW
13:11	CH0_PIC_TYPE	Pic type. 3'b000: ARGB 3'b001: RGB(per pixel occupy 4 byte in memory storage) 3'b010: NV12 3'b011: NV21 3'b100: RGBA1555(the sequence of RGB is determined by CH0_ARGB_TYPE)	RW
10:3	CH0_GLO_A	Channel 0 global value	RW
2:1	CH0_ALPHA_SEL	Channel 0 alpha sel. 2'b00: pixel alpha 2'b01: global alpha	RW

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		2'b10: pixel alpha x (global alpha/256)	
0	CH0_EN	Channel 0 dma enable 0: disable 1: enable	RW

4.7.2.43 OSD Dma In Channel 1 Parameters Register (OSD_CH1_PARA, 0x0120)

The OSD_CH1_PARA register is used to set controls signals for Channel 1 OSD function.

	OSD_CH1_PARA																															BASE + 0x0120
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CH1_CSC_CTL		CH1_MASK_EN	CH1_OSDM				CH1_PREM	CH1_ARGB_TYPE				CH1_PIC_TYPE			CH1_GLO_A								CH1_ALPHA_SEL		CH1_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect. Read as zero.	R
25:24	CH1_CSC_CTL	Channel 1 color space conversion control. 2'b00: no color conversion 2'b01: YUV to RGB conversion 2'b10: RGB to YUV conversion	RW
23	CH1_MASK_EN	Channel 1 mask enable If this bit is set to 1, the pixel values of this channel will always be the value in OSD_CH1_BAK_ARGB 0: Mask disable 1: Mask enable	RW
22:19	CH1_OSDM	Channel 1 OSD mode. 4'd0: source over 4'd1: src 4'd2: dst 4'd3: clear 4'd4: dst over 4'd5: src in 4'd6: dst in 4'd7: src out 4'd8: dst out 4'd9: src at top 4'd10: dst at top 4'd11: XOR	RW
18	CH1_PREM	Channel 1 OSD pre multiplier. If this bit is set to 0, then the pixel values for OSD calculation is: OSD_R = Alpha x R OSD_G = Alpha x G OSD_B = Alpha x B If this bit is set to 1, the pixel values for OSD calculation will not	RW

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		change. 0: not pre multiplier 1: pre multiplied	
17:14	CH1_ARGB_TYPE	Channel 1 ARGB type. 4'b0000: ARGB 4'b0001: ARBG 4'b0010: AGRB 4'b0011: AGBR 4'b0100: ABRG 4'b0101: ABGR 4'b1000: RGBA 4'b1001: RBGA 4'b1010: GRBA 4'b1011: GBRA 4'b1100: BRGA 4'b1101: BGRA	RW
13:11	CH1_PIC_TYPE	Pic type. 3'b000: ARGB 3'b001: RGB(per pixel occupy 4 byte in memory storage) 3'b010: NV12 3'b011: NV21 3'b100: RGBA1555(the sequence of RGB is determined by CH1_ARGB_TYPE)	RW
10:3	CH1_GLO_A	Channel 1 global value	RW
2:1	CH1_ALPHA_SEL	Channel 1 alpha sel. 2'b00: pixel alpha 2'b01: global alpha 2'b10: pixel alpha x (global alpha/256)	RW
0	CH1_EN	Channel 1 dma enable 0: disable 1: enable	RW

4.7.2.44 OSD Dma In Channel 2 Parameters Register (OSD_CH2_PARA, 0x0124)

The OSD_CH2_PARA register is used to set controls signals for Channel 2 OSD function.

	OSD_CH2_PARA																															BASE + 0x0124
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CH2_CSC_CTL		CH2_MASK_EN	CH2_OSDM				CH2_PREM	CH2_ARGB_TYPE				CH2_PIC_TYPE			CH2_GLO_A								CH2_ALPHA_SEL		CH2_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect. Read as zero.	R

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25:24	CH2_CSC_CTL	Channel 2 color space conversion control. 2'b00: no color conversion 2'b01: YUV to RGB conversion 2'b10: RGB to YUV conversion	RW
23	CH2_MASK_EN	Channel 2 mask enable If this bit is set to 1, the pixel values of this channel will always be the value in OSD_CH2_BAK_ARGB 0: Mask disable 1: Mask enable	RW
22:19	CH2_OSDM	Channel 2 OSD mode. 4'd0: source over 4'd1: src 4'd2: dst 4'd3: clear 4'd4: dst over 4'd5: src in 4'd6: dst in 4'd7: src out 4'd8: dst out 4'd9: src at top 4'd10: dst at top 4'd11: XOR	RW
18	CH2_PREM	Channel 2 OSD pre multiplier If this bit is set to 0, then the pixel values for OSD calculation is: OSD_R = Alpha x R OSD_G = Alpha x G OSD_B = Alpha x B If this bit is set to 1, the pixel values for OSD calculation will not change. 0: not pre multiplier 1: pre multiplied	RW
17:14	CH2_ARGB_TYPE	Channel 2 ARGB type. 4'b0000: ARGB 4'b0001: ARBG 4'b0010: AGRB 4'b0011: AGBR 4'b0100: ABRG 4'b0101: ABGR 4'b1000: RGBA 4'b1001: RBGA 4'b1010: GRBA 4'b1011: GBRA 4'b1100: BRGA 4'b1101: BGRA	RW
13:11	CH2_PIC_TYPE	Pic type. 3'b000: ARGB 3'b001: RGB(per pixel occupy 4 byte in memory storage) 3'b010: NV12 3'b011: NV21 3'b100: RGBA1555(the sequence of RGB is determined by CH2_ARGB_TYPE)	RW
10:3	CH2_GLO_A	Channel 2 global value	RW
2:1	CH2_ALPHA_SEL	Channel 2 alpha sel. 2'b00: pixel alpha 2'b01: global alpha 2'b10: pixel alpha x (global alpha/256)	RW
0	CH2_EN	Channel 2 dma enable 0: disable	RW

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		1: enable	

4.7.2.45 OSD Dma In Channel 3 Parameters Register (OSD_CH3_PARA, 0x0128)

The OSD_CH3_PARA register is used to set controls signals for Channel 3 OSD function.

	OSD_CH3_PARA																															BASE + 0x0128
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CH3_CSC_CTL		CH3_MASK_EN	CH3_OSDM				CH3_PREM	CH3_ARGB_TYPE				CH3_PIC_TYPE			CH3_GLO_A								CH3_ALPHA_SEL		CH3_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect. Read as zero.	R
25:24	CH3_CSC_CTL	Channel 3 color space conversion control. 2'b00: no color conversion 2'b01: YUV to RGB conversion 2'b10: RGB to YUV conversion	RW
23	CH3_MASK_EN	Channel 3 mask enable If this bit is set to 1, the pixel values of this channel will always be the value in OSD_CH3_BAK_ARGB 0: Mask disable 1: Mask enable	RW
22:19	CH3_OSDM	Channel 3 OSD mode. 4'd0: source over 4'd1: src 4'd2: dst 4'd3: clear 4'd4: dst over 4'd5: src in 4'd6: dst in 4'd7: src out 4'd8: dst out 4'd9: src at top 4'd10: dst at top 4'd11: XOR	RW
18	CH3_PREM	Channel 3 OSD pre multiplier If this bit is set to 0, then the pixel values for OSD calculation is: OSD_R = Alpha x R OSD_G = Alpha x G OSD_B = Alpha x B If this bit is set to 1, the pixel values for OSD calculation will not change.	RW

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		0: not pre multiplier 1: pre multiplied	
17:14	CH3_ARGB_TYPE	Channel 3 ARGB type. 4'b0000: ARGB 4'b0001: ARBG 4'b0010: AGRB 4'b0011: AGBR 4'b0100: ABRG 4'b0101: ABGR 4'b1000: RGBA 4'b1001: RBGA 4'b1010: GRBA 4'b1011: GBRA 4'b1100: BRGA 4'b1101: BGRA	RW
13:11	CH3_PIC_TYPE	Pic type. 3'b000: ARGB 3'b001: RGB(per pixel occupy 4 byte in memory storage) 3'b010: NV12 3'b011: NV21 3'b100: RGBA1555(the sequence of RGB is determined by CH3_ARGB_TYPE)	RW
10:3	CH3_GLO_A	Channel 3 global value	RW
2:1	CH3_ALPHA_SEL	Channel 3 alpha sel. 2'b00: pixel alpha 2'b01: global alpha 2'b10: pixel alpha x (global alpha/256)	RW
0	CH3_EN	Channel 3 dma enable 0: disable 1: enable	RW

4.7.2.46 OSD DMA In Back Channel Parameters Register (OSD_CH_BK_PARA, 0x012C)

The OSD_CH_BK_PARA register is used to set controls signals for background channel.

	OSD_CH_BK_PARA																															BASE + 0x012C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											CH_BK_WHOLE_PIC_IN	CH_BK_MASK_EN	CH_BK_PREM	CH_BK_ARGB_TYPE				CH_BK_PIC_TYPE			CH_BK_GLO_A								CH_BK_ALPHA_SEL		CH_BK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:21	Reserved	Writing has no effect. Read as zero.	R
20	CH_BK_WHOLE_PIC_EN	Whether whole picture need to do OSD operation. 0: only overlapped region in background need to do OSD operation, other pixels will just bypass OSD module. 1: whole background picture need to do OSD operation, if in this mode, not only the overlapped pixels of background picture with 4 OSD layers need to do OSD operation, but also the non-overlapped pixel need also to do OSD calculation with zero value pixel.	RW
19	CH_BK_MASK_EN	Channel background mask enable If this bit is set to 1, the pixel values of this channel will always be the value in OSD_BK_BAK_ARGB 0:disable 1: enable	RW
18	CH_BK_PREM	Background Channel OSD pre multiplier. 0: not pre multiplier 1: pre multiplied	RW
17:14	CH_BK_ARGB_TYPE	Background Channel ARGB type. 4'b0000: ARGB 4'b0001: ARBG 4'b0010: AGRB 4'b0011: AGBR 4'b0100: ABRG 4'b0101: ABGR 4'b1000: RGBA 4'b1001: RBGA 4'b1010: GRBA 4'b1011: GBRA 4'b1100: BRGA 4'b1101: BGRA	RW
13:11	CH_BK_PIC_TYPE	Pic type. 3'b000: ARGB 3'b001: RGB(per pixel occupy 4 byte in memory storage) 3'b010: NV12 3'b011: NV21	RW
10:3	CH_BK_GLO_A	Background Channel global alpha value	RW
2:1	CH_BK_ALPHA_SEL	Background Channel alpha sel. 2'b00: pixel alpha 2'b01: global alpha 2'b10: pixel alpha x (global alpha/256)	RW
0	Reserved	Writing has no effect. Read as zero.	RW

4.7.2.47 OSD Channel 0 in Back ARGB Value Register (OSD_CH0_BAK_ARGB, 0x0130)

The OSD_CH0_BAK_ARGB register is used to set background ARGB value for channel 0.

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	OSD_CH0_BAK_ARGB																															BASE + 0x0130
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH0_BAK_ARGB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_CH0_BAK_ARGB	When CH0_MASK_EN =1, channel 0 will output this ARGB values for OSD function. If background picture format is ARGB/RGB, this data sequence of this register is also ARGB. If background picture format is NV12/NV21, then the data sequence of this register is AYUV	RW

4.7.2.48 OSD Channel 1 in Back ARGB Value Register (OSD_CH1_BAK_ARGB, 0x0134)

The OSD_CH1_BAK_ARGB register is used to set background ARGB value for channel 1.

	OSD_CH1_BAK_ARGB																															BASE + 0x0134
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH1_BAK_ARGB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_CH1_BAK_ARGB	When CH1_MASK_EN =1, channel 1 will output this ARGB values for OSD function. If background picture format is ARGB/RGB, this data sequence of this register is also ARGB. If background picture format is NV12/NV21, then the data sequence of this register is AYUV	RW

4.7.2.49 OSD Channel 2 in Back ARGB Value Register (OSD_CH2_BAK_ARGB, 0x0138)

The OSD_CH2_BAK_ARGB register is used to set background ARGB value for channel 2.

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	OSD_CH2_BAK_ARGB																															BASE + 0x0138
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH2_BAK_ARGB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_CH2_BAK_ARGB	When CH2_MASK_EN =1, channel 2 will output this ARGB values for OSD function. If background picture format is ARGB/RGB, this data sequence of this register is also ARGB. If background picture format is NV12/NV21, then the data sequence of this register is AYUV	RW

4.7.2.50 OSD Channel 3 in Back ARGB Value Register (OSD_CH3_BAK_ARGB, 0x013C)

The OSD_CH3_BAK_ARGB register is used to set background ARGB value for channel 3.

	OSD_CH3_BAK_ARGB																															BASE + 0x013C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH3_BAK_ARGB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_CH3_BAK_ARGB	When CH3_MASK_EN =1, channel 3 will output this ARGB values for OSD function. If background picture format is ARGB/RGB, this data sequence of this register is also ARGB. If background picture format is NV12/NV21, then the data sequence of this register is AYUV	RW

4.7.2.51 OSD Background Channel Back ARGB Value Register (OSD_CH_B_BAK_ARGB, 0x0140)

The OSD_CH_B_BAK_ARGB register is used to set background ARGB value for background

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channel.

	OSD_CH_B_BAK_ARGB																															BASE + 0x0140
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_CH_B_BAK_ARGB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_CH_B_BAK_ARGB	When CH_BK_MASK_EN =1, background channel will output this ARGB values for OSD function. If background picture format is ARGB/RGB, this data sequence of this register is also ARGB. If background picture format is NV12/NV21, then the data sequence of this register is AYUV	RW

4.7.2.52 OSD Channel 0 CSC C0 Coefficient Register (CH0_CSC_C0_COEF, 0x0148)

The CH0_CSC_C0_COEF register is used to set the channel 0 coefficient of formula for YUV to RGB or RGB to YUV conversion in OSD function. If in CSC function, channel 0 CSC parameters are used for background CSC function, and the setting are as follows:

1. ARGB/RGB to NV: RGB to YUV conversion parameters.
2. NV to ARGB/RGB: YUV to RGB conversion parameters.
3. NV to HSV: YUV to RGB conversion parameters

	CH0_CSC_C0_COEF																															BASE + 0x0148
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_C01_COEF												Reserved								CH0_C00_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH0_C01_COEF	The C01 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

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19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH0_C00_COEF	The C00 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

NOTE:

1. YUV to RGB conversion formula:

   R = C00*(Y –LUMA_OF) + C01*(Cr-CHROM_OF) + C02*(Cr-CHROM_OF)

   G = C10*(Y – LUMA_OF) – C11*(Cb-CHROM_OF) – C12*(Cr-CHROM_OF)

   B = C20*(Y – LUMA_OF) + C21*(Cb-CHROM_OF) + C22*(Cr-CHROM_OF)

   Recomended parameters:

   C00: 0x4ad C01: 0 C02: 0x669

   C10: 0x4ad C11: 0x193 C12: 0x344

   C20: 0x4ad C21: 0x81A C22: 0x0

2. RGB to YUV conversion formula:

   Y = C00*R + C01*G + C02*B + LUMA_OF

   U = -C10*R – C11*G + C12*B + CHROM_OF

   V = C20*R - C21*G - C22*B + CHROM_OF

   Recomended parameters:

   C00: 0x106

   C01: 0x202

   C02: 0x64

   C10: 0x97

   C11: 0x129

   C12: 0x1C0

   C20: 0x1C0

   C21: 0x177

   C22: 0x49

4.7.2.53 OSD Channel 0 CSC C1 Coefficient Register (CH0_CSC_C1_COEF, 0x014C)

The CH0_CSC_C1_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH0_CSC_C1_COEF																															BASE + 0x014C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_C10_COEF												Reserved								CH0_C02_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH0_C10_COEF	The C10 coefficient for YUV/YCbCr to RGB or RGB to	RW

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		YUV/YCbCr conversion.	
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH0_C02_COEF	The C02 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.54 OSD Channel 0 CSC C2 Coefficient Register (CH0_CSC_C2_COEF, 0x0150)

The CH0_CSC_C2_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH0_CSC_C2_COEF																															BASE + 0x0150
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_C12_COEF												Reserved				CH0_C11_COEF															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH0_C12_COEF	The C12 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH0_C11_COEF	The C11 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.55 OSD Channel 0 CSC C3 Coefficient Register (CH0_CSC_C3_COEF, 0x0154)

The CH0_CSC_C3_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH0_CSC_C3_COEF																															BASE + 0x0154
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_C21_COEF												Reserved				CH0_C20_COEF															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH0_C21_COEF	The C21 coefficient for YUV/YCbCr to RGB or RGB to	RW

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		YUV/YCbCr conversion.	
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH0_C20_COEF	The C20 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.56 OSD Channel 0 CSC C4 Coefficient Register (CH0_CSC_C4_COEF, 0x0158)

The CH0_CSC_C4_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH0_CSC_C4_COEF																															BASE + 0x0158
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				CH0_C22_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH0_C22_COEF	The C22 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.57 OSD Channel 0 CSC Offset Parameter Register (CH0_CSC_OFSET_PARA, 0x015C)

The. CH0_CSC_OFSET_PARA register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH0_CSC_OFSET_PARA																															BASE + 0x015C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CH0_CHROM_OF								Reserved								CH0_LUMA_OF							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect. Read as zero.	R

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23:16	CH0_CHROM_OF	Chroma offset value.	RW
15:8	Reserved	Writing has no effect. Read as zero.	R
7:0	Ch0_LUMA_OF	Luma offset value.	RW

4.7.2.58 OSD Channel 1 CSC C0 Coefficient Register (CH1_CSC_C0_COEF, 0x0160)

The CH1_CSC_C0_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH1_CSC_C0_COEF																															BASE + 0x0160
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_C01_COEF												Reserved				CH1_C00_COEF															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH1_C01_COEF	The C01 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH1_C00_COEF	The C00 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

NOTE:

1. YUV to RGB conversion formula:

   R = C00*(Y –LUMA_OF) + C01*(Cr-CHROM_OF) + C02*(Cr-CHROM_OF)

   G = C10*(Y – LUMA_OF) – C11*(Cb-CHROM_OF) – C12*(Cr-CHROM_OF)

   B = C20*(Y – LUMA_OF) + C21*(Cb-CHROM_OF) + C22*(Cr-CHROM_OF)

   Recomended parameters:

   C00: 0x4ad C01: 0 C02: 0x669

   C10: 0x4ad C11: 0x193 C12: 0x344

   C20: 0x4ad C21: 0x81A C22: 0x0

2.RGB to YUV conversion formula:

   Y = C00*R + C01*G + C02*B + LUMA_OF

   U = -C10*R – C11*G + C12*B + CHROM_OF

   V = C20*R - C21*G - C22*B + CHROM_OF

   Recomended parameters:

   C00: 0x106

   C01: 0x202

   C02: 0x64

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C10: 0x97
C11: 0x129
C12: 0x1C0
C20: 0x1C0
C21: 0x177
C22: 0x49

4.7.2.59 OSD Channel 1 CSC C1 Coefficient Register (CH1_CSC_C1_COEF, 0x0164)

The CH1_CSC_C1_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH1_CSC_C1_COEF																															BASE + 0x0164
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_C10_COEF												Reserved								CH1_C02_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH1_C10_COEF	The C10 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH1_C02_COEF	The C02 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.60 OSD Channel 1 CSC C2 Coefficient Register (CH1_CSC_C2_COEF, 0x0168)

The CH1_CSC_C2_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH1_CSC_C2_COEF																															BASE + 0x0168
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_C12_COEF												Reserved								CH1_C11_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:20	CH1_C12_COEF	The C12 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH1_C11_COEF	The C11 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.61 OSD Channel 1 CSC C3 Coefficient Register (CH1_CSC_C3_COEF, 0x016C)

The CH1_CSC_C3_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH1_CSC_C3_COEF																															BASE + 0x016C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_C21_COEF												Reserved				CH1_C20_COEF															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH1_C21_COEF	The C21 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH1_C20_COEF	The C20 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.62 OSD Channel 1 CSC C4 Coefficient Register (CH1_CSC_C4_COEF, 0x0170)

The CH1_CSC_C4_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH1_CSC_C4_COEF																															BASE + 0x0170
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				CH1_C22_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH1_C22_COEF	The C22 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.63 OSD Channel 1 CSC Offset Parameter Register (CH1_CSC_OFSET_PARA, 0x0174)

The. CH1_CSC_OFSET_PARA register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH1_CSC_OFSET_PARA																															BASE + 0x0174
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CH1_CHROM_OF								Reserved								CH1_LUMA_OF							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect. Read as zero.	R
23:16	CH1_CHROM_OF	Chroma offset value.	RW
15:8	Reserved	Writing has no effect. Read as zero.	R
7:0	Ch1_LUMA_OF	Luma offset value.	RW

4.7.2.64 OSD Channel 2 CSC C0 Coefficient Register (CH2_CSC_C0_COEF, 0x0178)

The CH2_CSC_C0_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH2_CSC_C0_COEF																															BASE + 0x0178
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_C01_COEF												Reserved								CH2_C00_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:20	CH2_C01_COEF	The C01 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH2_C00_COEF	The C00 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

NOTE:

1. YUV to RGB conversion formula:

   R = C00*(Y –LUMA_OF) + C01*(Cr-CHROM_OF) + C02*(Cr-CHROM_OF)

   G = C10*(Y – LUMA_OF) – C11*(Cb-CHROM_OF) – C12*(Cr-CHROM_OF)

   B = C20*(Y – LUMA_OF) + C21*(Cb-CHROM_OF) + C22*(Cr-CHROM_OF)

   Recomended parameters:

   C00: 0x4ad C01: 0 C02: 0x669

   C10: 0x4ad C11: 0x193 C12: 0x344

   C20: 0x4ad C21: 0x81A C22: 0x0

2.RGB to YUV conversion formula:

   Y = C00*R + C01*G + C02*B + LUMA_OF

   U = -C10*R – C11*G + C12*B + CHROM_OF

   V = C20*R - C21*G - C22*B + CHROM_OF

   Recomended parameters:

   C00: 0x106

   C01: 0x202

   C02: 0x64

   C10: 0x97

   C11: 0x129

   C12: 0x1C0

   C20: 0x1C0

   C21: 0x177

   C22: 0x49

4.7.2.65 OSD Channel 2 CSC C1 Coefficient Register (CH2_CSC_C1_COEF, 0x017C)

The CH2_CSC_C1_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH2_CSC_C1_COEF																															BASE + 0x017C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_C10_COEF												Reserved								CH2_C02_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:20	CH2_C10_COEF	The C10 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH2_C02_COEF	The C02 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.66 OSD Channel 2 CSC C2 Coefficient Register (CH0_CSC_C2_COEF, 0x0180)

The CH2_CSC_C2_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH2_CSC_C2_COEF																															BASE + 0x0180
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_C12_COEF												Reserved				CH2_C11_COEF															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH2_C12_COEF	The C12 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH2_C11_COEF	The C11 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.67 OSD Channel 2 CSC C3 Coefficient Register (CH0_CSC_C3_COEF, 0x0184)

The CH2_CSC_C3_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH2_CSC_C3_COEF																															BASE + 0x0184
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_C21_COEF												Reserved				CH2_C20_COEF															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:20	CH2_C21_COEF	The C21 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH2_C20_COEF	The C20 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.68 OSD Channel 2 CSC C4 Coefficient Register (CH2_CSC_C4_COEF, 0x0188)

The CH2_CSC_C4_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH2_CSC_C4_COEF																															BASE + 0x0188
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				CH2_C22_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH2_C22_COEF	The C22 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.69 OSD Channel 2 CSC Offset Parameter Register (CH2_CSC_OFSET_PARA, 0x018C)

The. CH2_CSC_OFSET_PARA register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH2_CSC_OFSET_PARA																															BASE + 0x018C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CH2_CHROM_OF								Reserved								CH2_LUMA_OF							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:24	Reserved	Writing has no effect. Read as zero.	R
23:16	CH2_CHROM_OF	Chroma offset value.	RW
15:8	Reserved	Writing has no effect. Read as zero.	R
7:0	Ch2_LUMA_OF	Luma offset value.	RW

4.7.2.70 OSD Channel 3 CSC C0 Coefficient Register (CH0_CSC_C0_COEF, 0x0190)

The CH3_CSC_C0_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH3_CSC_C0_COEF																															BASE + 0x0190
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH3_C01_COEF												Reserved				CH3_C00_COEF															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH3_C01_COEF	The C01 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH3_C00_COEF	The C00 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

NOTE:

1. YUV to RGB conversion formula:

   R = C00*(Y –LUMA_OF) + C01*(Cr-CHROM_OF) + C02*(Cr-CHROM_OF)

   G = C10*(Y – LUMA_OF) – C11*(Cb-CHROM_OF) – C12*(Cr-CHROM_OF)

   B = C20*(Y – LUMA_OF) + C21*(Cb-CHROM_OF) + C22*(Cr-CHROM_OF)

   Recomended parameters:

   C00: 0x4ad C01: 0 C02: 0x669

   C10: 0x4ad C11: 0x193 C12: 0x344

   C20: 0x4ad C21: 0x81A C22: 0x0

2.RGB to YUV conversion formula:

   Y = C00*R + C01*G + C02*B + LUMA_OF

   U = -C10*R – C11*G + C12*B + CHROM_OF

   V = C20*R - C21*G - C22*B + CHROM_OF

   Recomended parameters:

   C00: 0x106

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C01: 0x202
C02: 0x64
C10: 0x97
C11: 0x129
C12: 0x1C0
C20: 0x1C0
C21: 0x177
C22: 0x49

4.7.2.71 OSD Channel 3 CSC C1 Coefficient Register (CH3_CSC_C1_COEF, 0x0194)

The CH3_CSC_C1_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH3_CSC_C1_COEF																															BASE + 0x0194
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH3_C10_COEF												Reserved								CH3_C02_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH3_C10_COEF	The C10 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH3_C02_COEF	The C02 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.72 OSD Channel 3 CSC C2 Coefficient Register (CH3_CSC_C2_COEF, 0x0198)

The CH3_CSC_C2_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH3_CSC_C2_COEF																															BASE + 0x0198
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH3_C12_COEF												Reserved								CH3_C11_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:20	CH0_C12_COEF	The C12 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH0_C11_COEF	The C11 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.73 OSD Channel 3 CSC C3 Coefficient Register (CH3_CSC_C3_COEF, 0x019C)

The CH3_CSC_C3_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH3_CSC_C3_COEF																															BASE + 0x019C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH3_C21_COEF												Reserved								CH3_C20_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	CH3_C21_COEF	The C21 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW
19:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH3_C20_COEF	The C20 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.74 OSD Channel 3 CSC C4 Coefficient Register (CH3_CSC_C4_COEF, 0x01A0)

The CH3_CSC_C4_COEF register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH3_CSC_C4_COEF																															BASE + 0x01A0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				CH0_C22_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CH3_C22_COEF	The C22 coefficient for YUV/YCbCr to RGB or RGB to YUV/YCbCr conversion.	RW

4.7.2.75 OSD Channel 3 CSC Offset Parameter Register (CH3_CSC_OFSET_PARA, 0x01A4)

The. CH3_CSC_OFSET_PARA register is used to set the coefficient of formula for YUV to RGB or RGB to YUV conversion.

	CH3_CSC_OFSET_PARA																															BASE + 0x01A4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CH3_CHROM_OF								Reserved								CH3_LUMA_OF							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect. Read as zero.	R
23:16	CH3_CHROM_OF	Chroma offset value.	RW
15:8	Reserved	Writing has no effect. Read as zero.	R
7:0	Ch3_LUMA_OF	Luma offset value.	RW

4.7.2.76 Read Arbiter Control Register (RD_ARB_CTL, 0x01A8)

The RD_ARB_CTL register is used to control read arbiter function.

	RD_ARB_CTL																															BASE + 0x01A8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH4_PRIO			CH3_PRIO			CH2_PRIO			CH1_PRIO			CH0_PRIO			ARB_MODE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:13	CH4_PRIO	Channel 4 priority	RW
12:10	CH3_PRIO	Channel 3 priority	RW
9:7	CH2_PRIO	Channel 2 priority	RW
6:4	CH1_PRIO	Channel 1 priority	RW
3:1	CH0_PRIO	Channel 0 priority There are 8 channels in this arbiter, and the priority value can be chosen from these values: 0, 1, 2, ,3, 4, 5, 6, 7(from high to low), if ARB_MODE =0, then the priority of 8 channels must be assigned a priority value, and each channel priority should be unique.	RW
0	ARB_MODE	Arbiter mode 0: fixed priority mode 1: round-robin mode	RW

4.7.2.77 Cycle Number For Processing One Frame Register (CYC_NUM_ONE_FRA, 0x01AC)

The CYC_NUM_ONE_FRA register is used to counter the cycle number for processing one frame data.

	CYC_NUM_ONE_FRA																															BASE + 0x01AC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLK_NUM_ONE_FRA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CLK_NUM_ONE_FRA	The total cycle number for processing one framer	R

4.7.2.78 OSD Layer Padding ARGB Value Register (OSD_LAY_PADDING_ARGB, 0x01B0)

The OSD_LAY_PADDING_ARGB register is used to set the padding argb value for 4 osd layer channels.

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	OSD_LAY_PADDING_ARGB																															
																																BASE + 0x01B0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSD_LAY_PADDING_ARGB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	OSD_LAY_PADDING_ARGB	Padding argb value for 4 OSD layer channel	RW

4.7.2.79 Debug Signals Register (DEBUG_INFO_SIGNALS, 0x01B4)

The DEBUG_INFO_SIGNALS register is used to provide signals information for IPU debug.

	DEBUG_INFO_SIGNALS																															
																																BASE + 0x01B4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEBUG_INFO_SIGNALS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEBUG_INFO_SIGNALS	Debug information signals, the value of this register depend on DEBUG_SEL in register 0x74: DEBUG_SEL: 3'b000: channel 0 module debug signals 3'b001: channel 1 module debug signals 3'b010: channel 2 module debug signals 3'b011: channel 3 module debug signals 3'b100: channel background module debug signals 3'b101: data control module debug signals 3'b110: yuv2nv module debug signals	R

4.8 Operation Flow

4.8.1 OSD function data flow

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NOTE:

1. If any of 4 OSD layers is enable, data output address must be set the same value with input data address in separated background channel.

4.8.2 CSC function data flow

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NOTE:

1. In CSC function, you should set channel 0 CSC parameter registers for CSC function if necessary.

4.9 Index

Table 4-4 Description of Proprietary Vocabulary

Name	Description
IPU	Image Process Unit
CSC	Color Space Conversion
OSD	On Screen Display
DMA	Direct Memory Access

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Section 3

DISPLAY/AUDIO

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5 Display Controller specification

5.1 Features

5.1.1 Layer feature

- Support 2 layer DMA channel
- Support input format：,RGB8888,RGB888, RGB565, RGB555,NV12, NV21
- Support frame size 4x4~800x800
- Support global alpha

5.1.2 Composition feature

- Support 2 layer Alpha Blending
- Support frame size 4x4~800x800

5.1.3 Display feature

- Support TFT(RGB666)
- Support SLCD(MIPI-DBI type A ,type B, type C)
- Support 640x480@60hz

5.2 Architecture map

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5.3 Descriptor definition

5.3.1 Frame Configure descriptor definition

Word	Bit	Name	Function
1st(FrameCfgAddr)	31-0	FrameNextCfgAddr	Frame 's next descriptor address
2nd(FrameSize)	31-27	reserved	--
	26-16	Height	Frame's height
	10-0	Width	Frame's width
3rd(FrameCtrl)	31-5	reserved	--
	4-3	Keep 0	For internal use only, please keep 0.
	2	Keep 1	For internal use only, Please keep 1.
	1	Keep 0	For internal use only, Please keep 0.
	0	Stop	1: This is the last frame; 0: Keep refreshing.
4th(Reserved)	31-0	reserved	--
5th(Reserved)	31-0	reserved	--
6th(Layer0CfgAddr)	31-0	Layer0CfgAddr	Layer0 Cfg Descriptor address
7th(Layer1CfgAddr)	31-0	Layer1CfgAddr	Layer1 Cfg Descriptor address
8th(Reserved)	31-0	reserved	--
9th(Reserved)	31-0	reserved	--
10th(LayerCfgScaleEn)	31-16	reserved	--
	15-12	Keep 0	Please keep default value.
	11-10	Lay1's Z order	Z order of layer.0 is the bottom layer; 1 is the top layer.
	9-8	Lay0's Z order	Z order of layer.0 is the bottom layer; 1 is the top layer.
	7-6	Keep 0	Please keep default value.
	5	Layer1 En	1: enable; 0: disable.
	4	Layer0 En	1: enable; 0: disable.
	3-0	Keep 0	For internal use only, Please keep 0.
11th(Interrupt Control)	31-16	Reserved	Writing has no effect, read as zero.
	17	EOD_MSK	mask of DISP_END 1: generate interrupt 0: interrupt is masked
	16	Reserved	Writing has no effect, read as zero.
	15	Keep 0	For internal use only, Please keep 0.
	14-2	Reserved	Writing has no effect, read as zero.
	2	SOF_MSK	mask of FRM_START 1: generate interrupt 0: interrupt is masked
	1	EOF_MSK	mask of FRM_END 1: generate interrupt

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			0: interrupt is masked
	0	Reserved	--

5.3.2 Layer Configure descriptor definition

Word	Bit	Name	Function
1st(LayerSize)	31-28	Reserved	--
	27-16	Height	Layer's height
	11-0	Width	Layer's width
2nd(LayerCfg)	31-20	Reserved	--
	19-16	Format	Format of layer. 0000：RGB555 0010：RGB565 0100：RGB888 0101：ARGB8888 1000：NV12 1001：NV21 others：reserved
	15	Reserved	--
	14	PREMULT	Premultiplied alpha: 1:enable;0:disable
	13	GAlpha_en	1: enable; 0: disable
	12-10	Color	Color of source data in memory 000：RGB 001：RBG 010：GRB 011：GBR 100：BRG 101：BGR The module will transform these colors to RGB, which will be used for composing or output to display module directly. These bits are useless when Format is not RGB kind.
	9-8	Reserved	--
	7-0	GAlpha	Global Alpha for layer.
3rd (LayerBufferAddr_RGB/Y)	31-0	LayerBufferAddr_RGB/Y	The head address of the RGB frame or Y buffer in DDR memory. Aligned by 8B..
4th(Reserved)	31-3	Reserved	--
	2-0	Keep 0	Internal use, please keep 0.
5th(Reserved)	31-0	Reserved	--

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6th(Reserved)	31-0	Reserved	--
7th(LayerPos)	31-28	Reserved	--
	27-16	YPos	Y position of Left-Top point of layer in frame.
	15-12	Reserved	--
	11-0	XPos	X position of Left-Top point of layer in frame.
8th(Reserved)	31-0	Reserved	--
9th(Reserved)	31-0	Reserved	--
10th(LayerStride_RGB/Y)	31-12	Reserved	--
	11-0	LayerStride_RGB/Y	stride(unit: pixel). Aligned by 8B. Layer Stride. Support 4k(4096) (Unit: pixel(RGB) or byte(Y))
11th(BufferAddr_UV)	31-0	BufferAddr_UV	The head address of the UV buffer in DDR memory. Aligned by 8B.
12th(stride_UV)	31-0	stride_UV	stride(unit: byte). Aligned by 8B.

5.4 Registers Description

5.4.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. The registers can be read and written by AHB2 bus
3. Register read/write attribute
   - ✧ R - Read only
   - ✧ W - Write only
   - ✧ RW - read and write
   - ✧ RCW - read and write, but clear to 0 by read
   - ✧ RSW - read and write, but set to 1 by read
   - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
   - ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
   - ✧ RC - read only, and clear to 0 by read
   - ✧ RS - read only, and set to 1 by read
   - ✧ SPEC - special access method, relate to its description
4. Reset Value
   - – 1 - reset to 1
   - – 0 - reset to 0
   - – ? - value unknown after reset

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5.4.2 Register Memory Map

The DC's registers map base address is 0x13050000

The DC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 5-1 DC Registers Map

Name	Reset Value	Address Offset	Description	RW	Mask
FRM_CFG_ADDR	0x0000_0000	0x0000	frame descriptor's address	RW	0xFFFF_FFFF
FRM_CFG_CTRL	0x0000_0000	0x0004	frame descriptor's control	W	0x0000_0003
CTRL	0x0000_0000	0x2000	DC control	RW	0x0000_006D
ST	0x0000_0000	0x2004	DC status	R	0x0082_0F57
CLR_ST	0x0000_0000	0x2008	DC clear status	W	0x8081_FFC6
INTC	0x0000_0000	0x200C	DC interrupt mask	RW	0x8081_FFC6
INT_FLAG	0x0000_0000	0x2010	DC interrupt flag	R	0x8081_FFC6
COM_CFG	0x003F_00FC	0x2014	DC common config	RW	0x0033_00FE
PCFG_RD_CTRL	0x0000_0006	0x2018	Back door for read channel's QoS	RW	0x0000_0007
PCFG_OFIFO	0x0319_0842	0x2020	Priority level threshold config when comp direct or rdma	RW	0x07FF_FFFF
LAY0_DES_READ	0x0000_0000	0x2100	for debug	R	0xFFFF_FFFF
LAY1_DES_READ	0x0000_0000	0x210c	for debug	R	0xFFFF_FFFF
FRM_CHAIN_SITE	0x0000_0000	0x2200	frame descriptor's current site	R	0xFFFF_FFFF
LAY0 _RGB_SITE	0x0000_0000	0x3100	layer0's REG current site	R	0xFFFF_FFFF
LAY1 _RGB_SITE	0x0000_0000	0x3104	layer1's REG current site	R	0xFFFF_FFFF
LAY0_Y_SITE	0x0000_0000	0x3120	layer0's Y current site	R	0xFFFF_FFFF
LAY0_UV_SITE	0x0000_0000	0x3124	layer0's UV current site	R	0xFFFF_FFFF
LAY1_Y_SITE	0x0000_0000	0x3128	layer1's Y current site	R	0xFFFF_FFFF
LAY1_UV_SITE	0x0000_0000	0x312C	layer1's UV current site	R	0xFFFF_FFFF
LAY0_CSC_MULT_YRV	0x0662_04a8	0x3200	CSC mult-coef for Y and RV	RW	0x07FF_07FF
LAY0_CSC_MULT_GUGV	0x0341_0190	0x3204	CSC mult-coef for GU and GV	RW	0x03FF_01FF
LAY0_CSC_MULT_BU	0x0000_0812	0x3208	CSC mult-coef for BU	RW	0x0000_0FFF
LAY0_CSC_SUB_YUV	0x0080_0000	0x320C	CSC sub-coef for YUV	RW	0x00FF_001F
LAY1_CSC_MULT_YRV	0x0662_04a8	0x3210	CSC mult-coef for Y and RV	RW	0x07FF_07FF
LAY1_CSC_MULT_GUGV	0x0341_0190	0x3214	CSC mult-coef for GU	RW	0x03FF_01FF

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			and GV		
LAY1_CSC_MULT_BU	0x0000_0812	0x3218	CSC mult-coef for BU	RW	0x0000_0FFF
LAY1_CSC_SUB_YUV	0x0080_0000	0x321C	CSC sub-coef for YUV	RW	0x00FF_001F
DISP_COM	0x0000_00E0	0x8000	display common configure	RW	0x0000_00E0
TFT_HSYNC	0x0000_0000	0x9000	TFT HSYNC	RW	0x0FFF_0FFF
TFT_VSYNC	0x0000_0000	0x9004	TFT VSYNC	RW	0x0FFF_0FFF
TFT_HDE	0x0000_0000	0x9008	TFT HDE	RW	0x0FFF_0FFF
TFT_VDE	0x0000_0000	0x900C	TFT VDE	RW	0x0FFF_0FFF
TFT_CFG	0x0000_0000	0x9010	TFT configure	RW	0x0000_07FF
TFT_ST	0x0000_0000	0x9014	TFT status	R	0x0000_0001
SLCD_CFG	0x0154_0D20	0xA000	SLCD configure	RW	0x0FFF_0FFF
SLCD_WR_DUTY	0x0000_0000	0xA004	SLCD WR's duty	RW	0xFFFF_FFFF
SLCD_TIMING	0x0000_0000	0xA008	SLCD timing	RW	0xFFFF_FFFF
SLCD_FRM_SIZE	0x0000_0000	0xA00C	frame size	RW	0xFFFF_FFFF
SLCD_SLOW_TIME	0x0000_0000	0xA010	slow time	RW	0x0000_FFFF
SLCD_REG_IF	0x8000_0000	0xA014	SLCD reg-op interface	RW	0xE0FF_FFFF
SLCD_ST	0x0000_0000	0xA018	SLCD status	R	0x0000_0001
SLCD_REG_CTRL	0x0000_0000	0xA01C	SLCD reg-op interface control	W	0x0000_0001

5.4.3 Composer configure

5.4.3.1 Frame configure

5.4.3.1.1 Frame descriptor address(DC_FRM_CFG_ADDR, 0x0000)

	DC_FRM_CFG_ADDR																BASE + 0x0000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_CHAIN_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FRM_CHAIN_ADDR	This is the address of the 1st descriptor when not composing; When composing, it is the address of the next descriptor. It can be set and changed.	RW

5.4.3.1.2 Frame descriptor control(DC_FRM_CFG_CTRL,0x0004)

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	DC_FRM_CFG_CTRL																															BASE + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														KEEP0	FRM_CFG_START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect. Read as zero.	R
1	Keep0	For internal use only, Please keep 0.	W
0	FRM_CFG_START	Frame descriptor DMA start	W

5.4.3.2 Control configure(DC_CTRL,0x2000)

	DC_CTRL																															BASE + 0x2000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									TFT_START	SLCD_START	Reserved	GEN_STP_DISP	DES_CNT_RST	Reserved	QCK_STP_DISP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6	TFT_START	Write 1 to start TFT transfer.	W
5	SLCD_START	Write 1 to start SLCD transfer. Used for sending pixel by DMA When in single frame mode, write 1 for each frame.	W
4	Reserved	Please keep default value.	W
3	GEN_STP_DISP	General stop the display channel. Assure integrity of the current frame	W
2	DES_CNT_RST	Reset the counter of FRM_DES, LAYx_DES	W
1	Reserved	Writing has no effect. Read as zero.	R
0	QCK_STP_DISP	Quick stop the display channel. Stop as quickly as possible, the integrity of the current frame not be guaranteed.	W

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5.4.3.3 Status Register(DC_ST,0x2004)

	DC_ST																															BASE + 0x2004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CMP_END	Reserved					DISP_END	Reserved					BDMA1_END	BDMA0_END	BDMA_END	TFT_UNDR	Reserved	STOP_DISP_ACK	WRBK_WORKING	DIRECT_WORKING	Reserved	FRM_START	FRM_END	WORKING
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect. Read as zero.	R
23	CMP_END	composer end of each frame	R
22:18	Reserved	Writing has no effect. Read as zero.	R
17	DISP_END	One frame display end	R
16:12	Reserved	Writing has no effect. Read as zero.	R
11	BDMA1_END	layer1's block DMA end	R
10	BDMA0_END	layer0's block DMA end	R
9	BDMA_END	all layer's block DMA end	R
8	TFT_UNDR	TFT jump into under-run mode	R
7	Reserved	Writing has no effect. Read as zero.	R
6	STOP_DISP_ACK	Display channel is general stop	R
5	Reserved	Writing has no effect. Read as zero.	R
4	DIRECET_WORKING	Composer direct output channel is working	R
3	Reserved	Writing has no effect. Read as zero.	R
2	FRM_START	One frame start reading	R
1	FRM_END	One frame read end	R
0	WORKING	display controller is working	R

5.4.3.4 Clear status Register(DC_CSR,0x2008)

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	DC_CSR																															BASE + 0x2008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLR_CMP_W_SLOW	Reserved							CLR_CMP_END	Reserved					CLR_DISP_END	Reserved					CLR_BDMA1_END	CLR_BDMA0_END	CLR_BDMA_END	CLR_TFT_UNDR	Reserved	CLR_STP_DISP_ACK	Reserved			CLR_FRM_START	CLR_FRM_END	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CLR_CMP_W_SLOW	Clear CMP_W_SLOW	W
30:24	Reserved	Writing has no effect. Read as zero.	R
23	CLR_CMP_END	clear CMP_END	W
22:18	Reserved	Writing has no effect. Read as zero.	R
17	CLR_DISP_END	clear DISP_END	W
16:12	Reserved	Writing has no effect. Read as zero.	R
11	CLR_BDMA1_END	clear BDMA1_END	W
10	CLR_BDMA0_END	clear BDMA0_END	W
9	CLR_BDMA_END	clear BDMA_END	W
8	CLR_TFT_UNDR	clear TFT_UNDR	W
7	Reserved	Writing has no effect. Read as zero.	W
6	CLR_STP_DISP_ACK	clear STOP_DISP_ACK	W
5:3	Reserved	Writing has no effect. Read as zero.	R
2	CLR_FRM_START	clear FRM_START	W
1	CLR_FRM_END	clear FRM_END	W
0	Reserved	Writing has no effect. Read as zero.	R

5.4.3.5 INTC register(DC_INTC,0x200C)

	DC_INTC																															BASE + 0x200C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CWS_MSK	Reserved							EOC_MSK	Reserved					EOD_MSK	OOW_MSK	EOW_MSK	EOR_MSK	EOB3_MSK	EOB2_MSK	EOB1_MSK	EOB0_MSK	EOB_MSK	UOT_MSK	SWA_MSK	SDA_MSK	Reserved			SOF_MSK	EOF_MSK	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31	CWS_MSK	mask of CMP_W_SLOW 1: generate interrupt 0: interrupt is masked	RW
30:24	Reserved	Writing has no effect, read as zero.	R
23	EOC_MSK	mask of CMP_END 1: generate interrupt 0: interrupt is masked	RW
22:18	Reserved	Writing has no effect, read as zero.	R
17	EOD_MSK	mask of DISP_END 1: generate interrupt 0: interrupt is masked	RW
22:12	Reserved	Writing has no effect, read as zero.	R
11	EOB1_MSK	mask of BDMA1_END 1: generate interrupt 0: interrupt is masked	RW
10	EOB0_MSK	mask of BDMA0_END 1: generate interrupt 0: interrupt is masked	RW
9	EOB_MSK	mask of BDMA_END 1: generate interrupt 0: interrupt is masked	RW
8	UOT_MSK	mask of TFT_UNDR 1: generate interrupt 0: interrupt is masked	RW
7	Reserved	Writing has no effect, read as zero.	R
6	SDA_MSK	mask of STOP_DISP_ACK 1: generate interrupt 0: interrupt is masked	RW
5:3	Reserved	Writing has no effect, read as zero.	R
2	SOF_MSK	mask of FRM_START 1: generate interrupt 0: interrupt is masked	RW
1	EOF_MSK	mask of FRM_END 1: generate interrupt 0: interrupt is masked	RW
0	Reserved	Writing has no effect. Read as zero.	R

5.4.3.6 INT flag register(DC_INTC,0x2010)

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	DC_INTC																															BASE + 0x2010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT_CWS	Reserved							INT_EOC	Reserved					INT_EOD	INT_OOW	INT_EOW	INT_EOR	INT_EOB3	INT_EOB2	INT_EOB1	INT_EOB0	INT_EOB	INT_UOT	INT_SWA	INT_SDA	Reserved			INT_SOF	INT_EOF	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	INT_CWS	interrupt of CMP_W_SLOW	RW
30:24	Reserved	Writing has no effect, read as zero.	R
23	INT_EOC	interrupt of CMP_END	R
22:18	Reserved	Writing has no effect, read as zero.	R
17	INT_EOD	interrupt of DISP_END	R
16:12	Reserved	Writing has no effect, read as zero.	R
11	INT_EOB1	interrupt of BDMA1_END	R
10	INT_EOB0	interrupt of BDMA0_END	R
9	INT_EOB	interrupt of BDMA_END	R
8	INT_UOT	interrupt of TFT_UNDR	R
7	Reserved	Writing has no effect, read as zero.	R
6	INT_SDA	interrupt of STOP_DISP_ACK	R
5:3	Reserved	Writing has no effect, read as zero.	R
2	INT_SOF	interrupt of FRM_START	RW
1	INT_EOF	interrupt of FRM_END	RW
0	Reserved	Writing has no effect, read as zero.	R

5.4.3.7 Common configure register(DC_COM_CONFIG,0x2014)

	DC_COM_CONFIG																															BASE + 0x2014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								Inner use		LAYER1_YUVDMA_4K	LAYER0_YUVDMA_4K	Inner use		LAYER1_CLKGATE_EN	LAYER0_CLKGATE_EN	Reserved								Keep 0				BURST_LEN_BDMA		Keep 0	Reserved
RST	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

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Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:22	Inner use	Value no effect.	RW
21	LAYER1_YUVDMA_4K	Burst command splitter for AXI bus command which's cross 4k border. 0:indicate enable 1:indicate disable	RW
20	LAYER0_YUVDMA_4K	Burst command splitter for AXI bus command which's cross 4k border. 0:indicate enable 1:indicate disable	RW
19:18	Inner use	Value no effect.	RW
17	LAYER1_CLKGATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, Layer1's DMA always has clock.	RW
16	LAYER0_CLKGATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, Layer0's DMA always has clock.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:4	Keep 0	Keep 0	R
3:2	BURST_LEN_BDMA	The max length of the block DMA's burst. 2'b00 : 4 burst 2'b01 : 8 burst 2'b10 :16 burst 2'b11 :32 burst(default) **Note:** BURST_LEN_BDMA must be set 16burst or 32 burst for NV12/NV21.no restrict for kind of RGB format. If layer0 use RGB,layer1 use NV12,BURST_LEN_BDMA can't be set 4burst or 8burst.	RW
1	Keep 0	For internal use only, Please keep 0	RW
0	Reserved	Writing has no effect, read as zero.	R

5.4.3.8 Priority configure register

5.4.3.8.1 PCFG_RD_CTRL register(DC_PCFG_RD_CTRL,0x2018)

	DC_PCFG_RD_CTRL																															BASE + 0x2018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													arqos_val		arqos_ctrl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
2:1	Arqos_val	QoS value. 00~11, and reset value is 11.	RW
0	Arqos_ctrl	Whether use the value set by software. 0: the value is generated by the hardware; 1: the value is specified by software.	RW

5.4.3.8.2 OFIFO's PCFG register(DC_OFIFO_PCFG,0x2020)

	DC_OFIFO_PCFG																																BASE + 0x2020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					Pcfg2									Pcfg1									Pcfg0								
RST	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0

OFIFO_PCFG is used when composer output direct or simple read dma

The 3 thresholds cut the output FIFO into 4 space. When the entries remained triggers one of them, the priority level will be altered by hardware. And the 3 thresholds must follow the order: pcfg2 ≥ pcfg1 ≥ pcfg0.

Priority level（arqos）

Priority_lv	Space
11	Empty ~ threshold0
10	Threshold0 ~ threshold1
01	Threshold1 ~ threshold2
00	Threshold2 ~ full

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect. Read as zero.	R
26:18	Pcfg2	Threshold2:0~263	RW
17:9	Pcfg1	Threshold1:0~263	RW
8:0	Pcfg0	Threshold0:0~263	RW

5.4.3.9 Descriptor read registers

5.4.3.9.1 Frame configure descriptor register(DC_FRM_DES,x02100)

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	DC_FRM_DES																															BASE + 0x2100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FRM_DES	Read the frame configure descriptor in order, one at a time. The counter will reset when writing DES_CNT_RST	R

5.4.3.9.2 Layer0 configure descriptor register(DC_LAY0_DES,0x2014)

	DC_LAY0_DES																															BASE + 0x2104
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY0_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY0_DES	Read the layer0 configure descriptor in order, one at a time. The counter will reset when writing DES_CNT_RST	R

5.4.3.9.3 Layer1 configure descriptor register(DC_LAY1_DES,0x2018)

	DC_LAY1_DES																															BASE + 0x2108
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY1_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY1_DES	Read the layer1 configure descriptor in order, one at a time. The counter will reset when writing DES_CNT_RST	R

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5.4.3.10 Software locate register

5.4.3.10.1 Frame descriptor's current site register(DC_FRM_CHAIN_SITE,0x2200)

	DC_FRM_CHAIN_SITE																															BASE + 0x2200
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_CHAIN_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FRM_CHAIN_SITE	Read the address to locate current descriptor's site in the chain.	R

5.4.3.10.2 Layer0's RGB current pixel site register(DC_LAY0_RGB_SITE,0x3100)

	DC_LAY0_RGB_SITE																															BASE + 0x3100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY0_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY0_RGB_SITE	Read the current pixel site in DDR memory of layer0.	R

5.4.3.10.3 Layer1's RGB current pixel site register(DC_LAY1_RGB_SITE,0x3104)

	DC_LAY1_RGB_SITE																															BASE + 0x3104
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY1_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY1_RGB_SITE	Read the current pixel site in DDR memory of layer1.	R

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5.4.3.10.4 Layer0's Y current pixel site register(DC_LAY0_Y_SITE,0x3120)

	DC_LAY0_Y_SITE																															BASE + 0x3120
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY1_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY1_Y_SITE	Read the current pixel site in DDR memory of layer0.	R

5.4.3.10.5 Layer0's UV current pixel site register(DC_LAY0_UV_SITE,0x3124)

	DC_LAY0_UV_SITE																															BASE + 0x3124
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY1_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY1_UV_SITE	Read the current pixel site in DDR memory of layer0.	R

5.4.3.10.6 Layer1's Y current pixel site register(DC_LAY1_Y_SITE,0x3128)

	DC_LAY1_Y_SITE																															BASE + 0x3128
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY1_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY1_Y_SITE	Read the current pixel site in DDR memory of layer1.	R

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5.4.3.10.7 Layer1's UV current pixel site register(DC_LAY1_UV_SITE,0x312C)

	DC_LAY1_UV_SITE																															BASE + 0x312C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY1_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY1_UV_SITE	Read the current pixel site in DDR memory of layer1.	R

5.4.3.11 layer 0's CSC config

5.4.3.11.1 CscMultYRv(LAY0_CSC_MULT_YRV,0x3200)

	LAY0_CSC_MULT_YRV																															BASE + 0x3200
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					CSC_MULT_RV											Reserved					CSC_MULT_Y										
RST	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0	1	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:16	CSC_MULT_RV	CSC multiplication coefficient for RV **NOTE**: reference value mode 0: CSC_MULT_RV = 0x48f mode 1: CSC_MULT_RV = 0x662 (default) mode 2: CSC_MULT_RV = 0x59c	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	CSC_MULT_Y	CSC multiplication coefficient for Y **NOTE**: reference value mode 0: CSC_MULT_Y = 0x400 mode 1: CSC_MULT_Y = 0x4a8 (default) mode 2: CSC_MULT_Y = 0x400	RW

5.4.3.11.2 CscMultGuGv(LAY0_CSC_MULT_GUGV,0x3204)

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	LAY0_CSC_MULT_GUGV																															BASE + 0x3204
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CSC_MULT_GV										Reserved							CSC_MULT_GU								
RST	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	CSC_MULT_GV	CSC multiplication coefficient for GV **NOTE**: reference value mode 0: CSC_MULT_Y = 0x253 mode 1: CSC_MULT_Y = 0x341 (default) mode 2: CSC_MULT_Y = 0x2db	RW
15:9	Reserved	Writing has no effect, read as zero.	R
8:0	CSC_MULT_GU	CSC multiplication coefficient for GU **NOTE**: reference value mode 0: CSC_MULT_Y = 0x193 mode 1: CSC_MULT_Y = 0x190 (default) mode 2: CSC_MULT_Y = 0x160	RW

5.4.3.11.3 CscMultBu(LAY0_CSC_MULT_BU,x03208)

	LAY0_CSC_MULT_BU																															BASE + 0x3208
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				CSC_MULT_BU											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	CSC_MULT_BU	CSC multiplication coefficient for BU **NOTE**: reference value mode 0: CSC_MULT_Y = 0x820 mode 1: CSC_MULT_Y = 0x812(default) mode 2: CSC_MULT_Y = 0x717	RW

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5.4.3.11.4 CscSubYUV(LAY0_CSC_SUB_YUV,0x320C)

	LAY0_CSC_SUB_YUV																															BASE + 0x320C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CSC_SUB_UV								Reserved											CSC_SUB_Y				
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	CSC_SUB_UV	CSC subtraction coefficient for UV **NOTE**: reference value mode 0: CSC_MULT_Y = 0x0 mode 1: CSC_MULT_Y = 0x80 (default) mode 2: CSC_MULT_Y = 0x80	RW
15:5	Reserved	Writing has no effect, read as zero.	R
4:0	CSC_SUB_Y	CSC subtraction coefficient for Y **NOTE**: reference value mode 0: CSC_MULT_Y = 0x0 mode 1: CSC_MULT_Y = 0x0(default) mode 2: CSC_MULT_Y = 0x0	RW

5.4.3.12 Layer 1's CSC config

5.4.3.12.1 CscMultYRv(LAY1_CSC_MULT_YRV,0x3210)

	LAY1_CSC_MULT_YRV																															BASE + 0x3210
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					CSC_MULT_RV											Reserved					CSC_MULT_Y										
RST	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0	1	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
26:16	CSC_MULT_RV	CSC multiplication coefficient for RV **NOTE**: reference value mode 0: CSC_MULT_RV = 0x48f mode 1: CSC_MULT_RV = 0x662 (default)	RW

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		mode 2: CSC_MULT_RV = 0x59c	
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	CSC_MULT_Y	CSC multiplication coefficient for Y **NOTE**: reference value mode 0: CSC_MULT_Y = 0x400 mode 1: CSC_MULT_Y = 0x4a8 (default) mode 2: CSC_MULT_Y = 0x400	RW

5.4.3.12.2 CscMultGuGv(LAY1_CSC_MULT_GUGV,0x3214)

	LAY1_CSC_MULT_GUGV																															BASE + 0x3214
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CSC_MULT_GV										Reserved							CSC_MULT_GU								
RST	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	CSC_MULT_GV	CSC multiplication coefficient for GV **NOTE**: reference value mode 0: CSC_MULT_Y = 0x253 mode 1: CSC_MULT_Y = 0x341 (default) mode 2: CSC_MULT_Y = 0x2db	RW
15:9	Reserved	Writing has no effect, read as zero.	R
8:0	CSC_MULT_GU	CSC multiplication coefficient for GU **NOTE**: reference value mode 0: CSC_MULT_Y = 0x193 mode 1: CSC_MULT_Y = 0x190 (default) mode 2: CSC_MULT_Y = 0x160	RW

5.4.3.12.3 CscMultBu(LAY1_CSC_MULT_BU,0x3218)

	LAY1_CSC_MULT_BU																															BASE + 0x3218
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				CSC_MULT_BU											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0

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Bits	Name	Description	RW
31:12	Reserved	Writing has no effect. Read as zero.	R
11:0	CSC_MULT_BU	CSC multiplication coefficient for BU **NOTE**: reference value mode 0: CSC_MULT_Y = 0x820 mode 1: CSC_MULT_Y = 0x812(default) mode 2: CSC_MULT_Y = 0x717	RW

5.4.3.12.4 CscSubYUV(LAY1_CSC_SUB_YUV,0x321C)

	LAY1_CSC_SUB_YUV																															**BASE + 0x321C**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CSC_SUB_UV								Reserved											CSC_SUB_Y				
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect. Read as zero.	R
23:16	CSC_SUB_UV	CSC subtraction coefficient for UV **NOTE**: reference value mode 0: CSC_MULT_Y = 0x0 mode 1: CSC_MULT_Y = 0x80 (default) mode 2: CSC_MULT_Y = 0x80	RW
15:5	Reserved	Writing has no effect. Read as zero.	R
4:0	CSC_SUB_Y	CSC subtraction coefficient for Y **NOTE**: reference value mode 0: CSC_MULT_Y = 0x0 mode 1: CSC_MULT_Y = 0x0(default) mode 2: CSC_MULT_Y = 0x0	RW

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5.4.4 Display interfaces configure

5.4.4.1 Common(DISP_COM,0x8000)

	DISP_COM																															BASE + 0x8000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										DP_DITHER_DW						Reserved								CGC_DITHER	CGC_SLCD	CGC_TFT	DP_DITHER_EN	Reserved		DP_IF_SEL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect, read as zero.	R
21:16	DP_DITHER_DW	Dither drop bit. [17:16]: configure blue color [19:18]: configure green color [21:20]: configure red color correspondence between blue/green/red color value and drop bit： 0: drop low 0 bit(default) 1: drop low 2 bit 2: drop low 3 bit 3: drop low 4 bit When source pixel is RGB888, and output at RGB666/565, the value should be 010101/100110.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7	CGC_DITHER	Clk gate control for Dither, 1:indicate open clk gate. 0:indicate disable clk gate, Dither always has clock.	RW
6	CGC_SLCD	Clk gate control for SLCD, 1:indicate open clk gate. 0:indicate disable clk gate, SLCD always has clock.	RW
5	CGC_TFT	Clk gate control for TFT, 1:indicate open clk gate. 0:indicate disable clk gate, TFT always has clock.	RW
4	DP_DITHER_EN	Dither enable. 0: dither disable(default) 1: dither enable **NOTE**: If source data is not 888 format, dither need be disabled.	RW
3:2	Reserved	Writing has no effect, read as zero.	R
1:0	DP_IF_SEL	Display interfaces select.	RW

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		0: no display(default) 1: TFT 2: SLCD	

5.4.4.2 TFT

5.4.4.2.1 TIMING_HSYNC(TFT_TIMING_HSYNC,0x9000)

	TFT_TIMING_HSYNC																															BASE + 0x9000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				HPS												Reserved				HPE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HPS	HSYNC pulse start point(base on dot clock cycle) This bit must not be 0.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HPE	HSYNC pulse end point(base on dot clock cycle) This bit must not be 0.	RW

5.4.4.2.2 TIMING_VSYNC(TFT_TIMING_VSYNC,0x9004)

	TFT_TIMING_VSYNC																															BASE + 0x9004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	Reserved				VPS												Reserved				VPE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VPS	VSYNC pulse start point(base on dot clock cycle) This bit must not be 0.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VPE	VSYNC pulse end point(base on dot clock cycle) This bit must not be 0.	RW

5.4.4.2.3 TIMING_HDE(TFT_TIMING_HDE,0x9008)

	TFT_TIMING_HDE																															BASE + 0x9008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				HDS												Reserved				HDE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HDS	Horizontal display area start point (base on dot clock cycle). And it is also the DE pulse start point in horizontal. It indicate the end point of horizontal back porch.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HDE	Horizontal display area end point (base on dot clock cycle). And it is also the DE pulse end point in horizontal. It indicate the end point of horizontal front porch.	RW

5.4.4.2.4 TIMING_VDE(TFT_TIMING_VDE,0x900C)

	TFT_TIMING_VDE																															BASE + 0x900C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	Reserved				VDS												Reserved				VDE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VDS	Vertical display area start point(base on dot clock cycle). And it is also the DE pulse start point in vertical. It indicate the end point of vertical back porch.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VDE	Vertical display area end point(base on dot clock cycle). And it is also the DE pulse end point in vertical. It indicate the start point of vertical front porch.	RW

5.4.4.2.5 TRANS_CONFIG(TFT_TRAN_CFG,0x9010)

	TFT_TRAN_CFG																															BASE + 0x9010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					PIXCLK_INV	DE_DL	SYNC_DL	COLOR_EVEN			COLOR_ODD			MODE	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect, read as zero.	R
10	PIX_CLK_INV	Inverse the polarity of the DOT_CLK	RW
9	DE_DL	Default level of DE(invalid level)	RW
8	SYNC_DL	Default level of HSYNC and VSYNC(invalid level)	RW
7:5	COLOR_EVEN	Output color mode of even lines(2, 4, 6...) 000: RGB→RGB 001: RGB→RBG 010: RGB→BGR 011: RGB→BRG 100: RGB→GBR 101: RGB→GRB	RW
4:2	COLOR_ODD	Output color mode of odd lines(1, 3, 5...)	RW

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		000: RGB→RGB 001: RGB→RBG 010: RGB→BGR 011: RGB→BRG 100: RGB→GBR 101: RGB→GRB	
1:0	MODE	0x: 24bits parallel mode 10: 8bits serial mode without dummy(RGB) 11: 8bits serial mode with dummy(RGBD)	RW

5.4.4.2.6 STATUS(TFT_ST,0x9014)

	TFT_ST																															BASE + 0x9014	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														WORKING	UNDER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	WORKING	0: TFT is not working 1: TFT is working	R
0	UNDER	Indicate the controller jump into recovery state, and starting trans one frame 0 to panel. 0: TFT is working order 1: TFT is in UNDER mode.	R

5.4.4.3 SLCD (Smart LCD)

5.4.4.3.1 SLCD_CONFIG(SLCD_PANEL_CFG,0xA000)

	SLCD_PANEL_CFG																															BASE + 0xA000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_MD	Reserved			RDY_JIT	FMT_EN	DBI_TYPE			PIX_FMT		TE_JIT	TE_MD	TE_SWITCH	RDY_SWITCH	CS_EN	Reserved				CS_DP	RDY_DP	DC_MD	WR_MD	Reserved	TE_DP	DWIDTH			CWIDTH		
RST	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0

Bits	Name	Description	RW
31	FRM_MD	Frame refresh mode.	RW

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		0: single frame mode(default) 1: continuous frame mode	
30:28	Reserved	Writing has no effect, read as zero.	R
27	RDY_ANTI_JIT	Anti-jitter for RDY. 0: sample RDY with 1 pixclk cycle(default) 1: sample RDY with 3 pixclk cycles for anti-jitter.	RW
26	FMT_EN	Whether the pixels by REG_IF need conversion 0: no use conversion;(default) 1: need conversion.	RW
25:23	DBI_TYPE	001: typeA(6800) 010: typeB(8080)(default) 100: typeC(SPI-3line) 101: typeC(SPI-4line) other: reserved NOTE:SPI-3line 444 register mode need to set SLCD_REG_CTRL	RW
22:21	PIX_FMT	Color format. 00: 565 (typeA/B、typeC) 01: 666 (typeA/B) 01: 444 (typeC) 10: 888 (typeA/B、typeC)(default) NOTE: typeA/B For 565, the DWIDTH can be 8bits and 16bits; For DWIDTH = 9bits, there is only 666 format; For DWIDTH = 16bits, there is only 565 format; For DWIDTH = 18bits, there is only 666 format; For 888, the DWIDTH can be 8bits and 24bits; Note: The pairing of DWIDTH and DATA_FMT is only these 5 modes, other configure is error. typeC: There are 444、565、888（for 888,high six bits are valid each byte for lcd screen, so format is 666 for lcd screen）	
20	TE_ANTI_JIT	Anti-jitter for TE. 0: sample TE with 1 pixclk cycle; 1: sample TE with 3 pixclk cycles for anti-jitter(default).	RW
19	TE_MD	The active edge of TE. 0: the front edge(default) 1: the back edge	RW
18	TE_SWITCH	0: do not wait TE, send pix_data after SLCD_START; 1: wait TE, and then send pix_data.(default)	RW
17	RDY_SWITCH	0: do not wait RDY, send command or data immediately;(default) 1: wait RDY, and then send command or data.	RW

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16	CS_EN	CS control enable. 0: The CS pin is controlled by GPIO.(default) 1: The CS pin is controlled by Display Controller.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11	CS_DP	The CS's default polarity 0: the default(invalid) level is low; 1: the default(invalid) level is high;(default)	RW
10	RDY_DP	The RDY's default polarity 0: the default(invalid) level is low; 1: the default(invalid) level is high;(default)	RW
9	DC_MD	DC's definition. 0: Command DC = low, Data DC = high(default) 1: Command DC = high, Data DC = low	RW
8	WR_MD	WR's definition. 0: drive at posedge(drive level is high) sample at negedge(sample level is low); 1: drive at negedge(drive level is low) sample at posedge(sample level is high).(default) Note: When typeC, the WR pin is SPI_CLK.	RW
7	Reserved	Writing has no effect, read as zero.	R
6	TE_DP	The TE' default polarity 0: the default(invalid) level is low;(default) 1: the default(invalid) level is high;	RW
5:3	DWIDTH	Panel's data bus width at typeA/B. 000: 8bits(typeA/B) 001: 9bits(typeA/B) 010: 16bits(typeA/B) 011: 18bits(typeA/B) 100: 24bits(typeA/B) (default) Note: When typeC, DWIDTH is no use.	RW
2:0	CWIDTH	The width of panel's command and it's parameters. 000: 8bits(typeA/B) (default) 001: 9bits(typeA/B) 010: 16bits(typeA/B) 011: 18bits(typeA/B) 100: 24bits(typeA/B) Note: When typeC, CWIDTH is no use. But only 8bits command can be supported.	RW

NOTE1: When configure stage, keep CS inactive.

NOTE2: When DMA mode, pixels will be formatted, not controlled by FMT_EN;
When register mode, command and parameters will not be formatted, not controlled by FMT_EN;
When register mode, pixels will be controlled by FMT_EN (0: SLCD will directly output the low 8/16/18 bits of content of REG_IF directly; 1: SLCD will convert the content of REG_IF.

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NOTE3: format define

8bpp (565 by 2 cycle)：

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																R7	R6	R5	R4	R3	G7	G6	G5
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																G4	G3	G2	B7	B6	B5	B4	B3

8bpp (888 by 3 cycle):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																R7	R6	R5	R4	R3	R2	R1	R0
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																G7	G6	G5	G4	G3	G2	G1	G0
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																B7	B6	B5	B4	B3	B2	B1	B0

9bpp(666 by 2 cycle):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															R7	R6	R5	R4	R3	R3	G7	G6	G5
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															G4	G3	G2	B7	B6	B5	B4	B3	B2

16bpp(565 by 1 cycle):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3

18bpp(666 by 1 cycle):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						R7	R6	R5	R4	R3	R2	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3	B2

24bpp(888 by 1 cycle):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Note4:

When send command by REG_IF, the output command is only decided by CWIDTH. If CWIDTH is 8bits, only the low 8 bits of content of REG_IF are useful, other bits will be lost; if CWIDTH is 9bits, only the low 9bit of content of REG_IF are useful, other bits will be lost; and so on, for each CWIDTH.

5.4.4.3.2 SLCD_WR_DUTY(SLCD_WR_DUTY,0xA004)

	SLCD_WR_DUTY																BASE + 0xA004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	DSTIME								DDTIME								CSTIME								CDTIME							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	DSTIME	WR's sample level period when transmitting pixels or parameters.	RW
23:16	DDTIME	WR's drive level period when transmitting pixels or parameters.	RW
15:8	CSTIME	WR's sample level period when transmitting command	RW
7:0	CDTIME	WR's drive level period when transmitting command	RW

NOTE: The description is based on 8080(MIPI DBI TypeB) and SPI(MIPI DBI TypeC)mode, it's opposite when 6800(MIPI DBI TypeA) mode. The actual cycle is n+1.

5.4.4.3.3 SLCD_TIMING(SLCD_TIMING,0xA008)

	SLCD_TIMING																															**BASE + 0xA008**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCH								TCS								TAH								TAS							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	TCH	Chip select hold time.	RW
23:16	TCS	Chip select setup time.	RW
15:8	TAH	Address hold time.	RW
7:0	TAS	Address setup time.	RW

Note：TAS, TCS, TCH are used in both parallel and serial mode, while TAH is only used in serial mode. The actual cycle is n+1.

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5.4.4.3.4 SLCD_FRM_SIZE(SLCD_FRM_SIZE,0xA00C)

	SLCD_FRM_SIZE																															BASE + 0xA00C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	V_SIZE																H_SIZE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	V_SIZE	Line number of each frame.	RW
15:0	H_SIZE	Pixel number of each line.	RW

5.4.4.3.5 SLCD_SLOW_TIME(SLCD_SLOW_TIME,0xA010)

	SLCD_SLOW_TIME																															BASE + 0xA010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SLOW_TIME															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R

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15:0	SLOW_TIME	SLCD will delay some period of pixclk before transmitting data, after TE's relative edge.	WR

5.4.4.3.6 SLCD_REG_IF(SLCD_REG_IF,0xA014)

	SLCD_REG_IF																															BASE + 0xA014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAG		CMD_END	Reserved					content																							
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	FLAG	It is used to decide the meanings of the DATA/CMD/PARAMETER. 00: pix_data; 01: parameter; 1x: command(default).	RW
29	CMD_END	Indicate this is the last content, the hardware will disable the CS	RW
28:24	Reserved	Writing has no effect, read as zero.	R
23:0	content	content	RW

NOTE: The next command(include its parameters) or pix_data must wait BUSY is 0 when using the reg_if for transferring.

There would no frm_end when sending pixels by SLCD_REG_IF.

5.4.4.3.7 SLCD_STATUS(SLCD_ST,0xA018)

	SLCD_ST																															BASE + 0xA018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															BUSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	BUSY	Indicate whether the SLCD DBI interface controller is working or not. 0: idle 1: busy	R

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5.4.4.3.8 SLCD_REG_CTRL(SLCD_REG_CTRL,x0A01C)

	SLCD_REG_CTRL																															BASE + 0xA01C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															RST_3lINE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	RST_3LINE	Write 1 to reset an inner counter when sending frame by SLCD_REG_IF, write one before each frame(only used at typeC 3line 444 register mode	W

5.5 Operation guide

5.5.1 Composer operation

(1) Prepare four layer and frame descriptor chain. In first, you should create four layer's descriptor, because frame descriptor has four layer descriptor's address.

(2) Set frame descriptor's address by DC_FRM_CFG_ADDR register.

(3) Set DIS_IF_SEL register for TFT or SLCD.

(4) Set DC_FRM_CFG_CTRL register to start composer.

(5) Wait until FRM_CFG_END interrupt, indicate frame's descriptor has been read, then software should update frame descriptor chain.

5.5.2 TFT operation

(1) Set TFT_TIMING_HSYNC, TFT_TIMING_VSYNC, TFT_TIMING_HDE, TFT_TIMING_VDE;

for example, see picture of 5.4.4.2: HS, invalid time of HSYNC, need 5 cycles at least, HBP need 10 cycles, HFP need 10 cycles, and there are 800 pixels per line. So HPS need set 5, HPE need set 825; HDS need set 15, HDE need set 815; configure VSYNC and VDE use same method.

(2) Set TFT_TRAN_CFG

PIX_CLK_INV, DE_DL and SYNC_DL respectively used to adjust the phase of DOT_CLK, DE, HSYNC and VSYNC; COLOR_EVEN and COLOR_ODD used to change the output mode of pixel color mode; MODE used to configure the transfer mode.

(3) Start to configure composer as steps 5.5.1

5.5.3 SLCD operation

(1) Configure each bit of SLCD_PANEL_CFG according to the relevant instructions;

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(2) Set SLCD_WR_DUTY, SLCD_TIMING and SLCD_SLOW_TIME to meet panel requirements;

(3) Set SLCD_FRM_SIZE to the actual size;

(4) Start to configure composer as steps 5.5.1

(5) Set FMT_EN of SLCD_PANEL_CFG to 0(if no command, skip this step);

(6) Write a command and its flag to SLCD_CMD(if no command, skip this step);

(7) Wait BUSY of SLCD_ST is 0(if no command, skip this step);

(8) Repeat step(5) and (6) until all command send out(if no command, skip this step);

(9) Set FMT_EN to 1;

(10) Write SLCD_START;

(11) Wait FRM_END of DC_ST, and clear it;

(12) Repeat step(5) to (11) for next frame transfer.

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6 Audio Interface Controller(AIC)

6.1 Overview

This chapter describes the AIC (I2S) included in this processor.

The AIC supports the I2S or IIS (for inter-IC sound), a protocol defined by Philips Semiconductor. Both normal I2S and the MSB-justified I2S formats are supported by AIC.

AIC consists of buffers, status registers, control registers, serializers, and counters for transferring digitized audio between the processor's system memory, an internal I2S CODEC. AIC can record digitized audio by storing the samples in system memory. For playback of digitized audio or production of synthesized audio, the AIC retrieves digitized audio samples from system memory and sends them to a CODEC through the serial connection with I2S formats. The internal digital-to-analog converter in the CODEC then converts the audio samples into an analog audio waveform. The audio sample data can be stored to and retrieved from system memory either by the DMA controller or by programmed I/O.

Where both normal I2S and MSB-justified-I2S work with a variety of clock rates, which can be obtained either by dividing the PLL clock by two programmable dividers or from an internal clock source.

6.2 Features

- 16, 20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
- DMA transfer mode supported
- Stop serial clock supported
- Programmable Interrupt function supported
- Support mono PCM data to stereo PCM data expansion on audio play back
- Support endian switch on 16-bits normal audio samples play back
- Internal programmable or internal serial clock and optional system clock supported for I2S or MSB-Justified format
- Two FIFOs for transmit and receive respectively

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6.3 Block Diagram

Figure 6-1 AIC Block Diagram

6.4 Data Format Description

6.4.1 I2S and MSB-justified serial audio format

Normal I2S and MSB-justified are similar protocols for digitized stereo audio transmitted over a serial path.

The BIT_CLK supplies the serial audio bit rate, the basis for the internal CODEC bit-sampling logic. Its frequency is 64 times the audio sampling frequency. Divided by 64, the resulting 8 kHz to 48 kHz or even higher signal signifies timing for left and right serial data samples passing on the serial data paths. This left/right signal is sent to the CODEC on the SYNC pin. Each phase of the left/right signal is accompanied by one serial audio data sample on the data pins DAC_SDATA and ADC_SDATA.

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Figure 6-2 I2S data format (A: LR mode)

In the A: LR mode, first send the left channel in a stereo frame. One Left slot and one Right slot make a sample frame. It is the normal mode of I2S.

Figure 6-3 I2S data format (B: RL mode)

In the B: RL mode, first send the right channel in a stereo frame. One Right slot and one Left slot make a sample frame. It is used in same CODEC.

Figure 6-4 MSB-justified data format (C: LR mode)

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In the C: LR mode, first send the left channel in a stereo frame. One Left slot and one Right slot make a sample frame. It is the normal mode in MSB-justified.

Figure 6-5 MSB-justified data format (D: RL mode)

In the D: RL mode, first send the right channel in a stereo frame. One Right slot and one Left slot make a sample frame.

Data is transmitted and received in frames of 64 BIT_CLK cycles(If BIT_CLK is generated internally). Each frame consists of a left sample and a right sample. Each sample holds 8, 16, 18, 20 or 24 bits of valid data. The LSB other bits of each sample is padded with zeroes.

In the normal I2S mode, the SYNC is low for the left sample and high for the right sample. Also, the MSB of each data sample lags behind the SYNC edges by one BIT_CLK cycle.
In the MSB-justified mode, the SYNC is high for the left sample and low for the right sample. Also, the MSB of each data sample is aligned with the SYNC edges.

6.4.2 Audio sample data placement in DAC_SDATA/ADC_SDATA

The placement of audio sample in incoming/outgoing serial data stream for all formats support in AIC is MSB (Most Significant Bit) justified. Suppose n bit sample composed by

S_{n-1}	S_{n-2}	…	S_2	S_1	S_0

Following table described the how sample data bits are transferred.

Table 6-1 Sample data bit relate to DAC_SDATA/ADC_SDATA bit

I2S/MSB-Justified Format					
SDATA IN/OUT	**8**	**16**	**18**	**20**	**24**
B31	S7	S15	S17	S19	S23
B30	S6	S14	S16	S18	S22

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B29	S5	S13	S15	S17	S21
B28	S4	S12	S14	S16	S20
B27	S3	S11	S13	S15	S19
B26	S2	S10	S12	S14	S18
B25	S1	S9	S11	S13	S17
B24	S0	S8	S10	S12	S16
B23	0	S7	S9	S11	S15
B22	0	S6	S8	S10	S14
B21	0	S5	S7	S9	S13
B20	0	S4	S6	S8	S12
B19	0	S3	S5	S7	S11
B18	0	S2	S4	S6	S10
B17	0	S1	S3	S5	S9
B16	0	S0	S2	S4	S8
B15	0	0	S1	S3	S7
B14	0	0	S0	S2	S6
B13	0	0	0	S1	S5
B12	0	0	0	S0	S4
B11	0	0	0	0	S3
B10	0	0	0	0	S2
B9	0	0	0	0	S1
B8	0	0	0	0	S0
B7~B0	0	0	0	0	0

If in 16 bits packed mode, the data transferred is the same as the 16 bits normal mode as shown above. But there are two samples in one word.

6.5 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect

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RC- Read only, and Clear to 0 by read

RS- Read only, and Set to 1 by read

3. Reset Value

1 - reset to 1

0 - reset to 0

? - value unknown after reset

6.5.1 Register Memory Map

Table 6-2 Registers Memory Map Base Address

Name	Base	Description
AIC	0x10020000	Address base of AIC

The AIC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 6-3 AIC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
AICFR	RW	0x0710_0000	0x0000	32
AICCR	RW	0x0124_0000	0x0004	32
I2SCR	RW	0x0000_0000	0x0010	32
AICSR	RW	0x0000_0008	0x0014	32
I2SSR	R	0x0000_0000	0x001C	32
I2SDIV	RW	0x0003_0003	0x0030	32
AICDR	RW	0x0000_0000	0x0034	32

- AICFR is used to control FIFO threshold, I2S/MSB-justified selection, AIC reset, master/slave selection
- AICCR is used to control DMA mode, FIFO flush, interrupt enable, internal loop-back, play back and recording enable. It also controls sample size and signed/unsigned data transfer.
- I2SCR is used to control BIT_CLK stop, audio sample size, I2S or MSB-justified selection in I2S/MSB-justified.
- AICSR is used to reflect FIFOs status.
- I2SDIV is used to set clock divider for BIT_CLK generating in I2S/MSB-justified format.
- AICDR is act as data input/output port to/from transmit/receive FIFO when write/read..

6.5.2 Register and Fields Description

6.5.2.1 AIC Configuration Register (AICFR,0x0000)

AICFR contains bits to control FIFO threshold, I2S/MSB-justified selection, AIC reset, master/slave selection, and AIC enable.

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	AICFR																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	rg_codec_srst	Reserved	Reserved		RFTH				Reserved			TFTH					Reserved			MSB	SYSCKD	IBCKD	ISYNCD	DMODE	CDC_MASTER	LSMP	ICDC	AUSEL	RST	BCKD	SYNCD	ENB
RST	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	rg_codec _srst	Internal codec software reset . 0：Not reset the internal codec； 1：Reset the internal codec	RW
30:28	Reserved	Writing has no effect, read as zero.	R
27:24	RFTH	Receive FIFO threshold for interrupt or DMA request. The RFTH valid value is 0 ~ 15. This value represents a threshold value of (RFTH + 1) * 2. When the sample number in receive FIFO, indicated by AICSR.RFL, is great than or equal to the threshold value, AICSR.RFS is set. Larger RFTH value provides lower DMA/interrupt request frequency but have more risk to involve receive FIFO overflow. The optimum value is system dependent.	RW
23:21	Reserved	Writing has no effect, read as zero.	R
20:16	TFTH	Transmit FIFO threshold for interrupt or DMA request. The TFTH valid value 0 ~ 31. This value represents a threshold value of TFTH * 2. When the sample number in transmit FIFO, indicated by AICSR.TFL, is less than or equal to the threshold value, AICSR.TFS is set. Smaller TFTH value provides lower DMA/interrupt request frequency but have more risk to involve transmit FIFO underflow. The optimum value is system dependent.	RW
15:11	Reserved	Writing has no effect, read as zero.	R
12	MSB	The big-endian format enable. When this bit is '1', the replay data will use the big-endian format. The sign bit at the bit 31. Else the replay data is little-endian format.	RW
11	SYSCKD	SYSCLK Direction. This bit specifies input/output direction of SYSCLK. BCKD: BIT_CLK Direction 0: SYSCLK is generated internally and driven out to the CODEC. 1: SYSCLK is input from an internal source.	RW
10	IBCKD	Keep this value to 0 in normal use.	RW
9	ISYNCD	Keep this value to 0 in normal use.	RW
8	DMODE	Keep this value to 0 in normal use.	RW
7	CDC_		RW

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	MASTER	**CDC_MASTER** / **CDC_MASTER used** 0 / **Reserved** 1 / **Codec master mode**	
6	LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. **LSMP** / **CODEC used** 0 / **Play ZERO sample when TX FIFO underflow.** 1 / **Play last sample when TX FIFO underflow.**	RW
5	ICDC	**ICDC** / **CODEC used** 0 / **Reserved** 1 / **Internal CODEC.**	RW
4	AUSEL	Audio Unit Select. Change this bit in case of BIT_CLK is stopped (I2SCR.STPBK = 1). **AUSEL** / **Selected** 0 / **Reserved** 1 / **Select I2S/MSB-justified format.**	RW
3	RST	Reset AIC. Write 1 to this bit reset AIC registers and FIFO except AICFR and I2SDIV register. Writing 0 to this bit has no effect and this bit is always reading 0.	W
2	BCKD	BIT_CLK Direction. This bit specifies input/output direction of BIT_CLK. It is only valid in I2S/MSB-justified format. Change this bit in case of BIT_CLK is stopped (I2SCR.STPBK = 1). **BCKD** / **BIT_CLK Direction** 0 / BIT_CLK is input from an internal source. 1 / BIT_CLK is generated internally and driven out to the CODEC.	RW
1	SYNCD	SYNC Direction. This bit specifies input/output direction of SYNC in I2S/MSB-justified format. Change this bit in case of BIT_CLK is stopped (I2SCR.STPBK = 1). **SYNCD** / **SYNC Direction** 0 / SYNC is input from an internal source. 1 / SYNC is generated internally and driven out to the CODEC.	RW
0	ENB	Enable AIC function. This bit is used to enable or disable the AIC function. **ENB** / **Description** 0 / **Disable AIC Controller.** 1 / **Enable AIC Controller.**	RW

The BCKD bit (bit 2) and SYNCD bit (bit 1) configure the mode of I2S/MSB-justified interface. This is compliant with I2S specification.

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BCKD	SYNCD	Description
0 (input)	0 (input)	AIC roles the slave of I2S/MSB-justified interface.
	1 (output)	AIC roles the master with internal serial clock source of I2S/MSB-justified interface.
1 (output)	0 (input)	Reserved.
	1 (output)	AIC roles the master of I2S/MSB-justified interface.

6.5.2.2 AIC Common Control Register (AICCR,0x0004)

AICCR contains bits to control DMA mode, FIFO flush, interrupt enable, internal loop-back, play back and recording enable. It also controls sample size and signed/unsigned data transfer.

	AICCR																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		Reserved_0	PACK16	Reserved	CHANNEL			Reserved		OSS			ISS			RDMS	TDMS	Reserved		M2S	ENDSW	ASVTSU	TFLUSH	RFLUSH	EROR	ETUR	ERFS	ETFS	ENLBF	ERPL	EREC
RST	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29	Reserved	Keep this value to 0 in normal use.	R
28	PACK16	Output Sample data 16bit packed mode select. This bit reflects that one word contains two sample data or only one sample data with LSB align. The packed mode is only support 16bit sample size. **PACK16** / **Sample Size** 0: Unpacked data mode. One word only contains one 16bit sample data aligned LSB. 1: Packed data mode. One word contains two 16 bit sample data.	RW
27	Reserved	Writing has no effect, read as zero.	R
26:24	CHANNEL	Output Channel Number Select. These bits reflect output data channels from AIC to device. The data supported are: 1(mono), 2(stereo), 4, 6 and 8 channels. The sample data is LSB-justified in memory/register. **CHANNEL** / **Sample Size** 0x0: 1 channel, mono mode. 0x1: 2 channels, stereo mode. 0x2 ~ 0x7: Reserved.	RW
23:22	Reserved	Writing has no effect, read as zero.	R

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<table>
<tr><td>21:19</td><td>OSS</td><td>Output Sample Size. These bits reflect output sample data size from memory or register. The data sizes supported are: 8, 16, 18, 20 and 24 bits. The sample data is LSB-justified in memory/register.
<table>
<tr><th>OSS</th><th>Sample Size</th></tr>
<tr><td>0x0</td><td>8 bit.</td></tr>
<tr><td>0x1</td><td>16 bit.</td></tr>
<tr><td>0x2</td><td>18 bit.</td></tr>
<tr><td>0x3</td><td>20 bit.</td></tr>
<tr><td>0x4</td><td>24 bit.</td></tr>
<tr><td>0x5~0x7</td><td>Reserved.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>18:16</td><td>ISS</td><td>Input Sample Size. These bits reflect input sample data size to memory or register. The data sizes supported are: 8, 16, 18, 20 and 24 bits. The sample data is LSB-justified in memory/register.
<table>
<tr><th>ISS</th><th>Sample Size</th></tr>
<tr><td>0x0</td><td>8 bit.</td></tr>
<tr><td>0x1</td><td>16 bit.</td></tr>
<tr><td>0x2</td><td>18 bit.</td></tr>
<tr><td>0x3</td><td>20 bit.</td></tr>
<tr><td>0x4</td><td>24 bit.</td></tr>
<tr><td>0x5~0x7</td><td>Reserved.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>15</td><td>RDMS</td><td>Receive DMA enable. This bit is used to enable or disable the DMA during receiving audio data.
<table>
<tr><th>RDMS</th><th>Receive DMA</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>14</td><td>TDMS</td><td>Transmit DMA enable. This bit is used to enable or disable the DMA during transmit audio data.
<table>
<tr><th>TDMS</th><th>Transmit DMA</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>13:12</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>11</td><td>M2S</td><td>Mono To Stereo. This bit control whether to do mono to stereo sample expansion in play back. When this bit is set, every outgoing sample data in the steam plays in both left and right channels. This bit should only be set in 2 channels configuration. It takes effective immediately when the bit is changed. Change this before replay started.
<table>
<tr><th>M2S</th><th>Description</th></tr>
<tr><td>0</td><td>No mono to stereo expansion.</td></tr>
<tr><td>1</td><td>Do mono to stereo expansion.</td></tr>
</table></td><td>RW</td></tr>
</table>

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<table>
<tr><td>10</td><td>ENDSW</td><td>Endian Switch. This bit control endian change on outgoing 16-bits size audio sample by swapping high and low bytes in the sample data.
<table>
<tr><th>ENDSW</th><th>Description</th></tr>
<tr><td>0</td><td>No change on outgoing sample data.</td></tr>
<tr><td>1</td><td>Swap high and low byte for outgoing 16-bits size sample data.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>9</td><td>ASVTSU</td><td>Audio Sample Value Transfer between Signed and Unsigned data format. This bit is used to control the signed ←→unsigned data transfer. If it is 1, the incoming and outgoing audio sample data will be transferred by toggle its most significant bit.
<table>
<tr><th>ASVTSU</th><th>Description</th></tr>
<tr><td>0</td><td>No audio sample value signed ←→unsigned transfer.</td></tr>
<tr><td>1</td><td>Do audio sample value signed ←→unsigned transfer.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>8</td><td>TFLUSH</td><td>Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.</td><td>W</td></tr>
<tr><td>7</td><td>RFLUSH</td><td>Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.</td><td>W</td></tr>
<tr><td>6</td><td>EROR</td><td>Enable ROR Interrupt. This bit is used to control the ROR interrupt enable or disable.
<table>
<tr><th>EROR</th><th>ROR Interrupt</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>5</td><td>ETUR</td><td>Enable TUR Interrupt. This bit is used to control the TUR interrupt enable or disable.
<table>
<tr><th>ETUR</th><th>TUR Interrupt</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>4</td><td>ERFS</td><td>Enable RFS Interrupt. This bit is used to control the RFS interrupt enable or disable.
<table>
<tr><th>ERFS</th><th>RFS Interrupt</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>3</td><td>ETFS</td><td>Enable TFS Interrupt. This bit is used to control the TFS interrupt enable or disable.
<table>
<tr><th>ETFS</th><th>TFS Interrupt</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
</table>

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2	ENLBF	Enable AIC Loop Back Function. This bit is used to enable or disable the internal loop back function of AIC, which is used for test only. When the AIC loop back function is enabled, normal audio replay/record functions are disabled. **ENLBF** / **Description** 0 / AIC Loop Back Function is Disabled. 1 / AIC Loop Back Function is Enabled.	RW
1	ERPL	Enable Playing Back function. This bit is used to disable or enable the audio sample data transmitting. **ERPL** / **Description** 0 / **AIC Playing Back Function is Disabled.** 1 / **AIC Playing Back Function is Enabled.**	RW
0	EREC	Enable Recording Function. This bit is used to disable or enable the audio sample data receiving. **EREC** / **Description** 0 / **AIC Recording Function is Disabled.** 1 / **AIC Recording Function is Enabled.**	RW

6.5.2.3 AIC I2S/MSB-justified Control Register (I2SCR,0x0010)

I2SCR contains bits to control BIT_CLK stop, audio sample size, I2S or MSB-justified selection in I2S/MSB-justified. It is valid only in I2S/MSB-justified format.

	I2SCR																																Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														RFIRST	SWLH	Reserved		ISTPBK	STPBK	Reserved							ESCLK	Reserved			AMSL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17	RFIRST	Send R channel first in stereo mode. This bit should only be set in 2 channels configuration. The frame is LR like or RL like. It takes effective immediately when the bit is changed. Change this before replay started. **RFIRST** / **Description** 0 / **Send L channel first. (LR)** 1 / **Send R channel first. (RL)**	RW
16	SWLH	Switch LR channel in 16bit-packed stereo mode. This bit control whether the low address data is L or R. This bit should	RW

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		only be set in 2 channels configuration and 16bit-packed mode. That means it can only valid with packed mode (PACK16 =1) and 2 channels (CHANNEL=0x1). It takes effective immediately when the bit is changed. Change this before replay started. **SWLH** / **Description** 0 — **16 bit LSB and 16bit MSB is not switched.** 1 — **16 bit LSB and 16bit MSB is switched.**	
15:14	Reserved	Writing has no effect, read as zero.	R
13	ISTPBK	Keep this value to 0 in normal use.	RW
12	STPBK	Stop BIT_CLK. It is used to stop the BIT_CLK in I2S/MSB-justified format. **STPBK** / **Description** 0 — **BIT_CLK is not stopped.** 1 — **BIT_CLK is stopped.** Please set this bit to 1 to stop BIT_CLK when change AICFR.AUSEL and AICFR.BCKD.	RW
11:5	Reserved	Writing has no effect, read as zero.	R
4	ESCLK	Enable SYSCLK output. When this bit is 1, the SYSCLK outputs to chip outside is enabled. Else, the clock is disabled.	RW
3:1	Reserved	Writing has no effect, read as zero.	R
0	AMSL	Specify Alternate Mode (I2S or MSB-Justified) Operation. **AMSL** / **Description** 0 — Select I2S Operation Mode. 1 — Select MSB-Justified Operation Mode.	RW

6.5.2.4 AIC Controller FIFO Status Register (AICSR,0x0014)

AICSR contains bits to reflect FIFOs status. Most of the bits are read-only except two, which can be written a 0.

	AICSR																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		RFL						Reserved								TFL								Reserved	ROR	TUR	RFS	TFS	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

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<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:30</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>29:24</td><td>RFL</td><td>Receive FIFO Level. The bits indicate the amount of valid PCM data in Receive FIFO.
<table>
<tr><th>RFL Value</th><th>Description</th></tr>
<tr><td>0x00 ~ 0x20</td><td>RFL valid PCM data in receive FIFO.</td></tr>
<tr><td>0x21 ~ 0x3F</td><td>Reserved.</td></tr>
</table></td><td>R</td></tr>
<tr><td>23:14</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>13:8</td><td>TFL</td><td>Transmit FIFO Level. The bits indicate the amount of valid PCM data in Transmit FIFO.
<table>
<tr><th>TFL Value</th><th>Description</th></tr>
<tr><td>0x00 ~ 0x3F</td><td>TFL valid PCM data in transmit FIFO.</td></tr>
</table></td><td>R</td></tr>
<tr><td>7</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>6</td><td>ROR</td><td>Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun.
<table>
<tr><th>ROR</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>When read, indicates over-run has not been found.</td></tr>
<tr><td>When write, clear itself.</td></tr>
<tr><td rowspan="2">1</td><td>When read, indicates data has even been written to full receive FIFO.</td></tr>
<tr><td>When write, not effects.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>5</td><td>TUR</td><td>Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run.
<table>
<tr><th>TUR</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>When read, indicates under-run has not been found.</td></tr>
<tr><td>When write, clear itself.</td></tr>
<tr><td rowspan="2">1</td><td>When read, indicates data has even been read from empty transmit FIFO.</td></tr>
<tr><td>When write, not effects.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>4</td><td>RFS</td><td>Receive FIFO Service Request. This bit indicates that receive FIFO level is or not below receive FIFO threshold, which is controlled by AICFR.RFTH. When RFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting.
<table>
<tr><th>RFS</th><th>Description</th></tr>
<tr><td>0</td><td>Receive FIFO level below RFL threshold.</td></tr>
<tr><td>1</td><td>Receive FIFO level at or above RFL threshold.</td></tr>
</table></td><td>R</td></tr>
<tr><td>3</td><td>TFS</td><td>Transmit FIFO Service Request. This bit indicates that transmit FIFO level is below Transmit FIFO threshold, which is controlled by AICFR.TFTH. When TFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting.
<table>
<tr><th>TFS</th><th>Description</th></tr>
</table></td><td>R</td></tr>
</table>

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			0	Transmit FIFO level exceeds TFL threshold.		
			1	Transmit FIFO level at or below TFL threshold.		
2:0	Reserved	Writing has no effect, read as zero.				R

6.5.2.5 AIC I2S/MSB-justified Status Register (I2SSR,0x001C)

I2SSR is used to reflect AIC status in I2S/MSB-justified. It is a read-only register.

	I2SSR																																Base+0x001C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CHBSY	TBSY	RBSY	BSY	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5	CHBSY	AIC Transmitter busy in I2S/MSB-justified format.(Multi-channel status) **CHBSY** — **Description** 0 — AIC Transmitter part is idle or disabled. 1 — AIC Transmitter part currently is transmitting or receiving a frame.	R
4	TBSY	AIC Transmitter busy in I2S/MSB-justified format. **TBSY** — **Description** 0 — AIC Transmitter part is idle or disabled. 1 — AIC Transmitter part currently is transmitting or receiving a frame.	R
3	RBSY	AIC Receiver busy in I2S/MSB-justified format. **RBSY** — **Description** 0 — AIC Receiver part is idle or disabled. 1 — AIC Receiver part currently is transmitting or receiving a frame.	R
2	BSY	AIC busy in I2S/MSB-justified format. **BSY** — **Description** 0 — AIC controller is idle or disabled. 1 — AIC controller currently is transmitting or receiving a frame.	R
1:0	Reserved	Writing has no effect, read as zero.	R

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6.5.2.6 AIC I2S/MSB-justified Clock Divider Register (I2SDIV,0x0030)

I2SDIV is used to set clock divider to generated BIT_CLK from SYS_CLK in I2S/MSB-justified format.

	I2SDIV																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							IDV									Reserved							DV								
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24:16	IDV	Audio IBIT_CLK clock divider value minus 1. I2SDIV.IDV is used to control the generating of IBIT_CLK from dividing SYS_CLK. The dividing value can be even or odd and I2SDIV.IDV should be set to the dividing value minus 1. IBIT_CLK frequency is fixed to 64 f_S in AIC, where f_S is the audio sample frequency. I2SDIV.IDV depends on SYS_CLK frequency f_{SYS_CLK}, which is selected according to internal CODEC's requirement and internal PLL frequency. Please reference to 1.4.10 Serial Audio Clocks and Sampling Frequencies for further description.	RW
15:9	Reserved	Writing has no effect, read as zero.	R
8:0	DV	Audio BIT_CLK clock divider value minus 1. I2SDIV.DV is used to control the generating of BIT_CLK from dividing SYS_CLK. The dividing value can be even or odd and I2SDIV.IDV should be set to the dividing value minus 1. BIT_CLK frequency is fixed to 64 f_S in AIC, where f_S is the audio sample frequency. I2SDIV.DV depends on SYS_CLK frequency f_{SYS_CLK}, which is selected according to internal CODEC's requirement and internal PLL frequency. Please reference to 1.4.10 Serial Audio Clocks and Sampling Frequencies for further description.	RW

6.5.2.7 AIC FIFO Data Port Register (AICDR,0x0034)

AICDR is act as data input port to transmit FIFO when write and data output port from receive FIFO when read, one audio sample every time. The FIFO width is 24 bits. Audio sample with size N that is less than 24 is located in LSB N-bits. The sample size is specified by I2SCR.WL in I2S/MSB-justified. In I2S/MSB-justified, the left channel sample is prior to the right channel sample.

Care should be taken to monitor the status register to insure that there is room for data in the FIFO when executing a program read or write transaction. This is taken care automatically in DMA.

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	AICDR																																Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								DATA																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	DATA	FIFO port. When write to it, data is push to the transmit FIFO. When read from it, data is pop from the receiving FIFO.	RW

6.6 Operation Flow

The AIC can be accessed either by the processor using programmed I/O instructions or by the DMA controller. The processor uses programmed I/O instructions to access the AIC and can access the following types of data.

- **The AIC memory mapped registers data**—All registers are 32 bits wide and are aligned to word boundaries.
- **AIC controller FIFO data—**An entry is placed into the transmit FIFO by writing to the I2S controller's Serial Audio Data register (AICDR). Writing to AICDR updates a transmit FIFO entry. Reading AICDR flushes out a receive FIFO entry.
- **The internal CODEC registers for I2S CODEC—**CODEC registers can be accessed through the L3 bus. The L3 bus operation is emulated by software controlling three GPIO pins.

The DMA controller can only access the FIFOs. Accesses are made through the data registers, as explained in the previous paragraph. The DMA controller responds to the following DMA requests made by the I2S controller:

- The transmit FIFO request is based on the transmit trigger-threshold (AICFR.TFTH) setting. See 6.5.2.1 for further details regarding AICFR.TFTH.
- The receive FIFO request is based on the receive trigger-threshold (AICFR.RFTH) setting. See 6.5.2.1 for further details regarding AICFR.RFTH.

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6.6.1 clock control

Figure 6-6 clock control

cpm_i2s_sysclk	The reference clock from cpm.
aic_mclk_o	The reference clock output to internal or external codec
aic_ibitclk_i	The adc bit clock from external codec use in codec master mode
aic_bitclk_i	The dac bit clock from external codec use in codec master mode
cdc_adc_bclk	The adc bit clock from internal codec use in codec master mode
cdc_dac_bclk	The dac bit clock from internal codec use in codec master mode
aic_ibitclk_o	The adc bit clock to external codec use in codec slave mode
aic_bitclk_o	The dac bit clock to external codec use in codec slave mode
fifo_i_bitclk	The aic adc rfifo clock
fifo_o_bitclk	The aic dac tfifo clock

6.6.1.1 internal codec

when use the internal codec ,the codec can only work as the master mode .please set The AICFR[5] to '1'.

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6.6.1.2 external codec(master mode)

when use the external codec(master mode) ,.please set The AICFR[5] to '0'.

6.6.1.3 external codec(slave mode)

when use the external codec(alave mode) ,.please set The AICFR[5] to '0'. Set AICFR[1], AICFR[2], AICFR[9], AICFR[10] to '1'.

6.6.2 Initialization

At power-on or other hardware reset (WDT and etc), AIC is disabled. Software must initiate AIC and the internal CODEC after power-on or reset. If errors found in data transferring, or in other places, software must initial AIC and optional, the internal CODEC. Here is the initial flow.

1. Select internal CODEC (AICFR.ICDC).
2. If I2S/MSB-Justified is selected, select between I2S and MSB-Justified (I2SCR.AMSL).
3. Decide BIT_CLK direction (AICFR.BCKD) and SYNC direction (AICFR.SYNCD).
4. If BIT_CLK is configured as output, BIT_CLK divider I2SDIV.DV must be set to what correspond with the values as shown in 6.5.2.6. And the clock selection and the divider between PLL clock out and AIC also must be set (CFCR.I2S and I2SCDR in CPM). Enable AIC by write 1 to AICFR.ENB.
5. If it needs to reset AIC registers and flush FIFOs, write 1 to AICFR.RST. If it need only flush FIFOs, write 1 to AICCR.FLUSH. BIT_CLK must exist here and after.
6. In case of internal CODEC with I2S/MSB-Justified format, configure I2S/MSB-justified CODEC via the control bus connected to the CODEC, for instance I2C or L3, depends on CODEC. If the resettlement without involving I2S/MSB-justified CODEC or ADC/DAC function changing, this step can be skip.

6.6.3 Internal CODEC Registers Access Operation

The internal audio CODEC can be configured/controlled by its internal registers. To access these registers, an I2S/MSB-justified CODEC usually employs L3 bus, SPI bus, I2C bus or other control bus. The L3 bus operation can be emulated by software by using 3 GPIO pins of the chip.

6.6.4 Audio Replay

Outgoing audio sample data (from AIC to CODEC) is written to AIC transmit FIFO from processor via store instruction or from memory via DMA. AIC then takes the data from the FIFO, serializes it, and sends it over the serial wire ADC_SDATA to an internal CODEC or over an internal wire to an internal CODEC.

The audio transmission is enabled automatically when the AIC is enabled by set AICFR.ENB. But all replay data is zero at this time except both of the following conditions are true:

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1 AICCR.ERPL must be 1. If AICCR.ERPL is 0, value of zero is send to CODEC even if there are samples in transmit FIFO.
2 At least one audio sample data in the transmit FIFO. If the transmit FIFO is empty, value of zero or last sample depends on AICFR.LSMP, is send to CODEC even if AICCR.ERPL is 1.

Here is the audio replay flow:

1 Configure the CODEC as needed.
2 Configure sample size by AICCR.OSS.
3 Configure sample channels (AICCR.CHANNEL).
4 If sample size is configured 16 bit, select packed or unpacked mode (AICCR.PACK16).
5 If two channels is configured, select the right-channel-first sample data or not (I2SCR.RFIRST).
6 If two channels is configured, select the sample data switched or not (I2SCR.SWLH).
7 Configure sample rate by clock dividers (for I2S/MSB-Justified format with BIT_CLK is provided internally) or by CODEC registers (for BIT_CLK provided by internal CODEC).
8 Some other configurations: mono to stereo, endian switch, signed/unsigned data transfer, transmit FIFO configuration, play ZERO or last sample when TX FIFO under-run, and etc.
9 Write 1 to AICCR.ERPL.
It is suggested that at least a frame of PCM data is pre-filled in the transmit FIFO to prevent FIFO under-run flag (AICSR.TUR).
Fill sample data to the transmit FIFO. Repeat this till finish all sample data. In this procedure, please control the FIFO to make sure no FIFO under-run and other errors happen. When the transmit FIFO under-run, noise or pause may be heard in the audio replay, AICSR.TUR is 1, and if AICCR.ETUR is 1, AIC issues an interrupt. Please reference to 6.6.6 for detail description on FIFO.
10 Waiting for AICSR.TFL change to 0. So that all samples in the transmit FIFO has been replayed, then we can have a clean start up next time.
11 Write 0 to AICCR.ERPL.

6.6.5 Audio Record

Incoming audio sample data (from CODEC to AIC) is received from DAC_SDATA (for an internal CODEC) serially and converted to parallel word and stored in AIC receive FIFO. Then the data can be taken from the FIFO to processor via load instruction or to memory via DMA.

The audio recording is enabled automatically when the AIC is enabled by set AICFR.ENB. But all received data is discarded at this time except both of the following conditions are true:

1 AICCR.EREC must be 1. If AICCR.EREC is 0, the received data is discarded even if there are rooms in the receive FIFO.
2 At least one room left in the receive FIFO. If the receive FIFO is full, the received data is discarded even if AICCR.EREC is 1.

Here is the audio record flow:

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1 Configure the CODEC as needed.
2 Configure sample size by AICCR.ISS.
3 Configure sample rate by clock dividers (for I2S/MSB-Justified format with BIT_CLK is provided internally) or by CODEC registers (for BIT_CLK provided by internal CODEC).
4 Some other configurations: signed/unsigned data transfer, receive FIFO configuration, and etc.
5 Write 1 to AICCR.EREC. Make sure there are rooms available in the receive FIFO before set AICCR.EREC. Usually, it should empty the receive FIFO by fetch data from it before set AICCR.EREC.
6 Take sample data form the receive FIFO. Repeat this till the audio finished. In this procedure, please control the FIFO to make sure no FIFO over-run and other errors happen. When the receive FIFO over-run, same recorded audio samples will be lost, AICSR.ROR is 1, and if AICCR.EROR is 1, AIC issues an interrupt. Please reference to 6.6.6 for detail description on FIFO. Write 0 to AICCR.EREC.
7 Take sample data from the receive FIFO until AICSR.RFL change to 0. So that all samples in the receive FIFO has been taken away, then we can have a clean start up next time. When the receive FIFO is empty, read from it returns zero.

6.6.6 FIFOs operation

AIC has two FIFOs, one for transmit audio sample and one for receive. All AIC played/recorded audio sample data is taken from/send to transmit/receive FIFOs. The RX FIFO is in 24 bits width and 32 entries depth, one entry for keeping one audio sample regardless of the sample size. The RX FIFO is in 32 bits width and 64 entries depth, one entry for keeping one audio sample regardless of the sample size, but in 16 bits packed mode, one entry for keeping two audio samples. AICDR.DATA provides the access point for processor/DMA to write to transmit FIFO and read from receive FIFO. One time access to AICDR.DATA process one sample. The sample data should be put in LSB (Least Significant Bit) in memory or processor registers. For transmitting, bits exceed sample are discarded. For receiving, these bits are set to 0. Figure 6-7 illustrates the FIFOs access.

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Figure 6-7 Transmitting/Receiving FIFO access via APB Bus

The software and bus initiator must guarantee the right sample placement at the bus.

In case of DMA bus initiator, one 24, 20, 18 bits audio sample must occupies one 32-bits word in memory, so 32-bits width DMA must be used. One 16 bits sample occupies one 16-bits half word in memory, so 16-bits width DMA must be used. One 8-bits sample occupies one byte in memory, and use 8-bits width DMA except 16bits packed mode. If in 16 bits packed mode, Two 16 bits sample occupies one 32-bits word in memory, so 32-bits width DMA must be used.

In case of processor bus initiator, any type of the audio sample must occupy one CPU general-purpose register at LSB, and read/write from/to AICDR.DATA with 32-bits load/store instruction. When process small sample size, 16-bits or 8-bits, software may need to do the data pack/unpack except 16 bits packed mode. In the 16bits packed mode, the sample data is packed, and two 16 bits audio samples occupy one CPU general-purpose register.

The AICFR.TFTH and AICFR.RFTH are used to set the FIFO level thresholds, which are the trig levels of DMA request and/or FIFO service interrupt. The AICFR.TFTH and AICFR.RFTH should be set to proper value; too small or too big are not good. When AICFR.RFTH is too small, or AICFR.TFTH is too big, the DMA burst length or the number of sample can be processed by processor is too small, which harms the bus or processor efficiency. When AICFR.RFTH is too big or AICFR.TFTH is too small, the

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bus or the interrupt latency left for under-run/over-run is too small, which may causes replay/record errors.

AICSR.TUR is set to 1 during transmit under-run conditions. If AICCR.ETUR is 1, this can trigger an interrupt. During transmit under-run conditions, zero or last sample is continuously sent out across the serial link. Transmit under-run can occur under the following conditions:

1 Valid transmit data is still available in memory, but the DMA controller/processor starves the transmit FIFO, as it is busy servicing other higher-priority tasks.
2 The DMA controller/processor has transferred all valid data from memory to the transmit FIFO.

AICSR.ROR is set to 1 during receive over-run conditions. If AICCR.EROR is 1, this can trigger an interrupt. During receive over-run conditions, data sent by the CODEC is lost and is not recorded.

When replay/record two channels data, the left channel is default the first data in FIFOs and in the serial link. In 16bits packed mode, could configure that the left channel is the first data or the right channel. By default, the 16 bits LSB is left channel, 16 bits MSB is the right channel. But it also could be switched the Left or the Right channel (I2SCR.SWLH).

6.6.7 Data Flow Control

There are three approaches provided to control/synchronize the audio incoming/outgoing data flow.

6.6.7.1 Polling and Processor Access

AICSR.RFL and AICSR.TFL reflect how many samples exist in receiving and transmitting FIFOs. Through read these register fields, processor can detect when there are samples in receiving FIFO in audio record and then load them from the RX-FIFO, and when there are rooms in transmitting FIFO in audio replay and then store samples to the TX-FIFO.

Polling approach is in very low efficiency and is not recommended.

6.6.7.2 Interrupt and Processor Access

Set proper values to AICFR.TFTH and AICFR.RFTH, the FIFO interrupts trig thresholds. Set AICCR.ETFS and/or AICCR.ERFS to 1 to enable transmitting and/or receiving FIFO level trigger interrupts. When the interrupt found, it means there are rooms or samples in the TX or RX FIFO, and processor can store or load samples to or from the FIFO.
Interrupt approach is more efficient than polling approach.

6.6.7.3 DMA Access

Audio data is real time stream, though it is in low data bandwidth, usually less than 1.2Mbps. DMA approach is the most efficient and is the recommended approach.

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To enable DMA operation, set AICCR.TDMS and AICCR.RDMS to 1 for transmit and receive respectively. It also needs to allocate two channels in DMA controller for data transmitting and receiving respectively. Please reference to the processor's DMA controller spec for the details.

The AICFR.TFTH and AICFR.RFTH are used to set the transmitting and receiving FIFO level thresholds, which determine the issuing of DMA request to DMA controller. To respond the request, DMAC initiator and controls the data movement between memory and TX/RX FIFO.

6.6.8 Audio Samples format

6.6.8.1 16 bits packed mode

One channel (mono) mode and two channels (stereo) mode:

Figure 6-8 One channel (Left) and Two channels (right) mode (16 bits packed mode)

Four channels mode and six channels mode:

Figure 6-9 Four channels (Left) and Six channels (right) mode (16 bits packed mode)

Eight channels mode:

Figure 6-10 Eight channels mode (16 bits packed mode)

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6.6.8.2 Normal mode

One channel (Mono) and two channels (stereo) mode:

Figure 6-11 One channel (Left) and Two channels (right) mode

Four channels mode and six channels mode:

Figure 6-12 Four channels (Left) and Six channels (right) mode

Eight channel mode:

Figure 6-13 Eight channels mode

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7 Codec

7.1 Overview

Video Codec is a low power, high resolution. The ADC, DAC and power amplifier are integrated to provide total solutions . With 24 bits resolution for DAC and 24 bits resolution for ADC, Audio Codec is suitable for applications in high and consumer digital audio systems, automobile audio multimedia and digital systems.

7.2 Features

- 24 bits DAC with 93dB SNR
- 24 bits ADC with 92dB SNR
- Support signal-ended and differential microphone input and line input
- Automatic Level Control (ALC) for smooth audio recording
- Pure logic process: no need for mixed signal layers and less mask cost
- Programmable input and output analog gains
- Digital interpolation and decimation filter integrated
- Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K

7.3 Block Diagram

Figure 7-1 Codec Block Diagram

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7.4 Data Format Description

The Codec support I2S stand mode and Left Justified mode.

7.4.1 I2S mode

For I2S mode, the data format is depicted in Figure 7-2.The MSB becomes available at the second rising edge of sck when ws transition is done. The other valid bits up to the LSB are transmitted in order. Due to varied word length, different sck frequency and sample rate ,some unused sck cycles may appear between the LSB of the current sample and the MSB of the next one, Which means the data in this period can be ignored.

Figure 7-2 I2S mode

7.4.2 Left Justified mode

For Left Justified mode，the data format is illustrated in Figure 7-3. The MSB is valid at the first rising edge of sck when ws transition is done. The other valid bits up to the LSB are transmitted sequentially. Due to varied word length, different sck frequency and sample rate, some unused sck cycles may appear before every transition, which means the data in this period can be ignored.

Figure 7-3 Left Justified mode

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7.5 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   RC- Read only, and Clear to 0 by read
   RS- Read only, and Set to 1 by read
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

7.5.1 Register Memory Map

Table 7-1 Registers Memory Map Base Address

Name	Base	Description
Codec	0x10021000	Address base of Codec

The Codec is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 7-2 Codec Registers Map

Name	RW	Reset Value	Address Offset	Access Size
CGR	RW	0x0000_0003	0x0000	32
CACR	RW	0x0000_0050	0x0008	32
CMCR	RW	0x0000_000E	0x000C	32
CDCR1	RW	0x0000_0050	0x0010	32
CDCR2	RW	0x0000_000E	0x0014	32
CADR	RW	0x0000_0000	0x001C	32
CGAINR	RW	0x0000_0000	0x0028	32
CASR	RW	0x0000_0000	0x0034	32
CDPR	RW	0x0000_0003	0x0038	32
CDDPR2	RW	0x0000_00FF	0x003C	32
CDDPR1	RW	0x0000_00E0	0x0040	32

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CDDPR0	RW	0x0000_0000	0x0044	32
CAACR	RW	0x0000_0000	0x0084	32
CMICCR	RW	0x0000_0000	0x0088	32
CAC2R	RW	0x0000_000C	0x008C	32
CAMPCR	RW	0x0000_0000	0x0090	32
CAR	RW	0x0000_0000	0x0094	32
CHR	RW	0x0000_0000	0x0098	32
CHCR	RW	0x0000_0040	0x009C	32
CCR	RW	0x0000_001E	0x00A0	32
CMR	RW	0x0000_0000	0x0100	32
CTR	RW	0x0000_0046	0x0104	32
CAGCCR	RW	0x0000_0041	0x0108	32
CPGR	RW	0x0000_002C	0x010C	32
CSRR	RW	0x0000_0000	0x0110	32
CALMR	RW	0x0000_0026	0x0114	32
CAHMR	RW	0x0000_0040	0x0118	32
CALMINR	RW	0x0000_0036	0x011C	32
CAHMINR	RW	0x0000_0020	0x0120	32
CAFR	RW	0x0000_0038	0x0124	32
CCAGVR	R	0x0000_000C	0x0130	32

7.5.2 Register and Fields Description

7.5.2.1 Codec Global Register(CGR,0x0000)

	CGR																															BASE+0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								bsten	Reserved					dcrst	srst
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	bsten	Inner-Bist wave generated model enable signal 1:Enable 0:disable	RW
6:2	Reserved	Writing has no effect. Read as zero.	R
1	dcrst	Codec Digital Core Reset. This reset only reset the codec data path. Low valid. 0:Reset 1:Work	RW

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0	srst	Codec system reset. This signal will reset the registers which control all the digital and analog part.	RW

7.5.2.2 Codec ADC Control Register(CACR,0x0008)

	CACR																															BASE+0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								adcen	adcvaldalength		I2smode		Reserved	adcswap	adcintf
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	adcen	The enable signal to control the I2S LRC Polarity of the ADC interface 1:Enable 0:disable	RW
6:5	adcvaldaleng th	Choose the valid data length in one 1/2 Frame of ADC I2S interface 00:16Bits 01:20Bits 10:24Bits	RW
4:3	I2smode	Choose I2S mode of ADC I2S interface 01:Left Justified Mode 10:I2S mode	RW
2	Reserved	Writing has no effect. Read as zero	R
1	adcswap	The enable signal to swap the left-right channel data of the ADC I2S interface 1:Enable the swap 0:keep the current state	RW
0	adcintf	Choose the type of ADC I2S interface 0:Stereo 1:Mono	RW

7.5.2.3 Codec Mode Control Register(CMCR,0x000C)

	CMCR																															BASE+0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										masteren	adcdacmaster	adcdalength		adci2srst	align
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

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Bits	Name	Description	RW
31:6	Reserved	Writing has no effect. Read as zero.	R
5	Masteren	Choose the input or output direction of the pin which is related to I2S Mode 0:Input(I2S slave Mode) 1:Output(I2S master Mode)	RW
4	adcdacmaster	Choose the input or output direction of the ADC and DAC i2s interface 0:Slave Mode 1:Master Mode	RW
3:2	adcdalength	Choose the data length in one 1/2 Frame of ADC I2S interface 00:16Bits 01:20Bits 10:24Bits 11:32Bits Relate CACR[4:3]	RW
1	adci2srst	The reset signal of the ADC I2S mode 1:Keep the current state 0:Reset	RW
0	align	Change the phase relationship between the pin_adc_sd_o and pin_sck_o 0:Falling edge aligns 1:Rising edge aligns	RW

7.5.2.4 Codec DAC Control Register1(CDCR1,0x0010)

	CDCR1																															BASE+0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								dacen	dacvaldalength		I2smode		dacswap	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

Bits	Name	Description	RW
1:0	Reserved	Writing has no effect. Read as zero.	R
7	dacen	The enable signal to control the I2S LRC Polarity of the DAC interface	RW

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		1:Enable 0:disable	
6:5	dacvaldalength	Choose the valid data length in one 1/2 Frame of DAC I2S interface 00:16Bits 01:20Bits 10:24Bits	RW
4:3	I2smode	Choose I2S mode of DAC I2S interface 01:Left Justified Mode 10:I2S mode	RW
2	adcswap	The enable signal to swap the left-right channel data of the ADC I2S interface 1:Enable the swap 0:keep the current state	RW
1:0	Reserved	Writing has no effect. Read as zero.	R

7.5.2.5 Codec DAC Control Register2(CDCR2,0x0014)

	CDCR2																															BASE+0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												dacdalength		daci2srst	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect. Read as zero.	R
3:2	dacdalength	Choose the data length in one 1/2 Frame of DAC I2S interface 00:16Bits 01:20Bits 10:24Bits 11:32Bits Relate CACR[4:3]	RW
1	daci2srst	The reset signal of the DAC I2S mode 1:Keep the current state 0:Reset	RW
0	Reserved	Writing has no effect. Read as zero.	R

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7.5.2.6 Codec ADC DAC Register(CADR,0x001C)

	CADR																																BASE+0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											adcloopdac	dacin	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4	adcloopdac	The enable signal of ADC to DAC loops 1:Enable 0:Disable	RW
3	dacin	Choose the input of DAC channel 1:using the register to control the input data of DAC channel 0:Normal data Note: When we choose this register to control the input data of the DAC channel, we can use the register	RW
2:0	Reserved	Writing has no effect. Read as zero.	R

7.5.2.7 Codec Gain Register(CGAINR,0x0028)

	CGR																																BASE+0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										gainen	Reserved				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect. Read as zero.	R
5	gainen	Enable the function that uses the ALCL module to control the gain of the PGAL 1:Enable 0:Disable	RW

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4:0	Reserved	Writing has no effect. Read as zero.	R

7.5.2.8 Codec Audio Source Register(CASR,0x0034)

	CASR																															BASE+0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								daclechsrc		Reserved		adclechsrc		Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:6	daclechsrc	Choose the digital audio source of DAC left channel 00:Choose the I2S left channel as the digital audio source 01:Choose the sine wave generated by the inner-bist module 10:Choose the square wave generated by the inne-bist module 11:24'h0 as the digital audio source. Note: please keep the default value	RW
5:4	Reserved	Writing has no effect. Read as zero.	R
3:2	gainen	Choose the digital audio source of ADC left channel 00:Choose the I2S left channel as the digital audio source 01:Choose the sine wave generated by the inner-bist module 10:Choose the square wave generated by the inner-bist module 11:24'h0 as the digital audio source. Note: please keep the default value	RW
1:0	Reserved	Writing has no effect. Read as zero.	R

7.5.2.9 Codec Data Path Register(CDPR,0x0038)

	CDPR																															BASE+0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								adcdatapath		Reserved		adcdatain	Reserved	dacindebug3	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

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Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:6	adcdatapath	Configure the input of the ADC data path when the CDPR. adcdatain is 1 Note: please keep the default value	RW
5:4	Reserved	Writing has no effect. Read as zero.	R
3	adcdatain	Select the input of the ADC data path 1:Select the register CDPR. adcdatapath as the input of ADC data path 0:Select the normal path as the input of the ADC data path Note: please keep the default value	RW
2	Reserved	Writing has no effect. Read as zero.	R
1:0	dacindebug3	Configure the bit [25:24] when we choose the register value as the input of DAC channel Please reference the description of CADR. dacin	

7.5.2.10 Codec DAC Data Path Register2(CDDPR2,0x003C)

	CDDPR2																															BASE+0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								Dacindebug2							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	dacindebug2	Configure the bit [23:16] when we choose the register value as the input of DAC channel Please reference the description of CADR. dacin	RW

7.5.2.11 Codec DAC Data Path Register1(CDDPR1,0x0040)

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	CDDPR1																															BASE+0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								Dacindebug1							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	dacindebug2	Configure the bit [15:8] when we choose the register value as the input of DAC channel Please reference the description of CADR. dacin	RW

7.5.2.12 Codec DAC Data Path Register0(CDDPR0,0x0044)

	CDDPR0																															BASE+0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								Dacindebug0							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	Dacindebug0	Configure the bit [7:0] when we choose the register value as the input of DAC channel Please reference the description of CADR. dacin	RW

7.5.2.13 Codec ADC Analog Control Register(CAACR,0x0084)

	CACCR																															BASE+0x0084
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								adcsrcen	Micbiasen	adczeroen	Reserved		Micbaisctr		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	adcsrcen	The enable signal of current source for ADC 0:Stop Working 1:Work	R
6	Micbiasen	The enable signal of MIC bias voltage (MICBIAS) buffer 0:Stop Working 1:Work	RW
5	adczeroen	The enable signal of the ADC input zero-crossing detection module 0:Stop Working, output 0 electrical level 1:Work	RW
4:3	Reserved	Writing has no effect. Read as zero.	R
2:0	Micbaisctr	The level range control signal of MIC bias voltage 000:1.0*VREF 111:1.7*VREF Step:0.1*VREF VREF=AVDD/2	RW

7.5.2.14 Codec Mic Control Register(CMICCR,0x0088)

	CMICCR																															BASE+0x0088
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									Micen	Micgain	Micmute	Reserved		Alcen	Alcmute
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6	Micen	The enable signal of MIC module 1:Work 0:Stop work	RW
5	Micgain	The gain control of MIC module 1:20dB 0:0dB	RW
4	Micmute	The mute signal of MIC module 0:Mute 1:Work	RW

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3:0	Reserved	Writing has no effect. Read as zero.	R
5	Alcen	The enable signal of ALC module 1:Work 0:Stop work	RW
4	Alcmute	The mute signal of ALC module 0:Mute 1:Work	RW

7.5.2.15 Codec ALC Control Register2(CACR2,0x008C)

	CACR2																															BASE+0x008C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Micsel	Alcgain				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect. Read as zero.	R
5	Alcsel	The signal to select the input module of ALC module 1:Signal-ended input 0:Full differential input	RW
4:0	Alcgain	The gain control of ALC gain 00000: -18dB 01100: 0dB 11111: 28.5dB Step: 1.5dB	RW

7.5.2.16 Codec Amplifier Control Register(CAMPCR,0x0090)

	CAMPCR																															BASE+0x0090
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								adcrefvolen	adcclken	adclampen	adclrst	Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	adcrefvolen	The enable signal of reference Voltage buffer for left ADCL PATH 1:Stop Working 0:Work	RW
6	adclclken	The enable signal of CLOCK for ADCL module 1:Set to logic "1" 0:Work	RW
5	adclampen	The enable signal of Amplifier in ADCL module 0:Stop Working all amplifier 1:Work	RW
4	adclrst	The reset signal of different levels integrator in ADCL module 0:Work 1:Clear	RW
3:0	Reserved	Writing has no effect. Read as zero.	R

7.5.2.17 Codec Audio Register(CAR,0x0094)

	CAR																															BASE+0x0094
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								detdacshort	audiodacen	dacrefvolen	Reserved	dacrefvolen	dacclken	dacen	dacinit
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	Detdacshort	The enable signal which is used to detect the short between the DAC output and Ground 0:Enable 1:Disable	RW
6	Audiodacen	The enable signal of reference Voltage buffer for AUDIO DAC 0:Stop working 1:Work	RW
5	Dacrefvolen	The enable signal of reference Voltage buffer for DAC PATH	RW
4	Reserved	Writing has no effect. Read as zero.	R

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3	dacrefvolen	The enable signal of reference Voltage buffer for left DAC module 1:Stop Working 0:Work	RW
2	daclclken	The enable signal of CLOCK for DAC module 1:Set to logic "1" 0:Work	RW
1	dacen	The enable signal of DAC module 0:Stop Work 1:Work	RW
0	dacinit	The initial signal of DAC module 0:Initialization 1:Work	RW

7.5.2.18 Codec HPOUT Register(CHR,0x0098)

	CHR																															BASE+0x0098
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								hpouten	hpoutinit	hpoutmute	Reserved				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	hpouten	The enable signal of HPOUT module 0:Stop Work 1:Work	RW
6	hpoutinit	The initial signal of HPOUT module 0:Initialization 1:Work	RW
5	hpoutmute	The mute signal of HPOUT module 0:Mute 1:Work	RW
4:0	Reserved	Writing has no effect. Read as zero.	R

7.5.2.19 Codec HPOUT Control Register(CHCR,0x009C)

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	CHCR																															BASE+0x009C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								hpoutpop		Reserved	hpoutgain				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
7:6	hpoutpop	The POP Sound Control signal of the HPOUT module 01:Precharge(or discharge) 10:Work	RW
5	Reserved	Writing has no effect. Read as zero.	R
4:0	hpoutgain	The signal to select gain of HPOUT module 00000: -39dB 11010: 0dB 11111: 6dB Step: 1.5dB	RW

7.5.2.20 Codec Charge Register(CCR,0x00A0)

	CCR																															BASE+0x00A0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								dacprecharge	chargeselect						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	dacprecharg e	The control signal of the precharge for Codec DAC 0:Precharge 1:Discharge	RW
6:0	chargeselect	The signal to select current to precharge for Codec Bit6: 0: Choose the current I_0 1: Don't choose the current I_0 Bit5: 0: Choose the current $1.5*I_0$ 1: Don't choose the current $1.5*I_0$ Bit4: 0: Choose the current $2*I_0$	RW

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		1: Don't choose the current 2*I_0 Bit3: 0: Choose the current 3*I_0 1: Don't choose the current 3*I_0 Bit2: 0: Choose the current 5*I_0 1: Don't choose the current 5*I_0 Bit1: 0: Choose the current 15*I_0 1: Don't choose the current 15*I_0 Bit0: 0: Choose the current 30*I_0 1: Don't choose the current 30*I_0	

7.5.2.21 Codec Method Register(CMR,0x0100)

	CMR																															BASE+0x0100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									gainmethod	ctrmethod		gainholdtime			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6	gainmsthod	Choose the method to control the gain attack 0: Normal way 1: Jack way	RW
5:4	ctrmsthod	There are for method to generate the control signal 00: Normal way 01: Jack way 1 10: Jack way 2 11: Jack way 3 This register is used to choose the method to generate the control signals according to the actual situation	RW
3:0	gainholdtime	AGC hold time before gain is increased in normal mode **Configure** / **Hold time(ms)** / **Configure** / **Hold time(ms)** 0000 / 0 / 0110 / 64 0001 / 2 / 0111 / 128 0010 / 4 / 1000 / 256 0011 / 8 / 1001 / 512 0100 / 16 / 1010 / 1000 0101 / 32 / 1011~1111 / 0	RW

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7.5.2.22 Codec Time register(CTR,0x0104)

	CTR																															BASE+0x0104
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								decaytime				attacktime			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:8</td><td>Reserved</td><td>Writing has no effect.
Read as zero.</td><td>R</td></tr>
<tr><td>7:4</td><td>decaytime</td><td>Decay(gain ramp-up) time
<table>
<tr><th colspan="4">Normal MODE(reg_agc_mode=0)</th></tr>
<tr><th>Configure</th><th>Hold time(ms)</th><th>Configure</th><th>Hold time(ms)</th></tr>
<tr><td>0000</td><td>0.5</td><td>0110</td><td>32</td></tr>
<tr><td>0001</td><td>1</td><td>0111</td><td>64</td></tr>
<tr><td>0010</td><td>2</td><td>1000</td><td>128</td></tr>
<tr><td>0011</td><td>4</td><td>1001</td><td>256</td></tr>
<tr><td>0100</td><td>8</td><td>1010</td><td>512</td></tr>
<tr><td>0101</td><td>16</td><td>1011~1111</td><td>512</td></tr>
</table>
<table>
<tr><th colspan="4">Limter MODE(reg_agc_mode=1)</th></tr>
<tr><th>Configure</th><th>Hold time(ms)</th><th>Configure</th><th>Hold time(ms)</th></tr>
<tr><td>0000</td><td>0.125</td><td>0110</td><td>8</td></tr>
<tr><td>0001</td><td>0.25</td><td>0111</td><td>16</td></tr>
<tr><td>0010</td><td>0.5</td><td>1000</td><td>32</td></tr>
<tr><td>0011</td><td>1</td><td>1001</td><td>64</td></tr>
<tr><td>0100</td><td>2</td><td>1010</td><td>128</td></tr>
<tr><td>0101</td><td>4</td><td>1011~1111</td><td>128</td></tr>
</table></td><td>RW</td></tr>
<tr><td>3:0</td><td>attacktime</td><td>Attack(gain ramp-down) time
<table>
<tr><th colspan="4">Normal MODE(reg_agc_mode=0)</th></tr>
<tr><th>Configure</th><th>Hold time(ms)</th><th>Configure</th><th>Hold time(ms)</th></tr>
<tr><td>0000</td><td>0.125</td><td>0110</td><td>8</td></tr>
<tr><td>0001</td><td>0.25</td><td>0111</td><td>16</td></tr>
<tr><td>0010</td><td>0.5</td><td>1000</td><td>32</td></tr>
<tr><td>0011</td><td>1</td><td>1001</td><td>64</td></tr>
<tr><td>0100</td><td>2</td><td>1010</td><td>128</td></tr>
<tr><td>0101</td><td>4</td><td>1011~1111</td><td>128</td></tr>
</table></td><td>RW</td></tr>
</table>

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			Normal MODE(reg_agc_mode=1)					
			Configure	**Hold time(ms)**	**Configure**	**Hold time(ms)**		
			0000	0.032	0110	2		
			0001	0.064	0111	4		
			0010	0.125	1000	8		
			0011	0.25	1001	16		
			0100	0.5	1010	32		
			0101	1	1011~1111	0.032		

7.5.2.23 Codec AGC Control Register(CAGCCR,0x0108)

	CAGCCR																															BASE+0x0108
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								agcmode	agczeroen	ampmode	fastdecr	agcnoisegate	cnoisethd		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	agcmode	Determines the AGC mode of operation 0: AGC mode 1: Limiter mode	RW
6	agczeroen	AGC users zero cross enable 0: Disable 1: Enable, the AGC gain will update at zero cross enable	RW
5	ampmode	When in the limiter mode, the low amplitude signal will recovery in two modes 0: The gain will recovery to the value of the reg_pga_lvol 1: The gain will recovery to the gain at the moment when the mode changes from AGC to Limiter	RW
4	fastdecr	When the amplitude of the signal is more than 87.5% of full scale, use this signal to control the fast decrement: 0: Disable 1: Enable	RW
3	agcnoisegate	AGC noise gate function enable: 0:Disable 1:Enable	RW
2:0	noisethd	AGC noise gate threshold:	RW

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			Configuration	**Threshold**	**Configuration**	**Threshold**		
			000	-39dB				
			001	-45dB				
			010	-51dB				
			011	-57dB				

7.5.2.24 Codec PGA Gain Register(CPGR,0x010C)

	CPGR																															BASE+0x010C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										pgalezeroen	pgalegain				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect. Read as zero.	R
5	pgalezeroen	Left channel input PGA zero cross enable: 0: Update gain when gain register change 1: Update gain 1st zero cross after gain register write	RW
4:0	pgalegain	Left channel input PGA gain **Configuration** / **GAIN** / **Configuration** / **GAIN** 00000 / -18dB / 01101 / +1.5dB 00001 / -16.5dB / 01110 / +3dB ... / ... / ... / ... 01100 / 0dB / 11111 / +28.5dB	RW

7.5.2.25 Codec Sample Rate Register(CSRR,0x0110)

	CSRR																															BASE+0x0110
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												slowclken	samplerate		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:4	Reserved	Writing has no effect. Read as zero.	R
3	slowclken	Slow clock enabled, used for the zero cross timeout	RW
2:0	samplerate	Left channel input PGA gain	RW

Configuration	Sample rate	Configuration	Sample rate
000	96K	100	24K
001	48K	101	16K
010	44.1K	110	12K
011	36K	111	8K

7.5.2.26 Codec AGC Low Maximum Register(CALMR,0x0114)

	CALMR																															BASE+0x0114
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								agclowmax							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	agclowmax	The Low 8bits of the AGC maximum level	RW

7.5.2.27 Codec AGC High Maximum Register(CAHMR,0x0118)

	CAHMR																															BASE+0x0118
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								agchighmax							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	agchighmax	The High 8bits of the AGC maximum level	RW

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7.5.2.28 Codec AGC Low Minimum Register(CALMINR,0x011C)

	CAHMINR																															BASE+0x011C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								agclowmin							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	agclowmin	The Low 8bits of the AGC maximin level	RW

7.5.2.29 Codec AGC High Minimum Register(CAHMINR,0x0120)

	CAHMINR																															BASE+0x0120
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								agchighmin							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	agchighmin	The High 8bits of the AGC maximin level	RW

7.5.2.30 Codec AGC Function Register(CAFG,0x0124)

	CAFG																															BASE+0x0124
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									agcfunsel	pgamaxgain			pgamingain		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

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Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6	agcfunsel	AGC function select 0: AGC function off 1: AGC function on	RW
5:3	pgamaxgain	Set maximum gain of PGA **Configuration** / **Max gain** / **Configuration** / **Max gain** 000 / -13.5dB / 100 / +10.5dB 001 / -7.5dB / 101 / +16.5dB 010 / -1.5dB / 110 / +22.5dB 011 / +4.5dB / 111 / +28.5dB	RW
2:0	pgamaxgain	Set minimum gain of PGA **Configuration** / **Max gain** / **Configuration** / **Max gain** 000 / -18dB / 100 / +6dB 001 / -12dB / 101 / +12dB 010 / -6dB / 110 / +18dB 011 / 0 / 111 / +24dB	

7.5.2.31 Codec Current AGC Gain Value Register(CCAGVR,0x0130)

	CCAGVR																													BASE+0x0130				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											agcgainvalue				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4:0	agcgainval	It shows the current value of the agc gain value. When the agc function is disable, this value is 0x0C	R

7.6 Operation Flow

This chapter will give some reference register configurations about how to power up/off Codec, make the codec in the stand by state and how to control the DAC, ADC, AGC.

Note: The every configurations step is better to keep more than 10ms.

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7.6.1 POWER UP

Step1: Supply the power of the digital part and reset the Audio Codec

Step2: Configure the register CHCR[7:6] to 2'b01

Step3: Configure the register CCR[7] to 0 to enable the precharge function

Step4: Configure the register CCR[6:0] to 7'b011_1111 and then change the register CCR[6:0] from 7'b011_1111 to 7'b000_0000 step by step. **The suggestion slot time of the step is 20ms**

Step5: Wait until the voltage of VCM keeps stable at the AVDD/2

Step6: Configure the register CCR[6:0] to choose a small current to decrease the power consumption

7.6.2 POWER OFF

Step1: Keep the power on and disable the ADC and DAC according to the description of section 1.7.4 and 1.7.6

Step2: Configure the register CHCR[7:6] to 2'b01

Step3: Configure the register CCR[6:0] to 7'b011_1111

Step4: Configure the register CCR[7] to 1 to begin to discharge

Step5: Configure the register CCR[6:0] . Then change the register CCR[6:0] from 7'b011_1111 to 7'b000_0000 step by step. **The suggestion slot time of the step is 20ms**

Step6: Wait until the voltage of VCM keep stable at AGND

Step7: Power off the analog power supply

Step8: Power off the digital power supply

7.6.3 ENABLE DAC

Step1: Power up the Codec according to the section1.7.1 and input the mute signal

Step2: Set the register CAR[6] to 1 to enable the current source of Codec DAC

Step3: Set the register CAR[6] to 1 to enable the reference voltage buffer of left DAC path

Step4: Set the register CHCR[7:6] to 2'b10 to enable the POP sound control signal of HPOUTL module

Step5: Set the register CAR[3] to 1 to enable the high and low reference voltage buffer of DACL module

Step6: Set the register CAR[2] to 1 to enable the clock module of DACL module

Step7: Set the register CAR[1] to 1 to enable the DACL module

Step8: Set the register CAR[0] to 1 to initial the DACL module

Step9: Set the register CHR[7] to 1 to enable the HPOUTL

Step10: Set the register CHR[6] to 1 to initial the HPOUTL

Step11: Set the register CHR[5] to 1 to disable the mute signal of HPOUTL module

Step12: Set the register CHCR[4:0] to select the gain of HPOUTL module

Step13: Input the music

7.6.4 DISABLE DAC

Step1: Keep the DAC work and input the mute signal

Step2: Set the register CHCR[4:0] to select the gain of HPOUTL module

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Step3: Set the register CHR[5] to 0 to enable the mute signal of HPOUTL module
Step4: Set the register CHR[6] to 0
Step5: Set the register CHR[7] to 0
Step6: Set the register CAR[1] to 0
Step7: Set the register CAR[2] to 0
Step8: Set the register CAR[3] to 0
Step9: Set the register CHCR[7:6] to 2'b01
Step10: Set the register CAR[5] to 0
Step11: Set the register CAR[6] to 0
Step12: Set the register CAR[0] to 0

7.6.5 ENABLE ADC

Step1: Power up the Codec according to the section1.7.1
Step2: Set the register CACR2[5] to choose the input mode of single-ended or full differential mode
Step3: Set the register CAACR[7] to 1 to enable the current source of ADC module
Step4: Set the register CAACR[6] to 1 to enable the MIC bias voltage buffer
Step5: Set the register CAACR[2:0] to choose the level range of MIC bais voltage
Step6: Set the register CAMPCR[7] to enable the reference voltage of ADCL path
Step7: Set the register CMICCR[6] to 1 to enable the BST_L module
Step8: Set the register CMICCR[5] to 1 to enable the ALCL module
Step9: Set the register CAMPCR[6] to enable the clock module of ADCL module
Step10: Set the register CAMPCR[6] to enable the amplifier of ADCL module
Step11: Set the register CMICCR[1] to 1 to make the ALCL in work state
Step12: Set the register CMICCR[4] to 1 to make the BST_L module in work state
Step13: Set the register CAACR[5] to 1 to enable the zero-crossing detect function of ADCL
Step14: Set the register CACR2[4:0] to choose the gain of ALC_L module
Step15: Set the register CMICCR[5] to choose the gain of BST_L module
Step16: Input the music
Step17: Begin to record and judge the valid channel

7.6.6 DISABLE ADC

Step1: Stop to recording using the ADC
Step2: Recovery the register used to enable ADC to the default value

7.6.7 ENABLE ALC

The Audio Codec has the ALC function which can adjust the amplitude of the input analog signal automatically. You can use the register to enable or disable this function.

Step1: Set the Max and Min level of the ALC need to control.

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The register CALMR and CAHMR control, the max level of the ALC.

max_level={ CAHMR , CAHMR }

The relationship between the max_level and this signal amplitude(dB) is equal to:

amplitude(dB) = 20log(max_level/16'h7fff)

16'h7fff mean the full scale amplitude.

The register CALMINR and CAHMINR control, the min level of the ALC.

min_level={ CAHMR , CAHMR }

The relationship between the min_level and this signal amplitude(dB) is equal to:

amplitude(dB) = 20log(min_level/16'h7fff)

16'h7fff mean the full scale amplitude.

Step2: Set the register CSRR[2:0] according to the sample rate

Step3: Set the register CAFG[6] to 1 to enable the ALC module

Step4: Set the register CGR[5] to 1 to choose the ALC module to control the gain of the PGA

Step5: Observe the current ALC output gain from CCAGVR

7.6.8 DISABLE ALC

Step1: Set the register CAFG[6] to 0 to disable ALC module, then the ALC output gain will keep to the last value

Step2: Set the register CGR[5] to 0 to use the register to control the gain of the PGA, then we can use the register CAR[4:0] and CHR[4:0] to control the gain of PGA

7.6.9 ENABLE DAC I2S INTERFACE

Step1: Provide stable clock to the pin_sys_clk and pin_mclk

Step2: Reset the IP by low the pin_rst_n

Step3: Reset the IP by soft reset register

configure the register CGR to 8'h00 , then configure the register CGR to 8'h03

Step4: Configure the register related to the DAC I2S function to make the I2S RX work in different mode

I2S mode	Valid data length	CMCR	CDCR1	CDCR2
I2S stand	24	8'h3e	8'h50	8'h0e
	20	8'h3e	8'h30	8'h0e
	16	8'h3e	8'h10	8'h0e
I2S left justified	24	8'h3e	8'h48	8'h0e
	20	8'h3e	8'h28	8'h0e
	16	8'h3e	8'h08	8'h0e

Step5: Begin to input the I2S data stream to the I2S interface of DAC

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7.6.10 ENABLE ADC I2S INTERFACE

Step1: Provide stable clock to the pin_sys_clk and pin_mclk

Step2: Reset the IP by low the pin_rst_n

Step3: Reset the IP by soft reset register

configure the register CGR to 8'h00 , then configure the register CGR to 8'h03

Step4: Configure the register related to the ADC I2S function to make the I2S TX work in different mode

I2S mode	Valid data length	CMCR	CACR
I2S stand	24	8'h3e	8'h50
	20	8'h3e	8'h50
	16	8'h3e	8'h10
I2S left justified	24	8'h3e	8'h48
	20	8'h3e	8'h28
	16	8'h3e	8'h08

Step5: Begin to use the I2S interface of the ADC to output the parallel data

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8 DMIC Controller

8.1 Overview

The DMIC Controller is used to convert the signal of Digital Microphone to PCM signal.

Digital microphone relative to the analog MEMS microphone is more advanced technology, because of its high sensitivity, high signal to noise ratio, high noise reject capability, low distortion, low power consumption and other characteristics, widely used in higher recording requirements on new equipment.

8.2 Features

- Low power DMIC Controller
- 16 bits data interface and 20bit precision internal controller.
- SNR: 90dB, THD: -90dB @ FS -20dB
- Linear high pass filter include. Attenuation: -2.9dB@100Hz, -22dB@27Hz. -36dB@10Hz
- Low power voice trigger when waiting to start talking.
- 1/2/3/4 channel digital MIC support.
- Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation.
- Sample frequency supported: 8k, 16k.
- Support low power mode, user for decrease DMIC sensor and DMIC Controller power dissipation.

8.3 Pin Description

There are 2 or 3 Pins used to connect between DMIC Controller and DMIC sensor. They are listed and described in following table.

Table 8-1 DMIC Controller Pins Description

Name	I/O	Description
DMIC0_CLK	Output	DMIC sensor clock.
DMIC0_IN	Input	DMIC sensor data. Support left and right channel wire and.
DMIC1_IN	Input	DMIC sensor data. Support front and back channel wire and.

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8.4 DMIC Controller Block Diagram

Figure 8-1 DMIC Controller block diagram 1 of 2

Figure 8-2 DMIC Controller block diagram 2 of 2

Note: Front and back is same as left and right by SW_LR mode.

8.5 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

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R - Read only
W - Write only
RW - read and write
RCW - read and write, but clear to 0 by read
RSW - read and write, but set to 1 by read
RWC - read and write, clear to 0 by write 1, write 0 has no effect
RWS - read and write, set to 1 by write 1, write 0 has no effect
RC - read only, and clear to 0 by read
RS - read only, and set to 1 by read
SPEC - special access method, relate to its description

3. Reset Value
1 - reset to 1
0 - reset to 0
? - value unknown after reset

8.5.1 Registers Memory Map

Table 8-2 Registers Memory Map Base Address

Name	Base	Description
DMIC	0x10023000	Address base of DMIC Controller.

The DMIC Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 8-3 DMIC Controller Registers Map

Name	RW	Reset Value	Address offset	Access Size
DMIC_CR0	RW	0x0000_00C8	0x0000	32
DMIC_GCR	RW	0x0000_0000	0x0004	32
DMIC_IMR	RW	0x0000_003F	0x0008	32
DMIC_ICR	RW	0x0000_0000	0x000C	32
TRI_CR	RW	0x0003_0000	0x0010	32
THR_H	RW	0x0002_0000	0x0014	32
THR_L	RW	0x0000_127A	0x0018	32
TRI_M_MAX	RW	0x0000_03E8	0x001C	32
TRI_N_MAX	RW	0x0000_0003	0x0020	32
DMIC_DR	R	0x0000_0000	0x0030	32
DMIC_FCR	RW	0x0000_0040	0x0034	32
DMIC_FSR	R	0x0000_0000	0x0038	32
DMIC_CGDIS	RW	0x0000_0000	0x0050	32

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8.5.2 Register and Fields Description

8.5.2.1 DMIC Control register 0 (DMIC_CR0,0x0000)

	DMIC_CR0																															BASE + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESET	RESET_TRI	Reserved											CHNUM			Reserved		UNPACK_MSB	UNPACK_DIS	SW_LR	Reserved	Reserved_0	PACK_EN	SR		Reserved	Reserved_0	LP_MODE	HPF1_EN	TRI_EN	DMIC_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0

Bits	Name	Description	RW
31	RESET	If set this bit to '1' will reset all DMIC (Include FIFO \ data interface \ trigger block but without software configuration registers).	RWS
30	RESET_TRI	If set this bit to '1' will reset DMIC TRI block. (Without software configuration registers).	RWS
29:19	Reserved	Writes to these bits have no effect and always read as 0.	R
18:16	CHNUM	DMIC data interface channel number. 0: Mono 1: Stereo 2: 3channel 3: 4channel 4~8: Reserved	RW
15:14	Reserved	Writes to these bits have no effect and always read as 0.	R
13	UNPACK_MSB	Use sample data switch at DMIC_DR when PACK_EN = 1 and UNPACK_DIS = 1. Set '1' to disable the function.	RW
12	UNPACK_DIS	Disable unpack function, when pack mode.	RW
11	SW_LR	Switch left and right channel when data input. Set this bit to '1' will enable the function.	RW
10	Reserved	Writes to these bits have no effect and always read as 0.	R
9	Reserved_0	Inner usage, keep to 0.	RW
8	PACK_EN	Pack the 16-bit data to FIFO aim to economize the FIFO. Set this bit to '1' will enable the function.	RW
7:6	SR	DMIC interface output sample rate: 0: 8k 1: 16k 2: 48k(test only) 3: Disable the DMIC interface.	RW
5	Reserved	Writes to these bits have no effect and always read as 0.	RW
4	Reserved_0	Inner usage, keep to 0.	RW
3	LP_MODE	Low power mode. When this mode the DMIC_CLK frequency is 1.2MHz else the DMIC_CLK frequency is 2.4MHz. Set this bit to '1' will enable the function.	RW
2	HPF1_EN	HPF1(High pass filter) enable. Set this bit to '1' will enable the function.	RW
1	TRI_EN	Trigger mode enable.	RW

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		Set this bit to '1' will enable the function.	
0	DMIC_EN	DMIC enable. Set this bit to '1' will enable the function.	RW

8.5.2.2 DMIC Gain Control Register (DMIC_GCR,0x0004)

	DMIC_GCR																															BASE + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DGAIN				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writes to these bits have no effect and always read as 0.	R
4:0	DGAIN	Digital gain register. The gain of PGA equal to DGAIN * 3 dB.	RW

8.5.2.3 DMIC Interrupt Mask Register (DMIC_IMR,0x0008)

	DMIC_IMR																															BASE + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										FIFO_TRIG_MASK	WAKEUP_MASK	EMPTY_MASK	FULL_MASK	PRE_READ_MASK	TRI_MASK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Name	Description	RW
31:6	Reserved	Writes to these bits have no effect and always read as 0.	R
5	FIFO_TRIG_MASK	Enable FIFO_TRIG Interrupt.	RW
4	WAKEUP_MASK	Enable WAKEUP Interrupt.	RW
3	EMPTY_MASK	Enable EMPTY Interrupt.	RW
2	FULL_MASK	Enable FULL Interrupt.	RW
1	PRE_READ_MASK	Enable PRE_READ Interrupt.	RW
0	TRI_MASK	Enable TRI Interrupt.	RW

Note: 1. The pre-read is a function used to control FIFO over run. When FIFO over run, FIFO will pre-read a data to ensure the data of FIFO and the later data is continuously, but the data is discontinuously with before.

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8.5.2.4 DMIC Interrupt Control Register (DMIC_ICR,0x000C)

	DMIC_ICR																															BASE + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										FIFO_TRIG_FLAG	WAKEUP_FLAG	EMPTY_FLAG	FULL_FLAG	PRE_READ_FLAG	TRI_FLAG
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writes to these bits have no effect and always read as 0.	R
5	FIFO_TRIG_FLAG	When this bit is '1' indicate that FIFO level is reach the FIFO threshold was generate. Write this bit '1' will clear it.	RWC
4	WAKEUP_FLAG	When this bit is '1' indicate that wakeup of voice trigger was generate. Write this bit '1' will clear it.	RWC
3	EMPTY_FLAG	When this bit is '1' indicate that empty of FIFO was generate. Write this bit '1' will clear it.	RWC
2	FULL_FLAG	When this bit is '1' indicate that full of FIFO was generate. Write this bit '1' will clear it.	RWC
1	PRE_READ_FLAG	When this bit is '1' indicate that pre-read of FIFO was generate. Write this bit '1' will clear it.	RWC
0	TRI_FLAG	When this bit is '1' indicate that voice trigger was triggered. Write this bit '1' will clear it.	RWC

Note: 1. The PRE_READ indicated that FIFO was over run. When FIFO over run, FIFO will pre-read a data to ensure the data of FIFO and the later data is continuously.

2. The FULL indicated that FIFO was over run. It active when pclk was stopped.

8.5.2.5 DMIC Trigger Control Register (TRI_CR,0x0010)

	TRI_CR																															BASE + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												TRI_MODE				Reserved											TRI_DEBUG	HPF2_EN	PREFETCH		TRI_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

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31:20	Reserved	Writes to these bits have no effect and always read as 0.	R
19:16	TRI_MODE	Trigger mode: 0. If the signal great than the THR_L level, trigger generate. 1. If the signal peak is great than THR_L and less than THR_H, trigger generate. 2. If the signal great than the THR_L level and continue num N times, trigger generate. 3. If the signal peak is great than THR_L and less than THR_H and continue num N times, trigger generate. 4. Same as mode 2, but use THR_L and THR_H to Schmitt mode. 5~15. Reserved.	RW
15:5	Reserved	Writes to these bits have no effect and always read as 0.	R
4	TRI_DEBUG	Voice Trigger module Debug mode enable. Set this bit to '1' will transmit the data of Voice Trigger module input to FIFO.	RW
3	HPF2_EN	HPF2(High pass filter) enable. Set this bit to '1' will enable the function.	RW
2:1	PREFETCH	Auto open the DMIC interface and prefetch the data to FIFO and ignore the SR when trigger. 0. Prefetch function disable. 1. Prefetch function use 8k mode. 2. Prefetch function use 16k mode. 3. Reserved.	RW
0	TRI_CLR	If write this bit '1' will clear trigger.	RWS

8.5.2.6 DMIC Trigger High Threshold (THR_H,0x0014)

	THR_H																															BASE + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												THR_H																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writes to these bits have no effect and always read as 0.	R
19:0	THR_H	DMIC Trigger High Threshold.	RW

8.5.2.7 DMIC Trigger Low Threshold (THR_L,0x0018)

	THR_L	BASE + 0x0018

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												THR_L																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	1	1	0	1	0

Bits	Name	Description	RW
31:20	Reserved	Writes to these bits have no effect and always read as 0.	R
19:0	THR_L	DMIC Trigger Low Threshold.	RW

8.5.2.8 DMIC Trigger number M Max value (TRI_M_MAX,0x001C)

	TRI_M_MAX																															BASE + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								M_MAX																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writes to these bits have no effect and always read as 0.	R
23:0	M_MAX	The num m max value used for the time out. After M cycle, if the trigger have not generate and the generate times of trigger less than N_MAX, the counter of N will be clear. The time of M one cycle is 1 / 12MHz.	RW

8.5.2.9 DMIC Trigger number N Max value (TRI_N_MAX,0x0020)

	TRI_N_MAX																															BASE + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																N_MAX															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
31:16	Reserved	Writes to these bits have no effect and always read as 0.	R

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15:0	N_MAX	The num n max value used for the time. If trigger generated N times, Interrupt will be generate.	RW

8.5.2.10 DMIC Data Register (DMIC_DR,0x0030)

	DMIC_DR																															BASE + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FIFO_DATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FIFO_DATA	FIFO data register. This register is connect to the FIFO. The left channel data laid at the bit 0 ~ bit 15, the right channel data laid at the bit 16 ~ bit 31. Note: When trigger debug mode,	R

8.5.2.11 DMIC FIFO Control register (DMIC_FCR,0x0034)

	DMIC_FCR																															BASE + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMS	Reserved																									FIFO_THR					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDMS	DMIC receive FIFO request enable. Set this bit to '1' will enable the function.	
30:6	Reserved	Writes to these bits have no effect and always read as 0.	R
5:0	FIFO_THR	FIFO threshold. When FIFO level is great than the FIFO threshold the DMIC request will generate.	RW

Note: FIFO_THR mast be less than 60. (FIFO size is 64 x 64)

8.5.2.12 DMIC FIFO State Register (DMIC_FSR,0x0038)

	DMIC_FSR	BASE + 0x0038

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												FULL_S	TRIG_S	PRERD_S	EMPTY_S	Reserved										FIFO_LVL					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writes to these bits have no effect and always read as 0.	R
19	FULL_S	FIFO FULL state.	R
18	TRIG_S	FIFO trigger state.	R
17	PRERD_S	FIFO pre-read mode state.	R
16	EMPTY_S	FIFO empty state.	R
15:6	Reserved	Writes to these bits have no effect and always read as 0.	R
5:0	FIFO_LVL	FIFO level state.	R

8.5.2.13 Clock Gate Disable Register (DMIC_CGDIS,0x0050)

(Internal use !)

	DMIC_CGDIS																															BASE + 0x0050
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HPF2_CGDIS	Reserved	HPF1F_CGDIS	SRC3F_CGDIS	SRC2F_CGDIS	SRC1F_CGDIS	FIR2F_CGDIS	FIR3F_CGDIS	TRI_CGDIS	Reserved	HPF1B_CGDIS	SRC3B_CGDIS	SRC2B_CGDIS	SRC1B_CGDIS	FIR2B_CGDIS	FIR3B_CGDIS	TRI_LPF_CGDIS	Reserved	HPF1R_CGDIS	SRC3R_CGDIS	SRC2R_CGDIS	SRC1R_CGDIS	FIR2R_CGDIS	FIR3R_CGDIS	INV_DAT_MASK_DIS	Reserved	HPF1L_CGDIS	SRC3L_CGDIS	SRC2L_CGDIS	SRC1L_CGDIS	FIR2L_CGDIS	FIR3L_CGDIS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	HPF2_CGDIS	HPF2 clock gate disable.	RW
30	Reserved	Writes to these bits have no effect and always read as 0.	R
29	HPF1B_CGDIS	HPF1 of Left channel clock gate disable.	RW
28	SRC3B_CGDIS	SRC3 of Left channel clock gate disable.	RW
27	SRC2B_CGDIS	SRC2 of Left channel clock gate disable.	RW
26	SRC1B_CGDIS	SRC1 of Left channel clock gate disable.	RW
25	FIR2B_CGDIS	LPF_FIR2 of Left channel clock gate disable.	RW
24	FIR3B_CGDIS	LPF_FIR3 of Left channel clock gate disable.	RW
23	TRI_CGDIS	Voice Trigger clock gate disable.	RW
22	Reserved	Writes to these bits have no effect and always read as 0.	R

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21	HPF1F_CGDIS	HPF1 of Left channel clock gate disable.	RW
20	SRC3F_CGDIS	SRC3 of Left channel clock gate disable.	RW
19	SRC2F_CGDIS	SRC2 of Left channel clock gate disable.	RW
18	SRC1F_CGDIS	SRC1 of Left channel clock gate disable.	RW
17	FIR2F_CGDIS	LPF_FIR2 of Left channel clock gate disable.	RW
16	FIR3F_CGDIS	LPF_FIR3 of Left channel clock gate disable.	RW
15	TRI_LPF_CGDIS	LPF for Trigger clock gate disable.	RW
14	Reserved	Writes to these bits have no effect and always read as 0.	R
13	HPF1R_CGDIS	HPF1 of Left channel clock gate disable.	RW
12	SRC3R_CGDIS	SRC3 of Left channel clock gate disable.	RW
11	SRC2R_CGDIS	SRC2 of Left channel clock gate disable.	RW
10	SRC1R_CGDIS	SRC1 of Left channel clock gate disable.	RW
9	FIR2R_CGDIS	LPF_FIR2 of Left channel clock gate disable.	RW
8	FIR3R_CGDIS	LPF_FIR3 of Left channel clock gate disable.	RW
7	INV_DAT_MASK_DIS	Invalid data when DMIC controller interface begin enable mask disable that all data will write to FIFO.	RW
6	Reserved	Writes to these bits have no effect and always read as 0.	R
5	HPF1L_CGDIS	HPF1 of Left channel clock gate disable.	RW
4	SRC3L_CGDIS	SRC3 of Left channel clock gate disable.	RW
3	SRC2L_CGDIS	SRC2 of Left channel clock gate disable.	RW
2	SRC1L_CGDIS	SRC1 of Left channel clock gate disable.	RW
1	FIR2L_CGDIS	LPF_FIR2 of Left channel clock gate disable.	RW
0	FIR3L_CGDIS	LPF_FIR3 of Left channel clock gate disable.	RW

8.6 DMIC Controller Timing

The following figures show the timing relationship for the DMIC transfers. The DMIC_CLK is generated from DMIC Controller to DMIC (Digital Microphone sensor). DMIC Controller samples the DMIC0_IN Pin use the different edge to two channels.

Figure 8-3 The DMIC signal Timing

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8.7 DMIC Controller Operation

8.7.1 Turn on data path flow

1. Set all configuration registers. Such as SR \ STEREO \ LP_MODE \ IMR \ ICR \ HPF1_EN \ GCR.
2. Set DMIC_CR0.RESET = ‘1’ and then wait for this bit read ‘0’.
3. Set DMIC_EN = ‘1’, DMIC Controller will transfer the data to FIFO.

8.7.2 Turn on trigger path flow

1. Set all configuration registers. Such as SR \ STEREO \ LP_MODE \ IMR \ ICR \ HPF1_EN \ GCR.
2. Set DMIC_CR0.RESET = ‘1’ and then wait for this bit read ‘0’.
3. Set TRI_EN = ‘1’ and DMIC_EN = ‘1’, DMIC Controller will transfer the data to FIFO.

8.7.3 Trigger application flow.

1. Set all configuration registers. Such as DMIC_CR0 \ SR \ STEREO \ LP_MODE \ IMR \ ICR \ HPF1_EN \ GCR.
2. Set DMIC_CR0.RESET = ‘1’ and then wait for this bit read ‘0’.
3. Set DMIC_EN = ‘1’, DMIC Controller will transfer the data to FIFO.
4. Set all Trigger configuration registers. Such as TRI_CR \ THR_H \ THR_L \ TRI_M \ TRI_N.
5. Set SR = ‘3’ use for close DMIC data path, the data level of FIFO no longer increases.
6. Set RESET_EN = ‘1’ and RESET_TRI = ‘1’, and then wait for these bit read ‘0’.
7. Wait trigger interrupt.
8. When the interrupt is generated, set SR to target value, then DMIC Controller will transfer the data to FIFO.
9. set DMIC_EN = ‘0’ to turn off the trigger part.

Note : If PREFETCH = ‘1’, the data transfer will start at trigger interrupt generate.

Trigger level configuration

1. Set LP_MODE = '1' or '0' (In accordance with recode and trigger mode configuration).
   Set PACK_EN = '0', set UNPACK_DIS = '0', set SR = '3'.
   Set HPF2_EN = '1' or '0' (In accordance with trigger mode configuration).
   Set TRI_DEBUG = '1'.
2. Set DMIC_CR0.RESET = ‘1’ and then wait for this bit read ‘0’.
3. Set DMIC_EN = '1', and set TRI_EN = '1'.
4. Read FIFO use by 32-bit signed format (The most 24-bit is valid data).
5. Identification the noise level and voice level, used to make sure the trigger level.
6. For example trigger mode 1. The THR_L = trigger result (the Trigger level of the previous step)(Normalization: range -1 ~ 1) * 2^19.
7. Set the THR_L value.
8. Run the trigger application follow.

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8.7.4 Wakeup by DMIC Trigger flow

When CPU is in sleep mode, If DMIC controller is active (please see CPM specification sleep mode) and the voice meet the requirements (Trigger configure registers), DMIC will generate a interrupt to INTC and then wakeup CPU. The DMIC wakeup flow is:

1. Configure DMIC controller for Trigger application flow.
2. configure CPM to mask INTC's interrupt
3. disable CPU's IE(interrupt enable)
4. configure CPM to make system turn into sleep, idle deep sleep or deep idle state. (See CPM sleep mode)
5. When the voice meet the requirements (Trigger configure registers), DMIC will generate a interrupt to INTC and then wakeup CPU.
6. Set step 2 \ 3 \ 4's configuration to normal state
7. Interrupt handler Configure DMIC controller for Turn on data path flow.
8. Check the voice data from DMIC controller by voice recognition software. If the voice is the keyword of wakeup, boot the operating system.

8.7.5 FIFO operations

DMIC controller has a 64*64 bit FIFO. The formats are configure by 3 registers: pack / chnum / tri_debug, which audio data store in FIFO. The all format as show below:

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debug=0
pack=0
chnum=3

63	32 31		0
B0	F0	R0	L0
B1	F1	R1	L1
⋮	⋮	⋮	⋮

debug=0
pack=1
chnum=0

63	32 31		0
L3	L2	L1	L0
L7	L6	L5	L4
⋮	⋮	⋮	⋮

debug=0
pack=1
chnum=1

63	32 31		0
R1	L1	R0	L0
R3	L3	R2	L2
⋮	⋮	⋮	⋮

debug=1

63	32 31	0
VT1	VT0	
VT3	VT2	
⋮	⋮	

The formats are configure by 4 registers: unpack_dis / chnum / rg_debug / unpack_msb, which the bus read from FIFO. The all format as show below:

debug=0
unpackage_dis=1
chnum=0

31	0
L1	L0
L3	L2
⋮	⋮

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debug=0
unpackage_dis=1
chnum=1

31	0
R0	L0
R1	L1
⋮	⋮

debug=0
unpackage_dis=1
chnum=2

31	0
R0	L0
0x0	F0
⋮	⋮

debug=0
unpackage_dis=1
chnum=3

31	0
R0	L0
B0	F0
⋮	⋮

debug=0
unpackage_dis=0
chnum=0

31	0
0x0	L0
0x0	L1
0x0	⋮

debug=0
unpackage_dis=0
chnum=1

31	0
0x0	L0
0x0	R0
0x0	L1
0x0	R1
0x0	⋮

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debug=0
unpackage_dis=0
chnum=2

31	0
0x0	L0
0x0	R0
0x0	F0
0x0	L1
0x0	⋮

debug=0
unpackage_dis=0
chnum=2

31	0
0x0	L0
0x0	R0
0x0	F0
0x0	B0
0x0	L0
0x0	⋮

debug=1

31	12	0
VT0		0
VT1		0
⋮		⋮

The unpack_msb use to switch the DR register 0~15 bit and 16~31 bit. Set unpack_msb = '1' to disable the function.

8.7.6 Trigger operations:

Voice trigger of DMIC controller has 5 trigger modes.

8.7.6.1 Single level trigger mode.

When this mode, the trigger interrupt generate condition is that voice signal was higher than the trigger level (THR_L).

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Figure 8-4 One word voice signal

Figure 8-5 Magnifying the above Figure 8-4

8.7.6.2 Multiple level trigger mode.

Some times, the noise can higher than the trigger level too. Such as bump noise or knocking noise. But the sound has a law that the signal duration is very short. We can use the multiple level trigger mode to avoid the false trigger.

When this mode, the trigger interrupt generate condition is that voice signal was higher than the trigger level (THR_L) multi-times (TRI_N_MAX).

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Figure 8-6 A bump noise before one word voice signal

Figure 8-7 Magnifying the bump part of above Figure 8-6

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Figure 8-8 Magnifying the voice part of above Figure 8-7

8.7.6.3 Single limited level trigger mode.

Some times, the noise can higher than the trigger level even and voice level. Such as bump noise or knocking noise. We can use the multiple limited level trigger mode to avoid the false trigger.

Figure 8-9 A bump noise before one word voice signal

8.7.6.4 Multiple limited level trigger mode.

This mode focus the advantages of the above two modes that Multiple level trigger mode and Single limited level trigger mode.

8.7.6.5 Multiple Schmitt trigger mode.

If the noise value is close to the voice level, noise will make the voice signal in the vicinity of the

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threshold trigger repeatedly. But perhaps the real voice is much less than the trigger cycles, it will make the purpose of setting the number (TRI_N_MAX and TRI_M_MAX) of inaccuracies. We can use the multiple Schmitt trigger mode to filter the noise of superimposed.

Figure 8-10 Magnifying the one word voice signal use by multiple level trigger mode

Figure 8-11 Magnifying the one word voice signal use by multiple Schmitt trigger mode

8.7.7 DMIC controller clocks set

DMIC controller needs a work clock from CPM. Set I2SCDR of CPM to generate a 12M Hz clocks for DMIC controller. The clock of I2SCDR generated is shared by AIC. DMIC controller generates a 1.2MHz (low power mode) or 2.4MHz DMIC clock for DMIC sensor use. If DMIC_EN was set to ‘0’, the DMIC clock will be gated

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Section 4

MEMORY INTERFACE

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9 DDR Controller

9.1 Overview

DDRC (DDR Controller) is a general IP which provides an interface to DDR2, DDR3, mobile DDR(LPDDR) and LPDDR2 memory. The DDRC IP is designed for SOC usage and is configurable, scalable to meet the requirement of various SOC.

9.2 Features

- Multi-port Architecture and asynchronous interface to all port
- Support clock-stop mode
- Support auto-refresh and self-refresh
- Support power-down mode and deep-power-down mode
- Programmable DDR timing parameters
- Programmable DDR row and column address width
- Programmable remapping from Logic address to Physical address

9.3 Supported DDR SDRAM Types

- DDR2
- DDR3
- LPDDR (mobile DDR)
- LPDDR2

Row address width less than 16-bit & Column width less than 12-bit are supported.

9.4 Block Diagram

Following figure shows the functional block diagram of DDR system.

Figure 9-1 DDR system block diagram

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9.5 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

9.5.1 Register Memory Map

Following table lists the registers of DDR Controller. All of these registers are 32bit. According different configure ports to be access, these registers are divided into 3 groups.

- DDRC_AHB_CFG_GROUP:
  Registers access by AHB2(CH5_AHB)
  Base Address: *0x134F0000 ~ 0x134F0FFF*
- DDRC_APB_CFG_GROUP:
  Registers access by DDRC_APB_Config port
  Base Address: *0xB3012000 ~ 0xB3012FFF*
- DDRP_APB_CFG_GROUP:
  Registers access by DDRP_APB_Config port
  Base Address: *0xB3011000 ~ 0xB3011FFF*

Please Note that: the DDRC_AHB_CFG_GROUP must not be access under retention mode.

Table 9-1 DDRC Register

Name	Group	Address offset	Width	Access	Description

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DSTATUS	DDRC_AHB	0x00	32	RW	DDR Status Register
DCFG	DDRC_AHB	0x04	32	RW	DDR Configure Register
DCTRL	DDRC_AHB	0x08	32	RW	DDR Control Register
DLMR	DDRC_AHB	0x0C	32	RW	DDR Load-Mode-Register
DTIMING 1	DDRC_AHB	0x60	32	RW	DDR Timing Configure Register 1
DTIMING 2	DDRC_AHB	0x64	32	RW	DDR Timing Configure Register 2
DTIMING 3	DDRC_AHB	0x68	32	RW	DDR Timing Configure Register 3
DTIMING 4	DDRC_AHB	0x6C	32	RW	DDR Timing Configure Register 4
DTIMING 5	DDRC_AHB	0x70	32	RW	DDR Timing Configure Register 5
DTIMING 6	DDRC_AHB	0x74	32	RW	DDR Timing Configure Register 6
DREFCN T	DDRC_AHB	0x18	32	RW	Auto-Refresh Counter
DMMAP0	DDRC_AHB	0x24	32	RW	DDR Memory CS0 Map Configure Register
DMMAP1	DDRC_AHB	0x28	32	RW	DDR Memory CS1 Map Configure Register
DDLP	DDRC_AHB	0xBC	32	RW	DDR DFI low power handshake register
DREMAP 1	DDRC_AHB	0x9C	32	RW	DDR address remapping register1
DREMAP 2	DDRC_AHB	0xA0	32	RW	DDR address remapping register2
DREMAP 3	DDRC_AHB	0xA4	32	RW	DDR address remapping register3
DREMAP 4	DDRC_AHB	0xA8	32	RW	DDR address remapping register4
DREMAP 5	DDRC_AHB	0xAC	32	RW	DDR address remapping register5
DSTRB	DDRC_AHB	0x34	32	RW	Multi-media stride register
WCMDCT RL1	DDRC_AHB	0x100	32	RW	Write command reorder & grouping (Performance control)

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RCMDCTRL0	DDRC_AHB	0x104	32	RW	Read Channel mode control (Performance control)
RCMDCTRL1	DDRC_AHB	0x108	32	RW	Read Channel mode control (Performance control)
BOUNDAEYSEL	DDRC_AHB	0x10C	32	RW	Channel boundary select
WDATTHD0	DDRC_AHB	0x114	32	RW	Wdata Channel mode control (Performance control)
WDATTHD1	DDRC_AHB	0x118	32	RW	Wdata Channel mode control (Performance control)
IPORTWPRI	DDRC_AHB	0x240	32	RW	Configuration of Internal Priority for write channel (Performance control)
IPORTRPRI	DDRC_AHB	0x244	32	RW	Configuration of Internal Priority for read channel (Performance control)
CHxWDOS	DDRC_AHB	0x200 0x204 0x208 0x20C 0x210 0x214 0x218	32	RW	WQoS configure for each channel (Performance control)
CHxRDOS	DDRC_AHB	0x220 0x224 0x228 0x22C 0x230 0x234 0x238	32	RW	RQoS configure for each channel (Performance control)
AUTOSR_CNT	DDRC_AHB	0x308	32	RW	Auto Self Refresh counter configuration
AUTOSR_EN	DDRC_AHB	0x304	32	RW	Auto Self Refresh enable
EFPRB_CFG	DDRC_AHB	0x30C	32	RW	Bus efficiency probe configuration
EFPRB_VALUE	DDRC_AHB	0x310	32	R	Bus efficiency data
CLKSTP_CFG	DDRC_APB	0x068	32	RW	Auto Clock Gating configuration
DDRC_STATUS	DDRC_APB	0x06C	32	R	DDR status

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PHYRET_CFG	DDRC_APB	0x034	32	RW	Retention Mode Configuration
EPD_HADDR	DDRC_APB	0x070	32	RW	EPD wake up configure
EPD_LADDR	DDRC_APB	0x074	32	RW	EPD wake up configure
AUTOPRE_CFG	DDRC_APB	0x07C	32	RW	Auto Pre-charge Configuration
PHYRST_CFG	DDRC_APB	0x080	32	RW	DDR Phy reset control
CKC_CFG0	DDRC_APB	0x084	32	RW	Clock change Configuration
PHY_INIT	DDRC_APB	0x08c	32	RW	DFI initial configuration
CKC_CFG1	DDRC_APB	0x088	32	RW	Clock change Configuration
CPM_DRCG		**0xB00000D0**	32	RW	CPM register, DLL & Clock control for DDR

9.5.2 Register and Fields Description

9.5.2.1 DDR Status Register (DSTATUS, 0x134F0000)

	DSTATUS																															**0x134F0000**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DFI_INIT_C	Reserved																							ENDIAN	MISS	DPD	PD	AREF	SREF	CKE1	CKE0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	DFI_INIT_C	0:DFI initialization not completed.(default) 1: DFI initialization completed	R
30:8	Reserved	Writing has no effect, read as zero.	R
7	ENDIAN	0: Little data Endian. 1: Big data Endian.	R
6	MISS	0: No operation miss DDRC memory mapping. (reset value) 1: At least one operation miss DDRC memory mapping. Indicate the accessed address is out of memory mapping range. (This bit is un-writable. Once read this register, this bit will be set to 0)	R

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5	DPD	0: DDR memory is NOT in deep-power-down state. 1: DDR memory is in deep-power-down state.	R
4	PD	0: DDR memory is NOT in power-down state. 1: DDR memory is in power-down state.	R
3	AREF	0: DDR memory is NOT in auto-refresh state. 1: DDR memory is in auto-refresh state.	R
2	SREF	0: DDR memory is NOT in self-refresh state. 1: DDR memory is in self-refresh state.	R
1	CKE1	0: CKE1 Pin is low 1: CKE1 Pin is high.	R
0	CKE0	0: CKE0 Pin is low. 1: CKE0 Pin is high.	R

9.5.2.2 DDR Configure Register (DCFG, 0x134F0004)

Configure the external memory, static configuration only. ie. This register can NOT be changed on-the-fly.

	DCFG																															0x134F0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AN_TE	Reserved	ROW1			COL1			BA1	IMBA	BSL	Reserved	TYPE			ODTEN	MISPE	Reserved	ROW0			COL0			CS1EN	CS0EN	Reserved				BA0	DW
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	AN_TE	Analog test enable.	RW
30	Reserved	Writing has no effect, read as zero.	R
29:27	ROW1	Row Address width. Specify the row address width of external DDR. **Description** 000: 12-bit row address(reset value) 001: 13-bit row address 010: 14-bit row address 011: 15-bit row address 100: 16-bit row address 101~111: Reserved	RW
26:24	COL1	Column Address width. Specify the Column address width of external DDR. **Description** 000: 8-bit Column address.(reset value) 001: 9-bit Column address	RW

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<table>
<tr><td></td><td></td><td>
<table>
<tr><td>010</td><td>10-bit Column address</td></tr>
<tr><td>011</td><td>11-bit Column address</td></tr>
<tr><td>100</td><td>12-bit Column address</td></tr>
<tr><td>101~111</td><td>Reserved</td></tr>
</table>
</td><td></td></tr>
<tr><td>23</td><td>BA1</td><td>Bank address width of external memory device.
<table>
<tr><th>BA1</th><th>Description</th></tr>
<tr><td>0</td><td>4 bank device(reset value)</td></tr>
<tr><td>1</td><td>8 bank device</td></tr>
</table>
</td><td>RW</td></tr>
<tr><td>22</td><td>IMBA</td><td>0: CS0, CS1 connected 2 memory chips which have same ROW, COL, BA configuration.In this mode, both chips are configured by ROW0,COL0, BA0 . ROW1,COL1,BA1 does not effect the system.

1: CS0, CS1 connected 2 memory chips which have different ROW, COL, BA configuration. Chip0 is configured by ROW0, COL0, BA0;Chip1 is configured by ROW1, COL1, BA1;</td><td>RW</td></tr>
<tr><td>21</td><td>BSL</td><td>Burst length for DDR chips
1: 8 burst
0: 4 burst</td><td>RW</td></tr>
<tr><td>20</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>19:17</td><td>TYPE</td><td>Select external memory device type.
<table>
<tr><th>Bit [19:17]</th><th>Description</th></tr>
<tr><td>000</td><td>Normal SDR (Single-Data-Rate) SDRAM(Not support).(reset value)</td></tr>
<tr><td>001</td><td>Mobile SDR(Not support).</td></tr>
<tr><td>010</td><td>Normal DDR1 (Not support)</td></tr>
<tr><td>011</td><td>Mobile DDR(LPDDR).</td></tr>
<tr><td>100</td><td>Normal DDR2.</td></tr>
<tr><td>101</td><td>LPDDR2(Not support)</td></tr>
<tr><td>110</td><td>Normal DDR3</td></tr>
<tr><td>111</td><td>LPDDR3 (Not support).</td></tr>
</table>
</td><td>RW</td></tr>
<tr><td>16</td><td>ODTEN</td><td>On-die terminate enable
0: On-die-termination off
1: On-die-termination on</td><td>RW</td></tr>
<tr><td>15</td><td>MISPE</td><td>Missing CS protection Enable. Set 1 to enable.
If software access a memory space which is not selected by any CS, controller will return random data to a read operation (or mask write operation) to avoid system bus being locked. As long as this happens, a flag will set in DSTATUS.miss.</td><td></td></tr>
<tr><td>14</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>13:11</td><td>ROW0</td><td>Row Address width. Specify the row address width of external DDR.
<table>
<tr><th></th><th>Description</th></tr>
</table>
</td><td>RW</td></tr>
</table>

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<table>
<tr><td></td><td></td><td><table><tr><td>000</td><td>12-bit row address(reset value)</td></tr><tr><td>001</td><td>13-bit row address</td></tr><tr><td>010</td><td>14-bit row address</td></tr><tr><td>011</td><td>15-bit row address</td></tr><tr><td>100</td><td>16-bit row address</td></tr><tr><td>101~111</td><td>Reserved</td></tr></table></td><td></td></tr>
<tr><td>10:8</td><td>COL0</td><td>Column Address width. Specify the Column address width of external DDR.<table><tr><th></th><th>Description</th></tr><tr><td>000</td><td>8-bit Column address.(reset value)</td></tr><tr><td>001</td><td>9-bit Column address</td></tr><tr><td>010</td><td>10-bit Column address</td></tr><tr><td>011</td><td>11-bit Column address</td></tr><tr><td>100</td><td>12-bit Column address</td></tr><tr><td>101~111</td><td>Reserved</td></tr></table></td><td>RW</td></tr>
<tr><td>7</td><td>CS1EN</td><td>If an DDR memory chip is connected to ddr pin cs1, set CS1EN=1.<table><tr><th>Bit [7]</th><th>Description</th></tr><tr><td>0</td><td>DDR Pin CS1 is not in use. (reset value)</td></tr><tr><td>1</td><td>DDR Pin CS1 is in use.</td></tr></table></td><td>RW</td></tr>
<tr><td>6</td><td>CS0EN</td><td>If an DDR memory chip is connected to ddr pin cs0, set CS1EN=0.<table><tr><th>Bit [6]</th><th>Description</th></tr><tr><td>0</td><td>DDR Pin CS0 is not in use. (reset value)</td></tr><tr><td>1</td><td>DDR Pin CS0 is in use.</td></tr></table></td><td>RW</td></tr>
<tr><td>5:2</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>1</td><td>BA0</td><td>Bank address width of external memory device.<table><tr><th>Bit [1]</th><th>Description</th></tr><tr><td>0</td><td>4 bank device(reset value)</td></tr><tr><td>1</td><td>8 bank device</td></tr></table></td><td>RW</td></tr>
<tr><td>0</td><td>DW</td><td>External DDR Memory Data Width.Specify the external DDR memory data width.<table><tr><th>Bit [0]</th><th>Description</th></tr><tr><td>0</td><td>External memory data width is 16-bit. (reset value)</td></tr><tr><td>1</td><td>External memory data width is 32-bit.</td></tr></table></td><td>RW</td></tr>
</table>

9.5.2.3 DDR Control Register (DCTRL, 0x134F0008)

On the positive edge of START, the command selected by CMD field will be performed.

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	DCTRL																															0x134F0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								DFI_RST	DLL_RST	CTL_RST	CFG_RST	Reserved		KEEPSR	Reserved	ACTPD	PDT			ACTSTP	Reserved				DPD	SR	Reserved		SLOWEXPD	CKE_PULSE	RESET
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23	DFI_RST	DFI interface reset. Set to 0 before initialize DDR PHY.	RW
22	DLL_RST	Reserved, please keep the default value.	R
21	CTL_RST	Reserved, please keep the default value.	R
20	CFG_RST	Reserved, please keep the default value.	R
19:18	Reserved	Writing has no effect, read as zero.	R
17	KEEPSR	inner usage, keep to 0.	
16	Reserved	Writing has no effect, read as zero.	R
15	ACTPD	Active Power-Down. Some SDRAM devices support Active-Power-Down. By default, ACTPD=0, hardware will percharge all active banks before entering Power-Down mode, so called Precharge-Power-Down. By setting ACTPD=1, hardware drives SDRAM into Power-Down mode without precharge all active banks, some banks are still active in Power-Down mode, so called Active-Power-Down. 0: Precharge all banks before entering power-down. 1: Do not precharge all banks before entering power-down.	RW
14:12	PDT	Power-Down Timer. When there's no access to DDR memory for a period of time, hardware drives DDR into power-down mode to save power consumption. Hardware can exit Power-Down mode automatically when new access arrives. If PDT=0, power-down function is disabled. If enable power-down mode, it is recommended to be set after DDR initialization.	RW

Bit [14:13]	Description
000	power-down disabled, hardware never drive SDRAM into power-down mode.
001	Enter power-down after 8 tCK idle.
010	Enter power-down after 16 tCK idle.
011	Enter power-down after 32 tCK idle.
100	Enter power-down after 64 tCK idle.

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<table>
<tr><td></td><td></td><td><table><tr><td>101</td><td>Enter power-down after 128 tCK idle.</td></tr><tr><td>110 - 111</td><td>Reserved.</td></tr></table></td><td></td></tr>
<tr><td>11</td><td>ACTSTP</td><td>Active Clock-Stop.
0: Clock can be stopped only after all banks be precharged.
1: Clock can be stopped after some bank’s row actived.</td><td>RW</td></tr>
<tr><td>10:7</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>6</td><td>DPD</td><td>Software drives external Mobile DDR device entering Deep-Power-Down mode.
Software set DPD = 1 drives external Mobile DDR device entering Deep-Power-Down mode instead of Power-Down mode, when there’s no access to DDR memory for a period of time. So you must firstly enable Power-Down mode (refer to PDT).
Software needs to reset DDR controller and re-do a complete initial process to exit Deep-Power-Down mode.
When external device goes to Deep-Power-Down mode, it lose all data store in memory and registers.
The memory chip will cut off inner power supply for power saving.</td><td>RW</td></tr>
<tr><td>5</td><td>SR</td><td>Software drive external DDR device entering Self-Refresh mode.
Software set SR=1 drive external DDR device entering self-refresh mode;
Software set SR=0 drive external DDR device exiting self-refresh mode;
In this mode, the CK to external DDR device would be stopped during self-refresh period;
But the clock supplied to ddr_controller logic would not stop.
Software can read & write ddr_controller registers in this mode.
Software can NOT read or write memory data in this mode.
NOTE: Software must guarantee that there’s no memory access during self-refresh mode. Otherwise, software can NOT exit this mode, system would be hang-up!!
<table><tr><th>SR</th><th>Description</th></tr><tr><td>0</td><td>Drive external DDR device exit self-refresh mode.</td></tr><tr><td>1</td><td>Drive external DDR device enter self-refresh mode.</td></tr></table></td><td></td></tr>
<tr><td>4:3</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>2</td><td>SLOWEXPD</td><td>Slow exit power-down enable.
If set, the controller use DTIMING6.tXSRD value as tXPDLL.
<table><tr><th>SLOWEXPD</th><th>Description</th></tr><tr><td>0</td><td>Slow exit power-down disenable.</td></tr><tr><td>1</td><td>Slow exit power-down enable.</td></tr></table></td><td></td></tr>
<tr><td>1</td><td>CKE_PULSE</td><td>If set, a CKE pulse will be trigger. This bit is hardware self cleaning.
Note:This register is used only for DDR initializing sequence; software should NOT update this register when DDR memory is in normal</td><td></td></tr>
</table>

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		working mode.	
0	RESET	Module reset for DDR controller. Software is able to reset DDR controller by setting RESET bit high and ends the reset by clear this bit. **RESET** / **Description** 0 / End resetting DDR controller. 1 / Resetting DDR controller.	

9.5.2.4 DDR Load-Mode-Register (DLMR, 0x134F000C)

DLMR register is used for initializing the DDR SDRAM memory device.

On the positive edge of START, the command selected by CMD field will be performed.

	DLMR																															0x134F000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDR_ADDR																				Reserved	BA			Reserved		CMD			Reserved		START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	DDR_ADDR	When performing a DDR command, DDR_ADDR[13:0]corresponding to external DDR address Pin A[13:0];DDR_ADDR[15:14] are reserved	RW
11	Reserved	Writing has no effect, read as zero.	R
10:8	BA	Bank Address. When performing a DDR command, BA[2:0] corresponding to external DDR address Pin BA[2:0].	
7:6	Reserved	Writing has no effect, read as zero.	R
5:3	CMD	Select command to process when setting START from low to high. On the positive edge of START, one of the following commands will be performed. **Bit [5:3]** / **Description** 000 / Precharge one bank / All banks. (dependent field : BA, DDR_ADDR) 001 / Auto-Refresh. 010 / Load Mode Register. (dependent field : BA, DDR_ADDR) 011 / ZQCS for DDR3 100 / ZQCL for DDR3 101~111 / Reserved.	
2:1	Reserved	Writing has no effect, read as zero.	R

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0	START	Start to perform a command to external DDR memory. The command is performed on the positive edge of START; Hardware will clear START bit to zero when command issued out to external DDR memory. Write 0 to START will be ignored and take no effect; START=1 means hardware is busy executing current command and can NOT accept new command; Software must check START=0 before writing 1 to START. 0: No command is performed. 1: On the positive edge of START, perform a command defined by CMD field.	

9.5.2.5 DDR Timing Configure Register 1 (DTIMING1, 0x134F0060)

The timing parameters are identical to the JEDEC DDR Specification.

If the DDR clock period are tCK.

All these registers's value equal to the number tCK cycle. For example, if tRTP=2, it means 2 tCK between READ and PRECHARGE;

	DTIMMING1																															0x134F0060
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		tRTP						Reserved		tWTR						Reserved		tWR						Reserved		tWL					
RST	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect. Read as zero.	R
29:24	tRTP	READ to PRECHARGE command period.	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tWTR	WRITE to READ command delay.	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tWR	WRITE Recovery Time defined by register MR of DDR2 DDR3 memory.	RW
7:6	Reserved	Writing has no effect. Read as zero.	R
5:0	tWL	Write latency, please notice that this version only support AL=0.	RW

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9.5.2.6 DDR Timing Configure Register 2 (DTIMING2, 0x134F0064)

	DTIMMING2																															0x134F0064
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		tCCD						Reserved		tRAS						Reserved		tRCD						Reserved		tRL					
RST	0	0	0	0	0	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:24	tCCD	CAS# to CAS# command delay	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tRAS	ACTIVE to PRECHARGE command period. tRAS defines the ACTIVE to PRECHARGE command period to the same bank.	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tRCD	ACTIVE to READ or WRITE command period. tRCD defines the ACTIVE to READ/WRITE command period to the same bank.	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	tRL	Read latency, please notice that this version only support AL=0.	RW

9.5.2.7 DDR Timing Configure Register 3 (DTIMING3, 0x134F0068)

	DTIMMING3																															0x134F0068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	ONUM				tCKSRE			Reserved		tRP						Reserved		tRRD						Reserved		tRC					
RST	0	0	1	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30:27	ONUM	Keep to 4 in this version.	RW
26:24	tCKSRE	Valid clock after enter self-refresh(tCKSRX = tCKSRE in this version). Delay time is tCKSRE*8 (tCK)	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tRP	PRECHARGE command period. tRP defines the PRECHARGE to	RW

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		next command period to the same bank.	
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tRRD	ACTIVE bank A to ACTIVE bank B command period. tRRD defines the ACTIVE to ACTIVE command period to different banks.	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	tRC	ACTIVE to ACTIVE command period. tRC defines the ACTIVE to ACTIVE command period to the same bank.	RW

9.5.2.8 DDR Timing Configure Register 4 (DTIMING4, 0x134F006C)

	DTIMING4																															0x134F006C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		tRFC						tEXTRW			tRWCOV		tCKE			Reserved				tMINSR				Reserved	tXP			Reserved		tMRD	
RST	0	0	0	0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	1

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:24	tRFC	AUTO-REFRESH command period. tRFC defines the minimum delay after an AUTO-REFRESH command. During tRFC period, no command can be issued to DDR memory. Delay Time = (tRFC + 1)*2.	RW

tRFC	Description
000000	2 tCK.
000001	4 tCK.
000010	6 tCK.
000011	8 tCK.
… …	**… (tRFC + 1)*2 …**
111101	126 tCK.
111110	128 tCK.
111111	130 tCK.

23:21	tEXTRW	keep the default value.	R
20:19	tRWCOV	keep the default value.	
18:16	tCKE	minimum CKE pulse width. tCKE define the minimum CKE pulse width, include high level and low level.	RW

Bit [18:16]	Description

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			000	1 tCK.	
			001	2 tCK.	
			010	3 tCK.	
			011	4 tCK.	
			100	5 tCK.	
			101	6 tCK.	
			110	7 tCK.	
			111	8 tCK.	
15:12	Reserved	Writing has no effect, read as zero.			R
11:8	tMINSR	Minimum Self-Refresh / Deep-Power-Down time. After DDR memory turns into Self-Refresh or Deep-Power-Down mode, it will NOT exit until tMINSR condition meets. Delay Time = (tMINSR+1) * 8.			RW
			Bit [11:8]	**Description**	
			0000	8 tCK.	
			0001	16 tCK.	
			0010	24 tCK.	
			0011	32 tCK.	
			… …	**… (tMINSR+1) * 8 …**	
7	Reserved	Writing has no effect, read as zero.			R
6:4	tXP	EXIT-POWER-DOWN to next valid command period. tXP defines the EXIT-POWER-DOWN to next valid command period to all banks.			RW
3:2	Reserved	Writing has no effect, read as zero.			R
1:0	tMRD	Load-Mode-Register to next valid command period. tMRD defines the Load-Mode-Register to next valid command period.			
			tMRD	**Description**	
			00	1 tCK.	
			01	2 tCK.	
			10	3 tCK.	
			11	4 tCK.	

9.5.2.9 DDR Timing Configure Register 5 (DTIMING5, 0x134F0070)

	DTIMMING5																															0x134F0070
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tCTLUPD								Reserved		tRTW						Reserved		tRDLAT						Reserved		tWDLAT					
RST	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

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Bits	Name	Description	RW
31:24	tCTLUPD	Inner usage. Not need to change.	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tRTW	Read to Write latency.	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tRDLAT	tRL-2. (when use LPDDR2, set tRDLAT=tRL).	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	tWDLAT	tWL-1(when use LPDDR2, set tWDLAT=tWL).	RW

9.5.2.10 DDR Timing Configure Register 6 (DTIMING6, 0x134F0074)

	DTIMING6																															0x134F0074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tXSRD								Reserved		tFAW						Reserved		tCFGW						Reserved		tCFGR					
RST	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
31:24	tXSRD	exit self-refresh to READ delay. Delay time is tXSRD*4 (tCK)	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tFAW	4-active command window.	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tCFGW	Write PHY configure registers to other commands delay. Not need to change.	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	tCFGR	Ready PHY configure registers to other commands delay. Not need to change.	RW

9.5.2.11 DDR Auto-Refresh Counter (DREFCNT, 0x134f0018)

	DREFCNT																															0x134f0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CON								CNT								Reserved				CLK_DIV			REF_EN
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	CON	A constant value used to compare with the CNT value. After reset, CON=0xFF and CNT=0x00; It is not recommended to set CON=0x00.	
15:8	CNT	8-bit counter; When the value of CNT match the value of CON, flag bit EQU is set high and an auto-refresh command will be issued to DDR memory. READ only.	
7:4	Reserved	Writing has no effect, read as zero.	R
3:1	CLK_DIV	Clock Divider. Divide the dclk to generate a lower frequency of clock to drive the auto-refresh counter. This helps to save power consumption. Set CLK_DIV=0 can disable the clock to auto-refresh counter. When the DDR memory is in self-refresh mode or in deep-power-down mode, disable the clock of auto-refresh counter can save power consumption. Future more, the module clock to DDRC can also be stopped. dclk is CKO clock, When ddr work in 500Mbps, dclk is 250Mhz. <table><tr><th>Bit [3:1]</th><th>Description</th></tr><tr><td>000</td><td>dclk / 16.</td></tr><tr><td>001</td><td>dclk / 32.</td></tr><tr><td>010</td><td>dclk / 64.</td></tr><tr><td>011</td><td>dclk / 128.</td></tr><tr><td>100</td><td>dclk / 256.</td></tr><tr><td>101</td><td>dclk / 512.</td></tr><tr><td>110</td><td>dclk / 1024.</td></tr><tr><td>111</td><td>--</td></tr></table>	
0	REF_EN	Enable Refresh Counter. Software set REF_EN=1 right after initialize ddr memory. <table><tr><th>Bit [29]</th><th>Description</th></tr><tr><td>0</td><td>Disenable auto-refresh counter.</td></tr><tr><td>1</td><td>Enable auto-refresh counter.</td></tr></table>	

9.5.2.12 DDR Memory CS0 Map Configure Register (DMMAP0, 0x134f0024)

The physical base address and size of external DDR Memory can be configured by DMMAP register. The size of external DDR Memory must be: **2^(24+n), n=0, 1, 2, 3, …**.

When the following equation is met:

(AXI_BUS_Address[31:24] & MASK[7:0]) == BASE

The DDR Memory is selected.

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	DMMAP0																															0x134f0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	BASE	base address.	RW
7:0	MASK	address mask.	RW

Examples:

1 DDR address space in system memory : 0x2000_0000 ~ 0x2FFF_FFFF (256MB)
BASE=0x20 MASK=0xF0.

2 DDR address space in system memory : 0x5000_0000 ~ 0x57FF_FFFF (128MB)
BASE=0x50 MASK=0xF8.

NOTE: If DDRC is disabled, please set DMMAP=0x0000_FF00 (reset value).

9.5.2.13 DDR Memory CS1 Map Configure Register (DMMAP1, 0x134f0028)

The physical base address and size of external DDR Memory can be configured by DMMAP register.

The size of external DDR Memory must be: **2^(24+n), n=0, 1, 2, 3, ….**

When the following equation is met:

(AXI_BUS_Address[31:24] & MASK[7:0]) == BASE

The DDR Memory is selected.

	DMMAP1																															0x134f0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	BASE	base address.	RW
7:0	MASK	address mask.	RW

Examples:

1 DDR address space in system memory : 0x2000_0000 ~ 0x2FFF_FFFF (256MB)

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BASE=0x20 MASK=0xF0.

2 DDR address space in system memory : 0x5000_0000 ~ 0x57FF_FFFF (128MB)

BASE=0x50 MASK=0xF8.

NOTE: If DDRC is disabled, please set DMMAP=0x0000_FF00 (reset value).

9.5.2.14 DDR DFI low power handshake control register (DDLP, 0x134f00BC)

	DDLP																															0x134f00BC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													Only	UAR	UZQ	SLP				FLP				Reserved					FSR	FPD	LPEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect. Read as zero.	R
18	Only	Inner usage, keep to 0	RW
17	UAR	Inner usage, keep to 0	RW
16	UZQ	Inner usage, keep to 0	RW
15:12	SLP	slow LP handshake timing register. Just keep it as reset value.	RW
11:8	FLP	fast LP handshake timing register. Just keep it as reset value.	RW
7:3	Reserved	Writing has no effect. Read as zero.	R
2	FSR	1: Use fast lp handshake process during self-refresh. 0: Use slow lp handshake process during self-refresh.	RW
1	FPD	1: Use fast lp handshake process during power down. 0: Use slow lp handshake process during power down.	RW
0	LPEN	DFI low power(lp) interface enable.	RW

9.5.2.15 DDR Address Remapping Register 1 (DREMAP1, 0x134f009C)

	DREMAP1																															0x134f009C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT3MP					Reserved			BIT2MP					Reserved				BIT1MP				Reserved			BIT0MP				
RST	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

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9.5.2.16 DDR Address Remapping Register 2 (DREMAP2, 0x134f00A0)

	DREMAP2																															0x134f00A0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT7MP					Reserved			BIT6MP					Reserved			BIT5MP					Reserved			BIT4MP				
RST	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0

9.5.2.17 DDR Address Remapping Register 3 (DREMAP3, 0x134f00A4)

	DREMAP3																															0x134f00A4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT11MP					Reserved			BIT10MP					Reserved			BIT9MP					Reserved			BIT8MP				
RST	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0

9.5.2.18 DDR Address Remapping Register 4 (DREMAP4, 0x134f00A8)

	DREMAP4																															0x134f00A8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT15MP					Reserved			BIT14MP					Reserved			BIT13MP					Reserved			BIT12MP				
RST	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	1	0	0	0	0	1	1	0	0

9.5.2.19 DDR Address Remapping Register 5 (DREMAP5, 0x134f00AC)

	DREMAP5																															0x134f00AC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT19MP					Reserved			BIT18MP					Reserved			BIT17MP					Reserved			BIT16MP				
RST	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

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DREMAP1~5 are used to define address mapping in DDRC. The “BITnMP” represents address[31:20]. The low 4KB(bit [11:0]) address are reserved without any change. The high 20 bits are configurable. For example, If you want to remap address between address[27:25] and address[14:12], you can set BIT12MP as 0, BIT13MP as 1, BIT14MP as 2, BIT0MP as 12, BIT1MP as 13 and BIT2MP as 14.

Original address:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11~0
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Reserved

Remapped address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11~0
19	18	17	16	2	1	0	12	11	10	9	8	7	6	5	4	3	15	14	13	Reserved

9.5.2.20 Performance wcmd reorder & grouping (WCMDCTRL1, 0x134f0100)

Terminology:

Priority: priority of command, the command with higher priority will be processed prior to that with lower priority. The priority is generated from:

1. on-port control signals (hpri, ARPRI, AWPRI)
2. iport_pri (register configurable for each port)
3. QoS counter

Page-hit-conflit:

Page-hit: wpage-hit

Page-conflict: the page of write command is conflict with the page of read command. In this case, to guarantee the read-write coherency, the write command must be process prior to read command.

	WCMDCTRL1																															**0x134f0100**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserve					wpage_hit_max								pend_qos_cnt												wram_in_use					disable_reorder	msk_empty_wfifo
RST	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:19	wpage_hit_max	Wpage-hit affects the reorder of wcmd, the wcmd with same page should be bonded for higher performance. This register indicates the maximum number of wcmd to be bonded.	RW

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		Higher value improves total bandwidth of ddr, but leads to longer read maximum latency.	
18:7	pend_qos_cnt	Once the wcmd is accepted, a counter indicates how long the command is pending, when the pending time is exceed Pend_QoS once, the priority of this command will increase 1, up to 3, which increases the priority to be processed. This mechanism avoids the wcmd with lower priority pending too long. Range: 0x001 ~0xFFF **NOTE**: configure step: 1. set d*isable_reorder* to 0. 2. execute *step1* for 14 times 3. set wcmd_pend_qos to expect value 4. set disable_reorder to 1, (Optional) Higher value improves total bandwidth of ddr, but leads to longer maximum latency for write command with lower priority. **Dynamic configuration is not supported.**	RW
6:2	wram_in_use	0~12. Ram to be used in write command reorder. Reduction of this number leads to poor performance. **Configuration is not recommended**	RW
1	disable_reorder	0: wcmd will be reordered based on priority and page-hit-conflict 1: wcmd will not be reordered, the commands will be process with the order of being received. **Dynamic configuration is not recommended.**	RW
0	msk_empty_wfifo	0: wcmd is involved in arbitration immediately. 1: wcmd is not involved in arbitration until receives enough wdata.	RW

9.5.2.21 Performance rcmd request control (RCMDCTRL0, 0x134f0104)

Terminology:

rfifo_thd: read fifo threshold. Read command is not involved in arbitration until the vacancy in rfifo is higher than rfifo threshold. This should improves the ddr performance when processing accessing discrete pages. However, for page-access (commands access the same page continuously) the performance will be lagged as the threshold affects the command grouping.

rcmd_igr_cflit: guarantee coherency between wcmd and rcmd. If the coherency if not required in some application (such as LCD), ignoring of confliction would improve ddr read performance.

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	RCMDCTRL0																															0x134f0104
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ch3_rcmd_igr_cflit	ch3_rfifo_thd_en	ch3_rfifo_thd						Reserved								ch1_rcmd_igr_cflit	ch1_rfifo_thd_en	ch1_rfifo_thd						Reserved							
RST	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0

Bits	Name	Description	RW
31	ch3_rcmd_igr_cflit	1: enable. Consistence between wcmd and rcmd will not be guaranteed. 0: disable.	RW
30	ch3_fifo_thd_en	0: disable rfifo_thd (recommanded) 1: enable rfifo_thd	RW
29:24	ch3_rfifo_thd	If Ch3 rfifo level threshold higher than this value, rcmd request is masked	RW
23:16	Reserved	Writing has no effect, read as zero.	R
15	ch1_rcmd_igr_cflit	1: enable. Consistence between wcmd and rcmd will not be guaranteed. 0: disable.	RW
14	ch1_fifo_thd_en	0: disable rfifo_thd (recommanded) 1: enable rfifo_thd	RW
13:8	ch1_rfifo_thd	If Ch3 rfifo level threshold higher than this value, rcmd request is masked	RW
7:0	Reserved	Writing has no effect, read as zero.	R

9.5.2.22 Performance rcmd request control (RCMDCTRL1, 0x134f0108)

	RCMDCTRL1																															0x134f0108
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Ch5_rcmd_igr_cflit	Ch5_rfifo_thd_en	Ch5_rfifo_thd						Ch4_rcmd_igr_cflit	Ch4_rfifo_thd_en	Ch4_rfifo_thd					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description	Reset
31:16	Reserved	Writing has no effect, read as zero.	R
15	ch5_rcmd_igr_cflit	0: disable rfifo_thd (recommended)	RW

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		1: enable rfifo_thd	
14	ch5_fifo_thd_en	1: enable. consistence between wcmd and rcmd will not be guaranteed. 0: disable.	RW
13:8	ch5_rfifo_thd	If Ch1 rfifo level threshold higher than this value, rcmd request is masked	RW
7	ch4_rcmd_igr_cflit	0: disable rfifo_thd (recommended) 1: enable rfifo_thd	RW
6	ch4_fifo_thd_en	1: enable. consistence between wcmd and rcmd will not be guaranteed. 0: disable.	RW
5:0	ch4_rfifo_thd	If Ch1 rfifo level threshold higher than this value, rcmd request is masked	RW

9.5.2.23 Channel boundary select (BOUNDARYSEL, 0x134f010C)

	BOUNDARYSEL																															0x134f010C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	CH6_block_wready	CH5_block_wready	CH4_block_wready	CH3_block_wready	CH2_block_wready	CH1_block_wready	CH0_block_wready	Reserved								CH7_boundary		CH6_boundary		CH5_boundary		CH4_boundary		CH3_boundary		CH2_boundary		CH1_boundary		CH0_boundary	
RST	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	Reset
31	Reserved	Writing has no effect, read as zero.	R
30	CH6_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
29	CH5_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
28	CH4_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
27	CH3_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
26	CH2_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW

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25	CH1_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
24	CH0_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
23:16	Reserved	Writing has no effect, read as zero.	R
15:14	CH7_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
13:12	CH6_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
11:10	CH5_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
9:8	CH4_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
7:6	CH3_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
5:4	CH2_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
3:2	CH1_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
1:0	CH0_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW

9.5.2.24 performance wcmd request control (WDATTHD0, 0x134f0114)

Terminology:

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Wfifo_thd: wdata fifo threshold. In axi port, as the wdata might be far behind of wcmd. The threshold guarantees the wcmd will not be involved in arbitration until receive enough wdata. 11

	WDATTHD0																															0x134f0114
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	Ch3_wfifo_thd_en	Ch3_wfifo_thd						Reserved									Ch1_wfifo_thd_en	Ch1_wfifo_thd						Reserved							
RST	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	Ch3_wfifo_thd_en	1: Enable 1: Disable (recommended)	RW
29:24	Ch3_wfifo_thd	Wcmd is involved in arbitration before receiving all wdata.	RW
23:15	Reserved	Writing has no effect, read as zero.	R
14	Ch1_wfifo_thd_en	1: Enable 1: Disable (recommended)	RW
13:8	Ch1_wfifo_thd	Wcmd is involved in arbitration before receiving all wdata.	RW
7:0	Reserved	Writing has no effect, read as zero.	R

9.5.2.25 performance wcmd request control (WDATTHD1, 0x134f0118)

	WDATTHD1																															**0x134f0118**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	Ch5_wfifo_thd_en	Ch5_wfifo_thd						Reserved	Ch4_wfifo_thd_en	Ch4_wfifo_thd					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description	RW
31:15	Reserved	Writing has no effect, read as zero.	R
14	Ch5_wfifo_thd_en	1: Enable 1: Disable (recommended)	RW
13:8	Ch5_wfifo_thd	Wcmd is involved in arbitration before receiving all wdata.	RW
7	Reserved	Writing has no effect, read as zero.	R

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6	Ch4_wfifo_thd_en	1: Enable 1: Disable (recommended)	RW
5:0	Ch4_wfifo_thd	Wcmd is involved in arbitration before receiving all wdata.	RW

9.5.2.26 performance priority control (IPORTPRI, 0x134f0240)

Terminology:

Priority affects on arbitration between ports. Transfers with higher priority will be grant first

Port_pri: priority provided by masters.

Iport_pri: register configurable which applies to each ports. The finial priority is the larger value of port_pri and iport_pri.

	IPORTWPRI																															0x134f0240
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								Ch7_iport_wpri_en	Ch6_iport_wpri_en	Ch5_iport_wpri_en	Ch4_iport_wpri_en	Ch3_iport_wpri_en	Ch2_iport_wpri_en	Ch1_iport_wpri_en	Ch0_iport_wpri_en	Ch7_iport_wpri		Ch6_iport_wpri		Ch5_iport_wpri		Ch4_iport_wpri		Ch3_iport_wpri		Ch2_iport_wpri		Ch1_iport_wpri		Ch0_iport_wpri	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	IPORTRPRI																															0x134f0244
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								Ch7_iport_rpri_en	Ch6_iport_rptr_en	Ch5_iport_rptr_en	Ch4_iport_rptr_en	Ch3_iport_rptr_en	Ch2_iport_rptr_en	Ch1_iport_rptr_en	Ch0_iport_rptr_en	Ch7_iport_rptr		Ch6_iport_rptr		Ch5_iport_rptr		Ch4_iport_rptr		Ch3_iport_rptr		Ch2_iport_rptr		Ch1_iport_rptr		Ch0_iport_rptr	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	Chn_iport_wpri_en Chn_iport_rpri_en	Enable iport_pri (iport_wpri is write channel priority, Iport rpri is read channel priority) 0: disable, use external priority 1: enable, use the max priority of external and internal priority	RW
15:0	Chn_iport_wpri	Priority of channel	RW

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	Chn_iport_rpri	0x3: the highest priority ... 0x0: the lowest priority	

9.5.2.27 performance QoS control (CHxQOS0,1,2,3,4,5)

Terminology:

Qos: Generally speaking, the Qos controller is a timer, it indicates the how long the command is pending. Once the timer exceed predefined threshold (con), the priority increases by 1, up to top-limit (max). The higher priority is, the sooner it will be processed. This register affects the latency.

	CHxWQOS0,1,2,3,4,5,6																															0x134f0200,204,208,20C,210,214,218
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Qos_en	Outstanding_en	Reserved												max		con															
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	CHxRQOS0,1,2,3,4,5,6																															0x134f0300,304,308,30C,310,314,318
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Qos_en	Outstanding_en	Reserved												max		con															
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Qos_en	enable	RW
30	Outstand_en	Outstand enable	RW
29:18	Reserved	Writing has no effect, read as zero.	R
17:16	Max	Up-limit of priority	RW
15:0	Con	Threshold of timer	RW

9.5.2.28 Auto Self Refresh counter configuration (AUTOSR_CNT, 0xB3010308)

Terminology:

AUTOSR: auto self-refresh. When the DDRC bus interface is idle for some time, the DDRC can issue a command to put the DRAM into self-refresh mode. This will same much power in off-chip DRAM.

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	AUTOSR_CNT																															0xB3010308
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												BUS_IDLE_CNT																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:0	BUS_IDLE_CNT	Timer Cnt: when the bus interface is idle(all transfer are finished), the internal timer is going to run, after the Timer Cnt is meet, DDR issues Self-Refresh command.	RW

9.5.2.29 Auto Self Refresh enable (AUTOSR_EN, 0xb3010304)

	AUTOSR_EN																															0xb3010304
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															AUTOSR_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	BUS_IDLE_EN	0: disable auto self-refresh 1: enable auto self-refresh	RW

9.5.2.30 Auto Clock Gating configuration (CLKSTP_CFG, 0xB3012068)

Description:

Under certain condition, the DDRC input clock can be stopped for power saving. For example, when the SDRAM is in self-refresh mode, the clock can be stop.

	CLKSTP_CFG																															0xB3012068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	clkstp_en	idle_cond_en	lp_cond_en	sr_cond_en	Reserved																dly_timer											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

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Bits	Name	Description	RW
31	clkstp_en	Function enable	RW
30	idle_cond_en	Enable judge condition: ddrc idle	RW
29	lp_cond_en	Enable judge condition: low-power mode (DCTRL.PDT)	RW
28	sr_cond_en	Enable judge condition: self-refresh	RW
27:12	Reserved	Writing has no effect, read as zero.	R
11:0	dly_timer	Specify the time before shutting down the clock after all condition met.	RW

Please Note that:

The CLKSTP will affect the function of lp(low power mode), auto-sr(auto self-refresh)mode. If the Clock is gating, the timer used for lp/auto-sr will stop running. As a result, if the Auto-self-refresh enabled, the bit [28] should be set.

9.5.2.31 DDR status (DDRC_STATUS, 0xB301206C)

Description:

Read-Only register indicates the ddrc status. This register can be accessed even in DDR retention mode.

	DDRC_STATUS																															0xB301206C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													ckc_reject	ckc_ack	ckc_req	Reserved		ddr_sr_mode	ddr_lp_mode	ddrc_idle	ch6_bus_idle	ch5_bus_idle	ch4_bus_idle	ch3_bus_idle	ch2_bus_idle	ch1_bus_idle	ch0_bus_idle	Reserved			clkstp_req
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	ckc_reject		R
17	ckc_ack		R
16	ckc_req		R
15:14	Reserved	Writing has no effect, read as zero.	R
13	ddr_sr_mode	0: DRAM is not in self-refresh mode 1: DRAM is in self-refresh mode	R
12	ddr_lp_mode	0: ddr PHY is not in low-power mode 1: ddr PHY is in low-power mode	R
11	ddrc_idle	Indicates the ddrc control logic is idle	R
10:4	ch*x*_bus_idle	Indicates the bus interface for each channel is idle	R
3:1	Reserved	Writing has no effect, read as zero.	R
0	clkstp_req	Indicates the ddrc is requiring CPM gating ddrc clock	R

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9.5.2.32 Retention Mode Configuration (PHYRET_CFG, 0xB3012034)

Description:

DDR PHY can be set into retention mode, which allow power cutting-down. This can save the leakage power in highest level.

However, when use this function, please flow the retention flow.

	PHYRET_CFG																															0xB3012034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			cfg_iso_en	Reserved			phy_iso_en	Reserved			clk_iso_en	Reserved		ret_en_n	ret_en
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Name	Description	RW
31:13	Reserved	Writing has no effect, read as zero.	R
12	cfg_iso_en	PHY output prdata isolation enable	RW
11:9	Reserved	Writing has no effect, read as zero.	R
8	phy_iso_en	PHY output dfi signal isolation enable (high-active)	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	clk_iso_en	PHY output clock isolation enable	RW
3:2	Reserved	Writing has no effect, read as zero.	R
1	ret_en_n	Retention enable: low-active	RW
0	ret_en	Retention enable: High-active (make sure: ret_en = ~ret_en_n)	RW

9.5.2.33 DDR Phy reset control (PHYRST_CFG, 0xB3012080)

Soft Reset of DDRC

	REG_NAME																															0xB3012080
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							dfi_reset	dll_reset	ctl_reset	cfg_reset	Reserved																				phy_reset
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	dfi_reset	Soft reset of dfi	RW

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23	dll_reset	Soft reset of dll	RW
22	ctl_reset	Soft reset of ctl	RW
21	cfg_reset	Soft reset of cfg	RW
20:1	Reserved	Writing has no effect, read as zero.	R
0	phy_reset	Soft reset of PHY	RW

9.5.2.34 DFI initial configuration (PHY_INIT, 0xB301208c)

	PHY_INIT																															0xB301208c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													ddr_plllock	init_complete	Init_start
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2	ddr_plllock	0: PLL UNLOCKED 1: PLL LOCKED PHY output	R
1	init_complete	PHY output dfi_init_complete signal	R
0	init_start	0: configure signal dfi_init_start low 1: configure signal dfi_init_start high	RW

9.5.2.35 CPM register, DLL & Clock control for DDR (CPM_DRCG, 0xB00000D0)

	CPM_DRCG																															0xB00000D0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									GATEN	Reserved			CFGRST	DLLRESET	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:7	Reserved	Inner usage, keep in default value	R
6	GATEN	Inner usage, keep to 1	RW
5:3	Reserved	Writing has no effect, read as zero.	R
2	CFGRST	1: reset the DDR PHY Configure Port	RW

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		0: disable the reset.	
1	DLLRESET	1: reset the DLL in DDR PHY 0: disable the reset.	RW
0	Reserved	Inner usage, keep in default value	RW

9.6 Functional Description

9.6.1 DDRC and DDR2 Memory Initialization Sequence

The following content is just an example for initialization, the sequence is already implementation in our BSP。

Example

One 512Mb x16 DDR2 device connected on CS0;
No memory device connected on CS1;
DCK = 133 MHz, CL = 3.

1 After system reset, wait system clock stable before initialize DDRC.
2 Configure the Clock-Control module for DDRC clocks.
3 DDR Memory device need at least 200us initialization time after power-on before it can accept any command.

//----------
// INIT DDRC
//----------
4 Configure DCFG = 0x.
5 Configure DTIMING1~6 = 0x.
6 Configure DMMAP0 = 0x.
7 Configure DMMAP1 = 0x0000FF00.
//----------
// INIT DDR PHY
//----------
8 Configure DDR PHY and finish PHY training process.(relate to DDRPHY spec)
//----------
// DDRC performance control configure (optional)
//----------
9 Configure RCMDCTRL0 = 0x08080808 (optional)
10 Configure RCMDCTRL1 = 0x00000808 (optional)
11 Configure WDATTHD0 = 0x08080808 (optional)
12 Configure WDATTHD1 = 0x00000808 (optional)
//----------
// INIT DDR memory device
//----------
13 Set CKE Pin HIGH : Configure DCTRL = 0x00000002.
//----------
// Enable Refresh Counter

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//----------
14 Enable Refresh Counter : Configure DREFCNT = 0x.
15 AUTO-REFRESH : Configure DCTRL = 0x.
//----------
// END INITIALIZING SEQUENCE
//----------

9.7 Change Clock Frequency

To reduce power consumption, the system clock frequency may be changed frequently according to the application. There are 3 ways to change the clock frequency.

9.7.1 Manually SELF-REFRESH Mode

DDR can stay in SELF-REFRESH & DEEP-POWER-DOWN mode for a long period of time. System clock frequency can be changed during this time. Even more, the clocks to DDRC module can also be stopped to save power-consumption.

Reference Sequence:

1. Manually issue SELF-REFRESH command to DDR.
2. Change relative register in CPM.
3. Change system clock frequency.
4. Drive DDR exit SELF-REFRESH mode.

9.7.2 CPM driven SELF-REFRESH Mode

CPM will auto drive DDRC to self-refresh mode, when use ddr2, ddr3.

To change clock frequency, please refer CPM spec.

9.7.3 DLL bypass mode

The clock frequency on which DLL in ddr phy works much faster than 200MHz, As the result, when ddr clock is failed to meet this condition (for example, work in 12MHz) , the DLL must be bypassed in order to supply clock to ddr controller.

Step1, Configure DLL into reset mode to guarantee a driving clock.

(0xB00000D0) CPM_DRCG[1] <= 1;

Step2, Configure DLL into bypass mode.

(0xB3011014) DDR_ACDLLCR[0] <= 1;

Then, (0xB00000D0) CPM_DRCG[1] <= 0;

9.8 Data Endian

Fix to little Endian.

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9.9 Retention Flow

9.9.1 Enter Retention mode

Description:

S0: Prepare Retention Program

Before perform retention enter flow, the program for this flow should be mapped to on chip RAM (such as TCSM in PDMA), during retention mode, any content in DRAM is not accessible. The PC of CPU should jump out of DDR range to on chip RAM

S1: Disable All Bus

Disable all device which addressing DDR, only DDRC APB/ DDRP APB port can be active.

S2: Put DRAM in self-refresh mode

there are two ways to drive DRAM into self-refresh

1. manually configuration (please refer DCTRL.SR)
2. Auto-self-refresh (AUTOSR_EN) (*recommended*)

polling the DDRC_STATUS.ddr_sr_mode to make sure the DRAM is in self-refresh mode

S3: Read ZQ value and reserve it future use.

(refer: X1000_ddrphy_spec: ZQnSR0.ZCTRL)

S4: Enable signal isolation

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PHYRET_CFG.cfg_iso_en <= 1
PHYRET_CFG.clk_iso_en <= 1

S5: Assert DDR PHY Retention

PHYRET_CFG.ret_en <= 1
PHYRET_CFG.ret_en_n <= 0

S6: Remove Power

please refer Power off sequence

S7: Further Operation for power saving

- Configure CPM, gating DDR clock
- Others

Now, the DDR is safely in retention mode, any transfer to DDR from CH0~CH6 is forbidden. Please refer 'Exit Retention mode' for wake DDR

Please note that, the retention mode is only used in system sleep mode, which still powering on GPIO. Because GPIO is must for exiting retention operation.

9.9.2 Exit Retention mode

Soft ware control flow

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Description:

S1: Ready for Power-On

S2: Restore DDR Power

Please refer Sequence of DDR Power up.

S3: Guarantee clock

- Turn off CPM: ddr gating if it is gated in '*Enter Retention Mode: S7*'.
- Disable PHY clock isolation
  PHYRET_CFG.clk_iso_en <= 0
- Disable Auto-clk-stp mode
  CLKSTP.clkstp_en <= 0

S4: Soft reset DDR PHY

1) PHYRST_CFT.*_reset <= 1
2) Delay for some cycles
3) PHYRST_CFT.*_reset <= 0

S5: Reconfigure PUBL registers

Please refer '*X1000_ddrphy_spec*'

S6: Set ZQ bypass enable

DDR_PHY_PIR.ZCLBYP <= 1

S7: Polling register

DDR_PHY_PGSR.IDONE = 1

S8: Override ZQ

DDR_PHY_ZQnCR0.ZDEN <= 1 + DDR_PHY_ZQnCR0.ZDATA <= previous value (in '*Enter Retention Mode: S3*').

S9: De-assert ret_en

PHYRET_CFG.ret_en <= 0 + PHYRET_CFG.ret_en_n <= 1

S10: Override ZQ disable

DDR_PHY_ZQnCR0.ZDEN <= 0

S11: Trigger ZQ Calibration

DDR_PHY_PIR.ZQCAL <= 1 + DDR_PHY_PIR.INIT <= 1

S12: Polling register

DDR_PHY_PGSR.IDONE = 1

S13: Grant DFI bus to DDRC

DDR_PHY_PIR.CTLDINIT <= 1 + DDR_PHY_PIR.INIT <= 1

S14: Polling register

DDR_PHY_PGSR.IDONE = 1

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S15: Disable signal isolation

PHYRET_CFG.cfg_iso_en <= 0

S16: Exit self-refresh

- If system works in Auto-self-refresh mode, disable this function
  AUTOSR_EN <= 0
- if works in manually self-refresh mode. Configure register to exit
  DCTL.SR <= 0

S17: Polling register to ensure ddrc exit self-refresh mode

DDRC_STATUS.ddr_sr_mode = 0

S18: Perform Data training

Please note that it will override some data in DDR, so make sure the training address is not in use.

DDR_PHY_PIR.DQTRN <= 1 + DDR_PHY_PIR.DRAMINIT <= 1

S19: Polling register

DDR_PHY_PGSR.DTDONE = 1 + DDR_PHY_PGSR.DTERR = 0

S20: Reconfigure DDRC feature:

eg:

- AUTODR_EN <= 1
- CLKSTP_CFG.clkstp_en <= 1
- ..... others .....

S21: Finish

DDR is thoroughly get out of Retention mode. Change PC to DDR for normal operation.

9.10 DDR Connection Diagrams

The following diagrams give examples on the connection to external DDR2 devices.
Note not all the possible connections are listed.

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9.10.1 Connection to one 512Mb x16 DDR2 devic

9.10.2 Connection to two 512Mb x16 DDR2 devices

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10 External Memory Controller

10.1 Overview

The External Memory Controller (EMC) divides the off-chip memory space and outputs control signals complying with specifications of various types of static memory and bus interfaces. It enables the connection of static memory such as NOR flash memory, etc. to this processor.

- Static memory interface
  - Support 2 external chip selection CS2~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8-bit or 16-bit (no byte control) bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

10.2 Pin Description

Following table list the EMC pins.

Table 10-1 EMC Pin Description

Pin Name	I/O	Signal	Description
Data Bus	I/O	SD15 – SD0	Data I/O.
Address bus	O	SA15–SA0	Address output.
Static chip select 2 ~ 1	O	CS2~1#	Chip select signal that indicates the static bank being accessed.
Read enable	O	RD# /	For Static memory read enable signal.
Write enable	O	WE# /	Static memory write enable signal.
Wait	I	Wait# /	External wait state request signal for memory-like devices.

10.3 Physical Address Space Map

Both virtual spaces and physical spaces are 32-bit wide in this architecture. Virtual addresses are translated by MMU into physical address which is further divided into several partitions for static memory, SDRAM, and internal I/O.

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Figure 10-1 Physical Address Space Map

Table 10-2 Physical Address Space Map

Start Address	End Address	Connectable Memory	Capacity
0x00000000	0x0FFFFFFF	SDRAM Memory	256MB
0x10000000	0x13FFFFFF	Internal I/O Devices	64MB

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0x14000000	0x14FFFFFF	Reserved	16MB
0x15000000	0x15FFFFFF	Reserved	16MB
0x16000000	0x1600003F	Reserved	64B
0x16000040	0x16FFFFFF	Reserved	
0x17000000	0x1700003F	Reserved	64B
0x17000040	0x17FFFFFF	Reserved	
0x18000000	0x1800003F	Reserved	64B
0x18000040	0x18FFFFFF	Reserved	
0x19000000	0x1900003F	Reserved	64B
0x19000040	0x19FFFFFF	Reserved	
0x1A000000	0x1A00FFFF	Static Memory, CS2#	64KB
0x1A000040	0x1AFFFFFF	Reserved	
0x1B000000	0x1B00FFFF	Static Memory, CS1#	64KB
0x1B000040	0x1BFFFFFF	Reserved	
0x1C000000	0x1FBFFFFF	Reserved	
0x1FC00000	0x1FC02FFF	On-chip Boot ROM (16kB)	16KB
0x1FC04000	0x1FFFFFFF	Reserved	
0x20000000	0xDFFFFFFF	SDRAM Memory	3072MB
0xE0000000	0xFFFFFFFF	Reserved	512MB

The base address and size of each memory banks are configurable. Software can re-configure these memory banks according to the actual connected memories. Following table lists the default configuration after reset.

Table 10-3 Default Configuration of EMC Chip Select Signals

Chip-Select Signal	Connected Memory	Capacity	Memory Width *1	Start Address	End Address
CS1#	Static memory bank 1	64 KB	8, 16	0x1B000000	0x1B00FFFF
CS2#	Static memory bank 2	64 KB	8, 16	0x1A000000	0x1A00FFFF

Note:

1 Data width of static memory banks can be configured to 8, 16 bits by software.

2 The 16KB address space from H'1FC00000 to H'1FC03FFF in bank 0 is mapped to on-chip boot ROM. The other memory spaces in bank 0 are not used.

10.4 Static Memory Interface

EMC provides a glueless interface to normal static memory which don't need byte control like SRAM, memory interface IO devices, etc.. It can directly control up to 2 devices using two chip select lines. Additional devices may be supported through external decoding of the address bus.

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Each chip select can directly access memory or IO devices that are 8-bits or 16-bits wide. Each device connected to a chip select line has 2 associated registers that control its operation and the access timing to the external device. The Static Memory Control Register SMCRn specifies various configurations for the device. The Static Memory Address Configuration Register SACRn specifies the base address and size for each device, enabling any device to be located anywhere in the physical address range.

The static memory interface includes the following signals:

- Six chip selects, CS2~1#
- Six address signals, SA15-SA0
- One read enable, RD#
- One write enable, WE#
- One wait pin, WAIT#

The SMT field in SMCRn registers specifies the type of memory and BW field specifies the bus width. BOOT_SEL[1:0] pin defines system boot from Nor.

10.5 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by soft write 1, set to 1 by hardware write 1, write 0 has no effect
   RWS - read and write, set to 1 by soft write 1, hardware clear to 0, soft write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - Reset to 1
   0 - reset to 0
   ? - Value unknown after reset

10.5.1 Register Memory Map

Table 10-4 Registers Memory Map Base Address

Name	Base	Description
EMC	0x13410000	EMC base address.

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The External Memory Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 10-5 Static Memory Interface Registers Map

Name	RW	Reset Value	Address Offset	Access Size
SMCR1	RW	0x0FFF_7700	0x0014	32
SMCR2	RW	0x0FFF_7700	0x0018	32
SACR1	RW	0x0000_1BFE	0x0034	32
SACR2	RW	0x0000_1AFE	0x0038	32

10.5.2 Register and Fields Description

10.5.2.1 Static Memory Control Register 1 (SMCR1, 0x0014)

SMCR1 are 32-bit read/write registers that contain control bits for static memory. On reset, SMCR1 is initialized to 0x0FFF7700.

	SMCR1																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		STRV						TAW				TBP				TAH				TAS				BW		Reserved			BL		SMT
RST	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:24	STRV	**Static Memory Recovery Time.** Its value is the number of idle cycles (0~63 cycles) inserted between bus cycles when switching from one bank to another bank or between a read access to a write access in the same bank. Its initial value is 0xF (15 cycles).	RW
23:20	TAW	**Access Wait Time.** For normal memory, these bits specify the number of wait cycles to be inserted in read strobe time. For burst ROM, these bits specify the number of wait cycles to be inserted in first data read strobe time. **TAW3~0 Wait cycle Wait# Pin** 0000 0 cycle Ignored 0001 1 cycle Enabled 0010 2 cycles Enabled 0011 3 cycles Enabled 0100 4 cycles Enabled 0101 5 cycles Enabled 0110 6 cycles Enabled	RW

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		0111 7 cycles Enabled 1000 8 cycles Enabled 1001 9 cycles Enabled 1010 10 cycles Enabled 1011 12 cycles Enabled 1100 15 cycles Enabled 1101 20 cycles Enabled 1110 25 cycles Enabled 1111 31 cycles Enabled (Initial Value)	
19:16	TBP	**Burst Pitch Time.** For burst ROM, these bits specify the number of wait cycles to be inserted in subsequent access. For normal memory, these bits specify the number of wait cycles to be inserted in write strobe time. **TBP3~0 Wait cycle Wait# Pin** 0000 0 cycle Ignored 0001 1 cycle Enabled 0010 2 cycles Enabled 0011 3 cycles Enabled 0100 4 cycles Enabled 0101 5 cycles Enabled 0110 6 cycles Enabled 0111 7 cycles Enabled 1000 8 cycles Enabled 1001 9 cycles Enabled 1010 10 cycles Enabled 1011 12 cycles Enabled 1100 15 cycles Enabled 1101 20 cycles Enabled 1110 25 cycles Enabled 1111 31 cycles Enabled (Initial Value)	RW
15:12	TAH	**Address Hold Time.** These bits specify the number of wait cycles to be inserted from negation of read/write strobe to address. **TAH2~0 Wait cycle** 0000 0 cycle 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles (Initial Value) 1000 8 cycles	RW

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		1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	
11:8	TAS	**Address Setup Time.** These bits specify the number of wait cycles (0~15 cycles) to be inserted from address to assertion of read/write strobe. **TAS2~0 Wait cycle** 000 0 cycle 001 1 cycle 010 2 cycles 011 3 cycles 100 4 cycles 101 5 cycles 110 6 cycles 111 7 cycles (Initial Value) 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	RW
7:6	BW	**Bus Width.** These bits specify the bus width. this filed is writeable and are initialized to 0 by a reset. **BW1~0 Bus Width** 00 8 bits (Initial Value) 01 16 bits 10 Reserved 11 Reserved	RW
5:3	Reserved	Writing has no effect, read as zero. **Note:** Don't write Bit3 to 1.	R
2:1	BL	**Burst Length (BL1, BL0).** When Burst ROM is connected; these bits specify the number of burst in an access. These bits are only valid when SMT is set to 1. **BL1~0 Burst Length** 00 4 consecutive accesses. Can be used with 8- or 16-bit bus width (Initial Value)	

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		01 8 consecutive accesses. Can be used with 8- or 16-bit bus width 10 16 consecutive accesses. Can only be used with 8- or 16-bit bus width 11 32 consecutive accesses. Can only be used with 8-bit bus width	
0	SMT	**Static Memory Type (SMT).** This bit specifies the type of static memory. **SMT Description** 0 Normal Memory (Initial Value) 1 Burst ROM	RW

10.5.2.2 Static Memory Control Register 2(SMCR2, 0x0018)

SMCR2 are 32-bit read/write registers that contain control bits for static memory. On reset, SMCR2 is initialized to 0x0FFF7700.

	SMCR2																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		STRV						TAW				TBP				TAH				TAS				BW		Reserved			BL		SMT
RST	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:24	STRV	**Static Memory Recovery Time.** Its value is the number of idle cycles (0~63 cycles) inserted between bus cycles when switching from one bank to another bank or between a read access to a write access in the same bank. Its initial value is 0xF (15 cycles).	RW
23:20	TAW	**Access Wait Time.** For normal memory, these bits specify the number of wait cycles to be inserted in read strobe time. For burst ROM, these bits specify the number of wait cycles to be inserted in first data read strobe time. **TAW3~0 Wait cycle Wait# Pin** 0000 0 cycle Ignored 0001 1 cycle Enabled 0010 2 cycles Enabled 0011 3 cycles Enabled 0100 4 cycles Enabled	RW

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		0101 5 cycles Enabled 0110 6 cycles Enabled 0111 7 cycles Enabled 1000 8 cycles Enabled 1001 9 cycles Enabled 1010 10 cycles Enabled 1011 12 cycles Enabled 1100 15 cycles Enabled 1101 20 cycles Enabled 1110 25 cycles Enabled 1111 31 cycles Enabled (Initial Value)	
19:16	TBP	**Burst Pitch Time.** For burst ROM, these bits specify the number of wait cycles to be inserted in subsequent access. For normal memory, these bits specify the number of wait cycles to be inserted in write strobe time. **TBP3~0 Wait cycle Wait# Pin** 0000 0 cycle Ignored 0001 1 cycle Enabled 0010 2 cycles Enabled 0011 3 cycles Enabled 0100 4 cycles Enabled 0101 5 cycles Enabled 0110 6 cycles Enabled 0111 7 cycles Enabled 1000 8 cycles Enabled 1001 9 cycles Enabled 1010 10 cycles Enabled 1011 12 cycles Enabled 1100 15 cycles Enabled 1101 20 cycles Enabled 1110 25 cycles Enabled 1111 31 cycles Enabled (Initial Value)	RW
15:12	TAH	**Address Hold Time.** These bits specify the number of wait cycles to be inserted from negation of read/write strobe to address. **TAH2~0 Wait cycle** 0000 0 cycle 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles	RW

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		0111 7 cycles (Initial Value) 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	
11:8	TAS	**Address Setup Time.** These bits specify the number of wait cycles (0~15 cycles) to be inserted from address to assertion of read/write strobe. **TAS2~0 Wait cycle** 000 0 cycle 001 1 cycle 010 2 cycles 011 3 cycles 100 4 cycles 101 5 cycles 110 6 cycles 111 7 cycles (Initial Value) 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	RW
7:6	BW	**Bus Width.** These bits specify the bus width. this filed is writeable and are initialized to 0 by a reset. **BW1~0 Bus Width** 00 8 bits (Initial Value) 01 16 bits 10 Reserved 11 Reserved	RW
5:3	Reserved	Writing has no effect, read as zero. **Note:** Don't write Bit3 to 1.	R
2:1	BL	**Burst Length (BL1, BL0).** When Burst ROM is connected; these bits specify the number of burst in an access. These bits are only valid when SMT is set to 1. **BL1~0 Burst Length**	

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		00 4 consecutive accesses. Can be used with 8- or 16-bit bus width (Initial Value) 01 8 consecutive accesses. Can be used with 8- or 16-bit bus width 10 16 consecutive accesses. Can only be used with 8- or 16-bit bus width 11 32 consecutive accesses. Can only be used with 8-bit bus width	
0	SMT	**Static Memory Type (SMT).** This bit specifies the type of static memory. **SMT** **Description** 0 Normal Memory (Initial Value) 1 Burst ROM	RW

10.5.2.3 Static Bank Address Configuration Register1 (SACR1,0x0034)

SACR1 defines the physical address for static memory bank 1, respectively. Each register contains a base address and a mask. When the following equation is met:

(*physical_address* [31:24] & $\mathbf{MASK_1}$) == $\mathbf{BASE_1}$

The bank 1 is active. The *physical_address* is address output on internal system bus. Static bank regions must be programmed so that each bank occupies a unique area of the physical address space. Programming overlapping bank regions will result in unpredictable error. These registers are initialized by a reset.

	SACR1																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	BASE	**Address Base:** Defines the base address of Static Bank 1. The initial value is 0x1B	RW
7:0	MASK	**Address Mask**: Defines the mask of Static Bank 1. The initial value is 0xFE.	RW

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10.5.2.4 Static Bank Address Configuration Register2 (SACR2,0x0038)

SACR2 defines the physical address for static memory bank 2, respectively. Each register contains a base address and a mask. When the following equation is met:

(*physical_address* [31:24] & **MASK$_2$**) == **BASE$_2$**

The bank 2 is active. The *physical_address* is address output on internal system bus. Static bank regions must be programmed so that each bank occupies a unique area of the physical address space. Programming overlapping bank regions will result in unpredictable error. These registers are initialized by a reset.

	SACR2																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	BASE	**Address Base:** Defines the base address of Static Bank 2. The initial value is 0x1A.	RW
7:0	MASK	**Address Mask**: Defines the mask of Static Bank 2. The initial values is 0xFE.	RW

10.6 Example of Connection

Following figures shows examples of connection to 16- and 8-bit data width normal memory.

Figure 10-2 Example of 16-Bit Data Width SRAM Connection

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Figure 10-3 Example of 8-Bit Data Width SRAM Connection

10.6.1 Basic Interface

When SMT field in SMCRn (n = 1 to 2) is 0, normal memory (non-burst ROM, Flash, normal SRAM or memory-like device) is connected to bank n. When bank n (n = 1 to 2) is accessed, CSn# is asserted as soon as address is output. In addition, the RD# signal, which can be used as OE#, and write control signals WE# is asserted.

The TAS field in SMCRn is the latency from CSn# to read/write strobe. The TAW3 field is the delay time of RD# in read access. TBP3~0 field is the delay time of WE# and WEn# in write access. In addition, any number of waits can be inserted by means of the external pin (WAIT#). The TAH field is the latency from RD# and WEn# negation to CSn# negation, also the hold time to address and write data.

All kinds of normal memories (non-burst ROM, normal SRAM and Flash) have the same read and write timing. There are some requirements for writes to flash memory. Flash memory space must be un-cacheable and un-buffered. Writes must be exactly the width of the populated Flash devices on the data bus (no byte writes or word writes to a 16-bit bus, and so on). Software is responsible for partitioning commands and data, and writing them out to Flash in the appropriate sequence.

Glossary

Th – hold cycle
Tw – wait cycle
Ts – setup cycle
T1 – read inherent cycle or first write inherent cycle
T2 – last write inherent cycle
Tb – burst read inherent cycle

Following figures show the timing of normal memory. A no-wait read access is completed in one cycle and a no-wait write access is completed in two cycles. Therefore, there is no negation period in case of access at minimum pitch.

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*In this example, SMCRn:MT = 0, TAS = 0, TAW = 0, TAH = 0

Figure 10-4 Basic Timing of Normal Memory Read

*In this example, SMCRn: SMT = 0, TAS = 0, TBP = 0, TAH = 0

Figure 10-5 Basic Timing of Normal Memory Write

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*In this example, SMCRn: SMT = 0, TAS = 1, TAW = 1, TAH = 1

Figure 10-6 Normal Memory Read Timing With Wait (Software Wait Only)

*In this example, SMCRn: SMT = 0, TAS = 1, TBP = 1, TAH = 1

Figure 10-7 Normal Memory Write Timing With Wait (Software Wait Only)

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*In this example, SMCRn: SMT = 0, TAS = 1, TAW = 1, TAH=1

Figure 10-8 Normal Memory Read Timing With Wait (Wait Cycle Insertion by WAIT# pin)

10.6.2 Burst ROM Interface

Setting SMT to 1 in SMCRn allows burst ROM to be connected to bank n (n = 1 to 2). The burst ROM interface provides high-speed access to ROM that has a nibble access function. Basically, access is performed in the same way as for normal memory, but when the first cycle ends, only the address is changed before the next access is executed. When 8-bit burst ROM is connected, the number of consecutive accesses can be set as 4, 8, 16, or 32 with bits BL1~0. When 16-bit ROM is connected, 4, 8, or 16 can be set in the same way.

For burst ROM read, TAW sets the delay time from read strobe to the first data, TBP sets the delay time from consecutive address to data. Burst ROM writes have the same timing as normal memory except TAW instead of TBP is used to set the delay time of write strobe.

WAIT# pin sampling is always performed when one or more wait states are set.

Following figures show the timing of burst ROM.

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*In this example, SMT = 1, BL = 0, TAS = 1, TAW = 3,TBP = 1,TAH = 1

Figure 10-9 Burst ROM Read Timing (Software Wait Only)

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11 SPI Flash Controller(SFC)

11.1 Overview

This module is an SPI master to control the SPI flash device. Data can be transferred in CPU controlling mode or DMA mode.

Figure 11-1 SFC Schematic Diagram

11.2 Features

- SPI protocol support: Standard, Dual, Quad SPI
- transmit-only or receive-only operation
- MSB first for command and data transfer, and LSB first for address transfer
- 64 entries x 32 bits wide data FIFO
- one device select
- Configurable sampling point for reception
- Configurable timing parameters: tSLCH, tCHSH and tSHSL
- Configurable flash address wide are supported
- 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
- two data transfer mode: slave mode and DMA mode
- Configurable 6 phases for software flow

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11.3 Block Diagram

Figure 11-2 SFC Block Diagram

The AHB Interface include one slave interface and one master interface. The slave interface is used for register configuration and slave transfer mode, and the master interface is designed for DMA operation.

The FIFO block is bidirectional, used as data buffer for transmission(from AHB to device) and reception(from device to AHB).

The Flow Control module controls the operation of the 6 phases.

The Transfer mode Control act as the handler of slave mode and DMA mode.

11.4 Functional Description

11.4.1 Bus function

11.4.1.1 AHB Slave Interface

- parameter configuration
- transfer data in slave mode.
- data and address must align with 4 bytes.
- only SINGLE transfer is supported.

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11.4.1.2 AHB Master Interface

- transfer data in DMA mode
- SINGLE, INCR, INCR4, INCR8, INCR16, INCR32 are supported.

11.4.2 Configurable Timing parameter

11.4.2.1 Propagation delay

The propagation delay do not effect the data transmission, and it would not effect the data reception when the serial clock has a low frequency, as shown in the Figure 11-3

But when the serial clock run at a fast frequency, the propagation delay will cause the incoming data could not arrival at the right clock edge, then the sampling point should be adjustable as shown in the Figure 11-4

Figure 11-3 Sample point(no delay)

Figure 11-4 Sample point(has delay)

11.4.2.2 AC timing

tSETUP(tSLCH), tHOLD(tCHSH), tSH(tSHSL) are configurable.

Figure 11-5 AC timing

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11.5 Pin Description

Table 11-1 I/O Pin Description

Name	I/O	Description
SFC_CLK	Output	Serial clock
SFC_CE	Output	Device select
SFC_DT_IO0	InOut	Serial data IO0
SFC_DR_IO1	InOut	Serial data IO1
SFC_WP_IO2	InOut	Serial data IO2(WP#)
SFC_HOLD_IO3	InOut	Serial data IO3(HOLD#)

NOTE:

1. *Port "SFC_CE", in GPIO Spec named as "SFC_CE0"*
2. *Port "SFC_DT_IO0" in GPIO Spec named as "SFC_DT"*
3. *Port "SFC_DR_IO1" in GPIO Spec named as "SFC_DR"*
4. *Port "SFC_WP_IO2" in GPIO Spec named as "SFC_CE1"*
5. *Port "SFC_HOLD_IO2" in GPIO Spec named as "SFC_GPC"*

More details Please refer GPIO Spec.

11.6 Data Format Description

11.6.1 Transfer format

Figure 11-6 Data Format(Standard SPI)

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Figure 11-7 Data Format(Dual SPI)

Figure 11-8 Data Format(Quad SPI)

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11.6.2 Endian Description

Command and data are MSB first, and address is LSB first, as shown in the Figure 11-6, Figure 11-7 and Figure 11-8

11.7 Registers Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. The registers can be read and written by AHB2 bus
3. Register read/write attribute
   - ✧ R - Read only
   - ✧ W - Write only
   - ✧ RW - read and write
   - ✧ RCW - read and write, but clear to 0 by read
   - ✧ RSW - read and write, but set to 1 by read
   - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
   - ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
   - ✧ RC - read only, and clear to 0 by read
   - ✧ RS - read only, and set to 1 by read
   - ✧ SPEC - special access method, relate to its description
4. Reset Value
   - 1 - reset to 1
   - 0 - reset to 0
   - ? - value unknown after reset

11.7.1 Registers Mapping

Table 11-2 Registers Memory Map Base Address

Name	Address Base	Description
SFC	0x13440000	Address base of SFC.

The SFC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 11-3 SFC Registers Map

Name	RW	Reset Value	Address Offset	Access size
SFC_GLB	RW	0x0000_008F	0x0000	32
SFC_DEV_CONF	RW	0x0000_0027	0x0004	32
SFC_DEV_STA_EXP	RW	0x0000_0000	0x0008	32
SFC_DEV_STA_RT	R	0x0000_0000	0x000C	32

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SFC_DEV_STA_MSK	RW	0x0000_0000	0x0010	32
SFC_TRAN_CONF0	RW	0x0000_0000	0x0014	32
SFC_TRAN_CONF1	RW	0x0000_0000	0x0018	32
SFC_TRAN_CONF2	RW	0x0000_0000	0x001C	32
SFC_TRAN_CONF3	RW	0x0000_0000	0x0020	32
SFC_TRAN_CONF4	RW	0x0000_0000	0x0024	32
SFC_TRAN_CONF5	RW	0x0000_0000	0x0028	32
SFC_TRAN_LEN	RW	0x0000_0000	0x002C	32
SFC_DEV_ADR0	RW	0x0000_0000	0x0030	32
SFC_DEV_ADR1	RW	0x0000_0000	0x0034	32
SFC_DEV_ADR2	RW	0x0000_0000	0x0038	32
SFC_DEV_ADR3	RW	0x0000_0000	0x003C	32
SFC_DEV_ADR4	RW	0x0000_0000	0x0040	32
SFC_DEV_ADR5	RW	0x0000_0000	0x0044	32
SFC_DEV_PLUS0	RW	0x0000_0000	0x0048	32
SFC_DEV_PLUS1	RW	0x0000_0000	0x004C	32
SFC_DEV_PLUS2	RW	0x0000_0000	0x0050	32
SFC_DEV_PLUS3	RW	0x0000_0000	0x0054	32
SFC_DEV_PLUS4	RW	0x0000_0000	0x0058	32
SFC_DEV_PLUS5	RW	0x0000_0000	0x005C	32
SFC_MEM_ADDR	RW	0x0000_0000	0x0060	32
SFC_TRIG	RW	0x0000_0000	0x0064	32
SFC_SR	R	0x0000_0000	0x0068	32
SFC_SCR	RW	0x0000_0000	0x006C	32
SFC_INTC	RW	0x0000_001F	0x0070	32
SFC_FSM	R	0x0001_0849	0x0074	32
SFC_CGE	RW	0x0000_003F	0x0078	32
SFC_DR	RW	0x0000_0000	0x1000	32

11.7.2 Register and Fields Description

11.7.2.1 SFC Global Register(SFC_GLB,0x0000)

	SFC_GLB																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		TRAN_DIR	THRESHOLD						OP_MODE	PHASE_NUM			WP_EN	BURST_LEN	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1

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Bits	Name	Description	RW
31:14	Reserved	Write has no effect. Read as zero.	R
13	TRAN_DIR	The direction of transfer. 0: read data from SPI flash (default) 1: write data to SPI flash	RW
12:7	THRESHOLD	FIFO threshold. (unit: word) Natural number, 1-63(default is 1). Note: cannot be 0	RW
6	OP_MODE	0: slave mode (default) 1: DMA mode	RW
5:3	PHASE_NUM	The number of phase in one flow. 001: 1 phase (default) 010: 2 phases 011: 3 phases 100: 4 phases 101: 5 phases 110: 6 phases Note: cannot be 0	RW
2	WP_EN	Enable the hardware write protection 0: disable WP 1: Enable WP (default)	RW
1:0	BURST_MD	The max beats of burst. 00: INCR4 01: INCR8 10: INCR16 11: INCR32 (default)	RW

11.7.2.2 SFC Device Configure Register(SFC_DEV_CONF,0x0004)

	SFC_DEV_CONF																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														SMP_DELAY		CMD_TYPE	STA_TYPE		THOLD		TSETUP		TSH				CPHA	CPOL	CE_DL	HOLD_DL	WP_DL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1

Bits	Name	Description	RW
31:18	Reserved	Write has no effect, read as zero.	R
17:16	SMP_DELAY	Sample delay, it's depends on the device output delay, PCB delay and the IO ports delay, etc.	RW

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		00: no delay (default) 01: half SFC_CLK cycle delay 10: one SFC_CLK cycle delay 11: one and a half SFC_CLK cycle delay	
15	CMD_TYPE	0: 8bits command type (default) 1: 16bits command type	RW
14:13	STA_TYPE	used for polling 00: 1 byte status (default) 01: 2 bytes status 10: 3 bytes status 11: 4 bytes status	RW
12:11	THOLD	Hold time of SFC_CE, the time between the last edge of SFC_CLK and SFC_CE de-assertion. 00: half SFC_CLK cycle (default) 01: one SFC_CLK cycle 10: one and a half SFC_CLK cycle 11: two SFC_CLK cycle	RW
10:9	TSETUP	Setup time of SFC_CE, the time between SFC_CE assertion and the first edge of SFC_CLK. 00: half SFC_CLK cycle (default) 01: one SFC_CLK cycle 10: one and a half SFC_CLK cycle 11: two SFC_CLK cycle	RW
8:5	TSH	The min interval time between twice assertion of SFC_CE. 0000: one SFC_CLK cycle 0001: one SFC_CLK cycle(default) 0010: one and a half SFC_CLK cycle 0011: two SFC_CLK cycle 0100: two and a half SFC_CLK cycle 0101: three SFC_CLK cycle 0110: three and a half SFC_CLK cycle 0111: four SFC_CLK cycle 1000: four and a half SFC_CLK cycle 1001: five SFC_CLK cycle 1010: five and a half SFC_CLK cycle 1011: six SFC_CLK cycle 1100: six and a half SFC_CLK cycle 1101: seven SFC_CLK cycle 1110: seven and a half SFC_CLK cycle 1111: eight SFC_CLK cycle	RW
4	CPHA	This bit is used to select the SPI clock format. 0 = Sampling of data occurs at odd edges (1,3,5,...) of the SFC_CLK clock (default)	RW

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		1 = Sampling of data occurs at even edges (2,4,6,...) of the SFC_CLK clock	
3	CPOL	This bit selects the active level of SFC_CLK. 0 = Active-high clocks selected. In idle state SFC_CLK is low. (default) 1 = Active-low clocks selected. In idle state SFC_CLK is high.	RW
2	CE_DL	The default invalid level of SFC_CE pin 0: low 1: high (default)	RW
1	HOLD_DL	The default invalid level of SFC_HOLD pin 0: low 1: high (default)	RW
0	WP_DL	The default invalid level of SFC_WP pin 0: low 1: high (default)	RW

11.7.2.3 SFC Device Status Expected Register(SFC_DEV_STA_EXP,0x0008)

	SFC_DEV_STA_EXP																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_STA_EXP																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_STA_EXP	The expected value of flash status for comparing.	RW

11.7.2.4 SFC Device Status Real-time Register(SFC_DEV_STA_RT,0x000C)

	SFC_DEV_STA_RT																															Base + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_STA_RT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_STA_RT	The real-time status of SPI Flash	R

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11.7.2.5 SFC Device Status Mask Register(SFC_DEV_STA_MSK,0x0010)

	SFC_DEV_STA_MSK																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_STA_MSK																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_STA_MSK	Flash status mask for comparing. 1: this bit will be checked. 0: this bit will not be checked.	RW

11.7.2.6 SFC Transfer Configure 0 Register (SFC_TRAN_CONF0, 0x0014)

	SFC_TRAN_CONF0																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRAN_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	TRAN_MODE	Transfer mode: 000：Standard SPI（default） 001：Dual Input/Dual Output SPI 010：Dual I/O SPI 011：Full Dual I/O SPI 100：reserved 101：Quad Input/Quad Output SPI 110：Quad I/O SPI 111：Full Quad I/O SPI	RW
28:26	ADDR_WIDTH	The width of address used in the phase. 000: no address transfer (default) 001: 1 bytes 010: 2 bytes 011: 3 bytes 100: 4 bytes	RW

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		101: 5 bytes >=110: 6 bytes	
25	POLL_EN	The polling function means that SFC checking the flash device's status. 0: no polling transfer (default) 1: has polling transfer. Note: it's priority is higher than tran_dir and data_en	RW
24	CMD_EN	0: no command transfer(default) 1: has command transfer	RW
23	PHASE_FORMAT	Phase format, see chapter 11.8.1 0: format0(default) 1: format1	RW
22:17	DMY_BITS	The needed dummy cycle num (unit: SFC_CLK cycle) 000000: no dummy transfer (default) ..... 000100: 4 dummy cycles ..... 000110: 6 dummy cycles ..... 001000: 8 dummy cycles ..... 001010: 10 dummy cycles ..... 010000: 16 dummy cycles ..... 011000: 24 dummy cycles ..... 100000: 32 dummy cycles	RW
16	DATE_EN	0: no data transfer(default) 1: has data transfer	RW
15:0	CMD	The transfer command	RW

11.7.2.7 SFC Transfer Configure 1 Register (SFC_TRAN_CONF1, 0x0018)

	SFC_TRAN_CONF1																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRAN_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:29	TRAN_MODE	Transfer mode: 000：Standard SPI（default） 001：Dual Input/Dual Output SPI 010：Dual I/O SPI 011：Full Dual I/O SPI 100：reserved 101：Quad Input/Quad Output SPI 110：Quad I/O SPI 111：Full Quad I/O SPI	RW
28:26	ADDR_WIDTH	The width of address used in the phase. 000: no address transfer (default) 001: 1 bytes 010: 2 bytes 011: 3 bytes 100: 4 bytes 101: 5 bytes >=110: 6 bytes	RW
25	POLL_EN	The polling function means that SFC checking the flash device's status. 0: no polling transfer (default) 1: has polling transfer. Note: it's priority is higher than tran_dir and data_en	RW
24	CMD_EN	0: no command transfer(default) 1: has command transfer	RW
23	PHASE_FORMAT	Phase format, see chapter 11.8.1 0: format0(default) 1: format1	RW
22:17	DMY_BITS	The needed dummy cycle num (unit: SFC_CLK cycle) 000000: no dummy transfer (default) ..... 000100: 4 dummy cycles ..... 000110: 6 dummy cycles ..... 001000: 8 dummy cycles ..... 001010: 10 dummy cycles ..... 010000: 16 dummy cycles ..... 011000: 24 dummy cycles	RW

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		100000: 32 dummy cycles	
16	DATE_EN	0: no data transfer(default) 1: has data transfer	RW
15:0	CMD	The transfer command	RW

11.7.2.8 SFC Transfer Configure 2 Register (SFC_TRAN_CONF2, 0x001C)

	SFC_TRAN_CONF2																															Base + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRAN_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	TRAN_MODE	Transfer mode: 000：Standard SPI（default） 001：Dual Input/Dual Output SPI 010：Dual I/O SPI 011：Full Dual I/O SPI 100：reserved 101：Quad Input/Quad Output SPI 110：Quad I/O SPI 111：Full Quad I/O SPI	RW
28:26	ADDR_WIDTH	The width of address used in the phase. 000: no address transfer (default) 001: 1 bytes 010: 2 bytes 011: 3 bytes 100: 4 bytes 101: 5 bytes >=110: 6 bytes	RW
25	POLL_EN	The polling function means that SFC checking the flash device's status. 0: no polling transfer (default) 1: has polling transfer. Note: it's priority is higher than tran_dir and data_en	RW
24	CMD_EN	0: no command transfer(default) 1: has command transfer	RW
23	PHASE_FORMAT	Phase format, see chapter 11.8.1	RW

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		0: format0(default) 1: format1	
22:17	DMY_BITS	The needed dummy cycle num (unit: SFC_CLK cycle) 000000: no dummy transfer (default) ..... 000100: 4 dummy cycles ..... 000110: 6 dummy cycles ..... 001000: 8 dummy cycles ..... 001010: 10 dummy cycles ..... 010000: 16 dummy cycles ..... 011000: 24 dummy cycles ..... 100000: 32 dummy cycles	RW
16	DATE_EN	0: no data transfer(default) 1: has data transfer	RW
15:0	CMD	The transfer command	RW

11.7.2.9 SFC Transfer Configure 3 Register (SFC_TRAN_CONF3, 0x0020)

	SFC_TRAN_CONF3																															Base + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRAN_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	TRAN_MODE	Transfer mode: 000：Standard SPI（default） 001：Dual Input/Dual Output SPI 010：Dual I/O SPI 011：Full Dual I/O SPI 100：reserved 101：Quad Input/Quad Output SPI	RW

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		110：Quad I/O SPI 111：Full Quad I/O SPI	
28:26	ADDR_WIDTH	The width of address used in the phase. 000: no address transfer (default) 001: 1 bytes 010: 2 bytes 011: 3 bytes 100: 4 bytes 101: 5 bytes >=110: 6 bytes	RW
25	POLL_EN	The polling function means that SFC checking the flash device's status. 0: no polling transfer (default) 1: has polling transfer. Note: it's priority is higher than tran_dir and data_en	RW
24	CMD_EN	0: no command transfer(default) 1: has command transfer	RW
23	PHASE_FORMAT	Phase format, see chapter 11.8.1 0: format0(default) 1: format1	RW
22:17	DMY_BITS	The needed dummy cycle num (unit: SFC_CLK cycle) 000000: no dummy transfer (default) ..... 000100: 4 dummy cycles ..... 000110: 6 dummy cycles ..... 001000: 8 dummy cycles ..... 001010: 10 dummy cycles ..... 010000: 16 dummy cycles ..... 011000: 24 dummy cycles ..... 100000: 32 dummy cycles	RW
16	DATE_EN	0: no data transfer(default) 1: has data transfer	RW
15:0	CMD	The transfer command	RW

11.7.2.10 SFC Transfer Configure 4 Register (SFC_TRAN_CONF4, 0x0024)

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	SFC_TRAN_CONF4																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRAN_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	TRAN_MODE	Transfer mode: 000：Standard SPI（default） 001：Dual Input/Dual Output SPI 010：Dual I/O SPI 011：Full Dual I/O SPI 100：reserved 101：Quad Input/Quad Output SPI 110：Quad I/O SPI 111：Full Quad I/O SPI	RW
28:26	ADDR_WIDTH	The width of address used in the phase. 000: no address transfer (default) 001: 1 bytes 010: 2 bytes 011: 3 bytes 100: 4 bytes 101: 5 bytes >=110: 6 bytes	RW
25	POLL_EN	The polling function means that SFC checking the flash device's status. 0: no polling transfer (default) 1: has polling transfer. Note: it's priority is higher than tran_dir and data_en	RW
24	CMD_EN	0: no command transfer(default) 1: has command transfer	RW
23	PHASE_FORMAT	Phase format, see chapter 11.8.1 0: format0(default) 1: format1	RW
22:17	DMY_BITS	The needed dummy cycle num (unit: SFC_CLK cycle) 000000: no dummy transfer (default) ..... 000100: 4 dummy cycles ..... 000110: 6 dummy cycles	RW

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		..... 001000: 8 dummy cycles ..... 001010: 10 dummy cycles ..... 010000: 16 dummy cycles ..... 011000: 24 dummy cycles ..... 100000: 32 dummy cycles	
16	DATE_EN	0: no data transfer(default) 1: has data transfer	RW
15:0	CMD	The transfer command	RW

11.7.2.11 SFC Transfer Configure 5 Register (SFC_TRAN_CONF5, 0x0028)

	SFC_TRAN_CONF5																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRAN_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	TRAN_MODE	Transfer mode: 000：Standard SPI（default） 001：Dual Input/Dual Output SPI 010：Dual I/O SPI 011：Full Dual I/O SPI 100：reserved 101：Quad Input/Quad Output SPI 110：Quad I/O SPI 111：Full Quad I/O SPI	RW
28:26	ADDR_WIDTH	The width of address used in the phase. 000: no address transfer (default) 001: 1 bytes 010: 2 bytes 011: 3 bytes 100: 4 bytes 101: 5 bytes	RW

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		>=110: 6 bytes	
25	POLL_EN	The polling function means that SFC checking the flash device's status. 0: no polling transfer (default) 1: has polling transfer. Note: it's priority is higher than tran_dir and data_en	RW
24	CMD_EN	0: no command transfer(default) 1: has command transfer	RW
23	PHASE_FORMAT	Phase format, see chapter 11.8.1 0: format0(default) 1: format1	RW
22:17	DMY_BITS	The needed dummy cycle num (unit: SFC_CLK cycle) 000000: no dummy transfer (default) ..... 000100: 4 dummy cycles ..... 000110: 6 dummy cycles ..... 001000: 8 dummy cycles ..... 001010: 10 dummy cycles ..... 010000: 16 dummy cycles ..... 011000: 24 dummy cycles ..... 100000: 32 dummy cycles	RW
16	DATE_EN	0: no data transfer(default) 1: has data transfer	RW
15:0	CMD	The transfer command	RW

11.7.2.12 SFC Transfer Length Register(SFC_TRAN_LEN,0x002C)

	SFC_TRAN_LEN																															Base + 0x002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRAN_LEN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	TRAN_LEN	Number of bytes to be transferred. 32'h0: no data transfer *Note: this register should be 0 when there isn't data phase in the flow, else the DMA or RMC will start.*	RW

11.7.2.13 SFC Device Address 0 Register(SFC_DEV_ADDR0, 0x0030)

	SFC_DEV_ADDR0																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR	The low bytes of flash address for transfer.	RW

11.7.2.14 SFC Device Address 1 Register(SFC_DEV_ADDR1, 0x0034)

	SFC_DEV_ADDR1																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR	The low bytes of flash address for transfer.	RW

11.7.2.15 SFC Device Address 2 Register(SFC_DEV_ADDR2, 0x0038)

	SFC_DEV_ADDR2																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	DEV_ADDR	The low bytes of flash address for transfer.	RW

11.7.2.16 SFC Device Address 3 Register(SFC_DEV_ADDR0-5, 0x003C)

	SFC_DEV_ADDR3																															Base + 0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR	The low bytes of flash address for transfer.	RW

11.7.2.17 SFC Device Address 4 Register(SFC_DEV_ADDR4, 0x0040)

	SFC_DEV_ADDR4																															Base + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR	The low bytes of flash address for transfer.	RW

11.7.2.18 SFC Device Address 5 Register(SFC_DEV_ADDR5, 0x0044)

	SFC_DEV_ADDR5																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	DEV_ADDR	The low bytes of flash address for transfer.	RW

11.7.2.19 SFC Device Address Plus 0 Register (SFC_DEV_ADDR_PLUS0, 0x0048)

	SFC_DEV_ADDR_PLUS0																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR_PLUS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR_PLUS	The high bytes of flash address for transfer.	RW

11.7.2.20 SFC Device Address Plus 1 Register (SFC_DEV_ADDR_PLUS1, 0x004C)

	SFC_DEV_ADDR_PLUS1																															Base + 0x004C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR_PLUS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR_PLUS	The high bytes of flash address for transfer.	RW

11.7.2.21 SFC Device Address Plus 2 Register (SFC_DEV_ADDR_PLUS2, 0x0050)

	SFC_DEV_ADDR_PLUS2																															Base + 0x0050
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR_PLUS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	DEV_ADDR_PLUS	The high bytes of flash address for transfer.	RW

11.7.2.22 SFC Device Address Plus 3 Register (SFC_DEV_ADDR_PLUS3, 0x0054)

	SFC_DEV_ADDR_PLUS3																															Base + 0x0054
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR_PLUS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR_PLUS	The high bytes of flash address for transfer.	RW

11.7.2.23 SFC Device Address Plus 4 Register (SFC_DEV_ADDR_PLUS4, 0x0058)

	SFC_DEV_ADDR_PLUS4																															Base + 0x0058
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR_PLUS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR_PLUS	The high bytes of flash address for transfer.	RW

11.7.2.24 SFC Device Address Plus 5 Register (SFC_DEV_ADDR_PLUS5, 0x005C)

	SFC_DEV_ADDR_PLUS5																															Base + 0x005C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR_PLUS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	DEV_ADDR_PLUS	The high bytes of flash address for transfer.	RW

11.7.2.25 SFC Memory Address Register(SFC_MEM_ADDR,0x0060)

	SFC_MEM_ADDR																															Base + 0x0060
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MEM_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	MEM_ADDR	Memory address for DMA. *Note: this register must be 0 when slave mode*	RW

11.7.2.26 SFC Trigger Register(SFC_TRIG,0x0064)

	SFC_TRIG																															Base + 0x0064
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													FLUSH	STOP	START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect. Read as zero.	R
2	FLUSH	Write 1 to reset the FIFO. Write 0 has no effect. *Note: FIFO will be flushed after start.*	W
1	STOP	Write 1 to stop all transmission. Write 0 has no effect.	W
0	START	Write 1 to start the transmission. Write 0 has no effect.	W

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11.7.2.27 SFC Status Register(SFC_SR,0x0068)

	SFC_SR																															Base + 0x0068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									FIFO_NUM							Reserved									BUSY		END	TRAN_REQ	RECE_REQ	OVER	UNDER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Write has no effect. Read as zero.	R
22:16	FIFO_NUM	The quantity of data in FIFO (unit: word)	R
15:7	Reserved	Write has no effect. Read as zero.	R
6:5	BUSY	00: the SFC is IDLE 01: the SFC is in transaction 10: the SFC is in reception 11: the SFC is waiting for transfer	R
4	END	Indicate whether the transfer is end 0: the transfer isn't end or SFC is IDLE 1: the transfer is end This bit will generate INT_END signal.	R
3	TRAN_REQ	0: no request 1: vacancy num in FIFO is more than or equal to the threshold. This bit will generate the INT_TREQ interrupt.	R
2	RECE_REQ	0: no request 1: data num in FIFO is more than or equal to the threshold. This bit will generate the INT_RREQ interrupt.	R
1	OVER	0: no over-run 1: FIFO is over-run. This bit will generate the INT_OVER interrupt.	R
0	UNDER	0: no error. 1: FIFO is under-run This bit will generate INT_UNDR signal.	R

11.7.2.28 SFC Status Clear Register(SFC_SCR,0x006C)

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	SFC_SCR																															Base + 0x006C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CLR_END	CLR_TREQ	CLR_RREQ	CLR_OVER	CLR_RUNDR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Write has no effect. Read as zero.	R
4	CLR_END	0: has no effect. 1: clear the SFC_SR.END flag and the INT_END.	W
3	CLR_TREQ	0: has no effect. 1: clear the SFC_SR.TREQ flag and the INT_TREQ	W
2	CLR_RREQ	0: has no effect. 1: clear the SFC_SR.RREQ flag and the INT_RREQ	W
1	CLR_OVER	0: has no effect. 1: clear the SFC_SR.OVER flag and the INT_OVER	W
0	CLR_UNDR	0: has no effect. 1: clear the SFC_SR.UNDER flag and the INT_UNDR	W

11.7.2.29 SFC Interrupt Controller Register(SFC_INTC,0x0070)

	SFC_INTC																															Base + 0x0070
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											MASK_END	MASK_TREQ	MASK_RREQ	MASK_OVER	MASK_UNDR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:5	Reserved	Write has no effect, read as zero.	R
4	MASK_END	0: the INT_END is not masked 1: the INT_END will be masked (default)	RW
3	MASK_TREQ	0: the INT_TREQ is not masked 1: the INT_TREQ will be masked (default)	RW
2	MASK_RREQ	0: the INT_RREQ is not masked 1: the INT_RREQ will be masked (default)	RW

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1	MASK_OVER	0: the INT_OVER is not masked 1: the INT_OVER will be masked (default)	RW
0	MASK_UNDR	0: the INT_UNDR is not masked 1: the INT_UNDR will be masked (default)	RW

Note: When the interrupt flag is cleared, the next interrupt will be generated immediately, so long as the requirement is contented.

11.7.2.30 SFC FSM Register(SFC_FSM,0x0074)

	SFC_FSM																															Base + 0x0074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												FSM_AHB				FSM_SPI					Reserved	FSM_CLK				FSM_DMAC			FSM_RMC		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	1

Bits	Name	Description	RW
31:20	Reserved	Write has no effect. Read as indeterminate value.	R
19:16	FSM_AHB	The AHB_master module's FSM state	R
15:11	FSM_SPI	The SPI_ctrl module's FSM state	R
10	Reserved	Write has no effect. Read as indeterminate value.	R
9:6	FSM_CLK	The clk_gen module's FSM state	R
5:3	FSM_DMAC	The DMAC module's FSM state	R
2:0	FSM_RMC	The RCM module's FSM state	R

11.7.2.31 SFC Clk_gate Enable register(SFC_CGE,0x0078)

	SFC_CGE																															Base + 0x0078
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CGE_SFC_EN	CGE_FIFO_EN	CGE_DMA_EN	CGE_RMC_EN	CGE_SPI_EN	CGE_REG_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Name	Description	RW
31:6	Reserved	Write has no effect.	R

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		Read as indeterminate value.	
5	CGE_SFC_EN	0: disable the flow_ctrl module's clk_gate function 1: enable the flow_ctrl module's clk_gate function (default)	RW
4	CGE_FIFO_EN	0: disable the fifo module's clk_gate function 1: enable the fifo module's clk_gate function (default)	RW
3	CGE_DMA_EN	0: disable the dmac and ahb_mst module's clk_gate function 1: enable the dmac and ahb_mst module's clk_gate function (default)	RW
2	CGE_RMC_EN	0: disable the rmc module's clk_gate function 1: enable the rmc module's clk_gate function (default)	RW
1	CGE_SPI_EN	0: disable the spi and clk_gen module's clk_gate function 1: enable the spi and clk_gen module's clk_gate function (default)	RW
0	CGE_REG_EN	0: disable the reg module's clk_gate function 1: enable the reg module's clk_gate function (default)	RW

11.7.2.32 SFC Data Register(SFC_DR,0x1000)

	SFC_DR																																Base + 0x1000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DR	Data register for FIFO.	RW

11.8 Software Guideline

11.8.1 Phase Description

- ✧ The phase is consisted of four sections: CMD, ADDR, DUMMY, DATA.
- ✧ Each phase could have one or more sections, four at the most.
- ✧ For one section, one phase could have one at the most.
- ✧ In all phases, only one phase can have DATA section.(we call this phase as data phase, other are command phase)
- ✧ Sections in a phase will be operated by two sequence format:

CMD	ADDR	DUMMY	DATA

Format0

CMD	DUMMY	ADDR	DATA

Format1

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✧ For one flow, only one kind of the direction of transmission is supported.

11.8.2 Multi phases flow

Figure 11-9 Multi phases flow

1 Configure the parameter related to the device hardware.
Such as the default level of IO port, timing parameter, etc.
related reg：SFC_DEV_CONF

2 Configure the parameter related to this transmission flow.
Such as num of phase, command format, operation mode, source address and target address, transfer direction and length, etc.
related reg：SFC_GLB、SFC_DEV_STA_EXP、SFC_DEV_STA_MSK、SFC_TRAN_CONF0-6、SFC_TRAN_LEN、SFC_DEV_ADDR0-6、SFC_MEM_ADDR

3 Open the trigger
related reg：SFC_TRIG

4 Waiting for end_end

5 Repeat step 2 for other flow

11.8.3 One phase flow

The flow can also be executed by only one phase. The NAND write perspective flow shown in the Figure 11-10 as follow:

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Figure 11-10 One phase flow

11.8.4 Meters of DMA operation need attention

DMA need some other parameter on the basic configuration.

– configure SFC_GLB (BURST_LEN、OP_MODE、BURST_LEN)

– configure SFC_MEM_ADDR (the memory address)

–

11.8.5 Meters of slave mode operation need attention

The SFC will generate request according to the THRESHOLD. Whether the CPU polling the SFC_SR register or waiting for an interrupt, the number of data, transferred by AHB bus each time, must match the THRESHOLD too.

11.8.6 Example (NAND flash write)

a) configure SFC_DEV_CONF and SFC_GLB register

b) program load (PL)

Configure the parameter of PL into phase0 registers:

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– configure the SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, DMY_NUM, etc)
– configure SFC_DEV_ADDR0
– configure SFC_TRAN_LEN

c) write enable (WE)

Configure the parameter of WE into phase1 registers:

– configure SFC_TRAN_CONF1(TRAN_MODE, CMD_EN, CMD, etc)

d) program execute

Configure the parameter of PE into phase2 registers:

– configure SFC_TRAN_CONF2(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, etc)
– configure SFC_DEV_ADDR2

e) get features command to read the status

Configure the parameter of PE into phase2 registers:

– configure SFC_TRAN_CONF(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, POLL_EN, etc)
– configure SFC_DEV_ADDR
– configure SFC_DEV_STA_EXP
– configure SFC_DEV_STA_MSK

f) open the trigger

g) waiting the END interrupt

h) clear the END bit zone

11.9 Index

Table 11-4 Terms and Abbreviations

Name	Description
AHB	Advanced Microcontroller Bus Architecture

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Dual SPI	See SPI
CPU	Central Processing Unit
DMA	Direct Memory Access
Endian	The convention used to interpret the bytes making up a data word when those bytes are stored in computer memory. See Endianness at Wikipedia
FIFO	First In, First Out, a method for organizing and manipulating a data buffer
LSB	See Endian
MSB	See Endian
Quad SPI	See SPI
SPI	Serial Peripheral Interface
Standard SPI	See SPI
tCHSH	Time from clock pull high to select pull low. See a NOR Flash device spec
tSHSL	Time from select pull high to select pull low. See a NOR Flash device spec
tSLCH	Time from select pull low to clock pull high. See a NOR Flash device spec

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Section 5

SYSTEM FUNCTIONS

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12 Clock Reset and Power Controller

12.1 Overview

The Clock & Power management block consists of three parts: Clock control, PLL control, and Power control, Reset control.

The Clock control logic can generate the required clock signals including CCLK for CPU, HHCLK for L2CACHE, H0CLK for the AHB0, H2CLK for the AHB2, PCLK for the APB bus peripherals , DDR_CLK for DDR.

The Chip has four Phase Locked Loops (PLL):
1.APLL mainly is used to CPU and L2CACHE, also may use the AHB0 and AHB2, or other peripherals
2.MPLL mainly is used to DDR, also uses AHB0 and AHB2 APB, or other peripherals.
3.VPLL and EPLL mainly is used to Helix,Radix,ISP,I2S,MAC,LCD Pixel Clock and External Sensor Clock(cim_clk),SSI/SFC,MSC0/1.

It is recommend DDR clock to use MPLL.

For the power control logic, there are various power management schemes to keep optimal power consumption for a given task. The power management block can activate four modes: NORMAL mode, IDLE mode, SLEEP mode.

For reset control logic, the hardware reset and hibernate reset is extended to more 80ms. It controls or distributes all of the system reset signals.

12.2 Feature

- On-chip 5MHz~200MHZ oscillator circuit, 24M oscillator circuit has recommended
- On-chip 32.768KHZ oscillator circuit, it's mainly to generate for RTC clock
- One three-chip phase-locked loops (PLL) with programmable multiplier
- CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, frequency can be changed separately for software by setting registers
- MSC clock supports 50M clock
- Functional-unit clock gating

12.3 Block Diagram

Following figure illustrates a block diagram of CGU.

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NOTES:

1. Clock mux in grey color represents glitch-free clock mux, which is free of glitches if clock selection is changed. Clock mux in white color represents non-glitch-free clock mux, which can suffer from glitches when changing clock sources. Care must be taken in using each of clock muxes.
2. VPLL and EPLL not used for all, it's just fixed to helix/radix/isp/aic/cim/gmac/lcd/ssi/sfc/msc clock needed

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12.4 Registers description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

12.4.1 Register Memory Map

Table 12-1 Registers Memory Map Base Address

Name	Base	Description
CPM	0x10000000	Address base of CPM

The Clock Reset and Power Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 12-2 CPM Registers Map

Name	RW	Reset Value	Address offset	Access Size
CPCCR	RW	0x5500_0000	0x0000	32
CPPCR	RW	0x0000_0020	0x000C	32
CPAPCR	RW	0x0630_5040	0x0010	32
CPMPCR	RW	0x0630_5040	0x0014	32
DDRCDR	RW	0x4000_0000	0x002C	32
HELIXCDR	RW	0x0000_0000	0x0030	32
CPSPR	RW	0x????_????	0x0034	32
CPSPPR	RW	0x0000_A5A5	0x0038	32
USBPCR	RW	0x4099_19B8	0x003C	32
USBRDT	RW	0x0000_0004	0x0040	32

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USBVBFIL	RW	0x00FF_0080	0x0044	32
USBPCR1	RW	0x8a80_0090	0x0048	32
MACCDR	RW	0x0000_0000	0x0054	32
CPEPCR	RW	0x0630_5040	0x0058	32
I2SCDR	RW	0x0000_0000	0x0060	32
LPCDR	RW	0x0000_0000	0x0064	32
MSC0CDR	RW	0x0000_0000	0x0068	32
I2SCDR1	RW	0x0000_0000	0x0070	32
SSICDR	RW	0x0000_0000	0x0074	32
CIMCDR	RW	0x0000_0000	0x007C	32
ISPCDR	RW	0x0000_0000	0x0080	32
EXCLK_DS	RW	0x0000_0002	0x008C	32
MSC1CDR	RW	0x0000_0000	0x00A4	32
CPM_INTR	RO	0x0000_0000	0x00B0	32
CPM_INTRE	RW	0x0000_0000	0x00B4	32
DRCG	RW	0x0000_0001	0x00D0	32
CPCSR	RO	0x0000_0000	0x00D4	32
CPVPCR	RW	0x0630_5040	0x00E0	32
MACPHYC	RW	0x0000_0000	0x00E8	32

12.4.2 Register and Fields Description

12.4.2.1 Clock Control Register(CPCCR,0x0000)

The Clock Control Register (CPCCR) is a 32-bit read/write register, which controls CCLK, H0CLK, H2CLK and PCLK division ratios. It is initialized to 0x55000000 by any reset. Only word access can be used on CPCCR.

	CPCCR																															BASE + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SEL_SRC		SEL_CPLL		SEL_H0PLL		SEL_H2PLL		GATE_SCLKA	CE_CPU	CE_AHB0	CE_AHB2	PDIV				H2DIV				H0DIV				L2CDIV				CDIV			
RST	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	SEL_SRC	00: stop MUX clock output 01: EXCLK 10: APLL The mux clock output is SCLK_A The clock mux is free of glitches if clock selection is changed	RW

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		When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	
29:28	SEL_CPLL	00: stop MUX clock output 01: SCLK_A 10: MPLL The mux clock output is to CPU and L2CAHE The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
27:26	SEL_H0PLL	00: stop MUX clock output 01: SCLK_A 10: MPLL The mux clock output is to AHB0 The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
25:24	SEL_H2PLL	00 : stop MUX clock output 01: SCLK_A 10: MPLL The mux clock output is to AHB2 and APB The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
23	GATE_SCLKA	0: SCLK_A not gating 1: SCLK_A is gating. Gating modules: VPU ISP MSC GMAC MAC AIC（i2s） SSI CIM_MCLK etc	RW
22	CE_CPU	Change enable for CPU and L2CAHE. If CE_CPU is 1 , write on CDIV, L2CDIV will start a frequency changing sequence immediately. If CE_CPU is 0, writes on CDIV and L2CDIV have no affect.	RW
21	CE_AHB0	Change enable for AHB0. If CE_AHB0 is 1 , write on H0DIV will start a frequency changing sequence immediately. If CE_AHB0 is 0, writes on H0DIV have no affect.	RW
20	CE_AHB2	Change enable for AHB2. If CE_AHB2 is 1 , write on H2DIV, PDIV will start a frequency changing sequence immediately. If CE_AHB2 is 0, writes on H2DIV, PDIV have no affect.	RW
19:16	PDIV	Divider for Peripheral Frequency. Specified the APB PCLK division ratio. <table><tr><th colspan="4">Bit 19~16: PDIV</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>X1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>X1/2</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>X1/3</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>X1/4</td></tr></table>	RW

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			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	**1**	**1**	**0**	**X1/X15**	
			1	**1**	**1**	**1**	**X1/16**	
15:12	H2DIV	Divider for AHB2 Frequency. Specified the AHB2 CLK division ratio.						RW
			Bit 15~12: H2DIV				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	1	1	0	X1/15	
			1	1	1	1	X1/16	
11:8	H0DIV	Divider for AHB0 Frequency. Specified the AHB0 CLK division ratio.						RW
			Bit 11~8: H0DIV				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	

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			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	**1**	**1**	**0**	**X1/15**	
			1	**1**	**1**	**1**	**X1/16**	
7:4	L2CDIV	Divider for L2CACHE Frequency. Specified the L2C CLK division ratio.						RW
			Bit 7~4: L2CDIV				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	**1**	**1**	**0**	**X1/15**	
			1	**1**	**1**	**1**	**X1/16**	
3:0	CDIV	Divider for CPU Frequency. Specified the CPU CLK division ratio.						RW
			Bit 3~0: CDIV				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	

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		1	1	1	0	X1/15	
		1	1	1	1	X1/16	

Import Note1 : for PDIV and AHB2DIV, AHB2's clock frequency must be 1 or 2 times of PDIV's clock frequency. For L2CDIV and CDIV, CPU's clock frequency must be 1,2,3, or 4 times of L2CACHE's clock frequency.

Import Note2 : After reset, H0DIV and CE_AHB0 will be zero, and ahb0's clock freq and apb0's clock freq will be 1:1, but if you have ever set CE_AHB0 and change the value of H0DIV, ahb0's clock freq and apb0's clock freq will be 2:1 from then on.

12.4.2.2 PLL Control Register(CPPCR,0x000C)

The PLL Control Register (CPPCR) is a 32-bit read/write register, which controls PLL some controls bits and stabilize time. It is initialized to 0x00000020 only by any reset. Only word access can be used on CPPCR. It is used to control all PLL.

	CPPCR																															BASE + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	APLL_BP	Reserved	MPLL_BP	Reserved	VPLL_BP	Reserved	EPLL_BP	Reserved																PLLST							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, Read as zero.	R
30	APLL_BP	APLL bypass Mode: 0 - not bypass 1- bypass mode	RW
29	Reserved	Writing has no effect, Read as zero.	R
28	MPLL_BP	MPLL bypass Mode: 0 - not bypass 1- bypass mode	RW
27	Reserved	Writing has no effect, Read as zero.	R
26	VPLL_BP	VPLL bypass Mode: 0 - not bypass 1- bypass mode	RW
25	Reserved	Writing has no effect, Read as zero.	R
24	EPLL_BP	EPLL bypass Mode: 0 - not bypass 1- bypass mode	RW
23:8	Reserved	Writing has no effect, Read as zero.	R

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7:0	PLLST	PLL Stabilize Time. Specifies the PLL stabilize time by unit of RTCCLK (approximate 32kHz) cycles. It is used when change PLL multiplier or change PLL from off to on. It is initialized to H'20. It is used to control all PLL.	RW

12.4.2.3 APLL Control Register(CPAPCR,0x0010)

The APLL Control Register (CPAPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x0630_5040 only by any reset. Only word access can be used on CPAPCR.

	CPAPCR																															BASE + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			APLLM									APLLN						APLLOD			Reserved			APLLRG			Reserved	APLL_ON	ALOCK	Reserved	APLLEN
RST	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, Read as zero.	R
28:20	APLLM	APLL feedback 8-bit multiplication factor NF = APLLM [8:0] +1	RW
19:14	APLLN	APLL input reference 6-bit divider. NR = APLLN[5:0] +1	RW
13:11	APLLOD	APLL output divider value 0~6 : valid value. NQ = 2^{APLLOD} 7 : invalid value .please don't use it.	RW
10:8	Reserved	Writing has no effect, Read as zero.	R
7：5	APLLRG	APLL Filter Range 000=BYPASS 001=5-10MHz 010=10-16MHz 011=16-26MHz 100=26-42MHz 101=42-68MHz 110=68-110MHz 111=110-200MHz	RW
4	Reserved	Writing has no effect, Read as zero.	
3	APLL_ON	PLL ON Flag. 0: PLL is off or not stable 1: PLL is on and stable	R

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2	ALOCK	When change stable , alock bit is set to 1 . Stable Flag bit .	R
1	Reserved	Writing has no effect, Read as zero.	R
0	APLLEN	APLL Enable. When APLLEN is set to 1, APLL starts to lock phase. After APLL stabilizes, APLL_ON bit is set.	RW

12.4.2.4 MPLL Control Register(CPMPCR,0x0014)

The MPLL Control Register (CPMPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x0630_5040 only by any reset. Only word access can be used on CPMPCR.

	CPMPCR																															BASE + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			MPLLM									MPLLN						MPLLOD			Reserved			MPLLRG			Reserved	MPLL_ON	MLOCK	Reserved	MPLLEN
RST	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, Read as zero.	R
28:20	MPLLM	MPLL feedback 12-bit multiplication factor NF = MPLLM[8:0] +1	RW
19:14	MPLLN	MPLL input reference 6-bit divider. NR = MPLLN[5:0] +1	RW
13:11	MPLLOD	MPLL output divider value 0~6 : valid value. NQ = 2^{MPLLOD} 7 : invalid value .please don't use it.	RW
10:8	Reserved	Writing has no effect, Read as zero.	RW
7:5	MPLLRG	MPLL Filter Range 000=BYPASS 001=5-10MHz 010=10-16MHz 011=16-26MHz 100=26-42MHz 101=42-68MHz 110=68-110MHz 111=110-200MHz	R
4	Reserved	Writing has no effect, Read as zero.	R
3	MPLL_ON	PLL ON Flag. 0: PLL is off or not stable	R

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		1: PLL is on and stable	
2	MLOCK	When change stable , mlock bit is set to 1 . Stable Flag bit .	R
1	Reserved	Writing has no effect, Read as zero.	R
0	MPLLEN	MPLL Enable. When MPLLEN is set to 1, MPLL starts to lock phase. After MPLL stabilizes, MPLL_ON bit is set.	RW

12.4.2.5 VPLL Control Register(CPVPCR,0x00E0)

The VPLL Control Register (CPVPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x0630_5040 only by any reset. Only word access can be used on CPVPCR.

	CPVPCR																															BASE + 0x00E0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			VPLLM									VPLLN						VPLLOD			Reserved			VPLLRG			Reserved	VPLL_ON	VLOCK	Reserved	VPLLEN
RST	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, Read as zero.	R
28:20	VPLLM	VPLL feedback 12-bit multiplication factor NF = VPLLM[8:0]	RW
19:14	VPLLN	VPLL input reference 6-bit divider. NR = VPLLN[5:0]	RW
13:11	VPLLOD	VPLL output divider value 0~6 : valid value. NQ = 2^{VPLLOD} 7 : invalid value .please don't use it.	RW
10:8	Reserved	Writing has no effect, Read as zero.	R
7:5	VPLLRG	VPLL Filter Range 000=BYPASS 001=5-10MHz 010=10-16MHz 011=16-26MHz 100=26-42MHz 101=42-68MHz 110=68-110MHz 111=110-200MHz	R
4	Reserved	Writing has no effect, read as zero.	R
3	VPLL_ON	PLL ON Flag.	R

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		0: PLL is off or not stable. 1: PLL is on and stable.	
2	VLOCK	When change stable , vlock bit is set to 1 . Stable Flag bit .	R
1	Reserved	Writing has no effect, Read as zero.	R
0	VPLLEN	VPLL Enable. When VPLLEN is set to 1, VPLL starts to lock phase. After VPLL stabilizes, VPLL_ON bit is set.	RW

12.4.2.6 EPLL Control Register(CPEPCR,0x0058)

The EPLL Control Register (CPEPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x0630_5040 only by any reset. Only word access can be used on CPEPCR.

	CPEPCR																															BASE + 0x0058
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			EPLLM									EPLLN						EPLLOD			Reserved			EPLLRG			Reserved	EPLL_ON	ELOCK	Reserved	EPLLEN
RST	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, Read as zero.	RW
28:20	EPLLM	EPLL feedback 12-bit multiplication factor NF = EPLLM[8:0]	RW
19:14	EPLLN	EPLL input reference 6-bit divider. NR = EPLLN[5:0]	RW
13:11	EPLLOD	EPLL output divider value 0~6 : valid value. NQ = 2^{EPLLOD} 7 : invalid value .please don't use it.	RW
10:8	Reserved	Writing has no effect, Read as zero.	R
7:5	EPLLRG	EPLL Filter Range 000=BYPASS 001=5-10MHz 010=10-16MHz 011=16-26MHz 100=26-42MHz 101=42-68MHz 110=68-110MHz 111=110-200MHz	R
4	Reserved	Writing has no effect, Read as zero.	R

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3	EPLL_ON	PLL ON Flag. 0: PLL is off or not stable 1: PLL is on and stable	R
2	ELOCK	When change stable , elock bit is set to 1. Stable Flag bit .	R
1	Reserved	Writing has no effect, Read as zero.	R
0	EPLLEN	EPLL Enable. When EPLLEN is set to 1, EPLL starts to lock phase. After EPLL stabilizes, EPLL_ON bit is set.	RW

12.4.2.7 DDR Memory clock divider Register(DDRCDR,0x002C)

DDR memory clock divider Register (DDRCDR) is a 32-bit read/write register that specifies the divider of DDR memory clock . This register is initialized to 0x40000000 only by any reset. Only word access can be used on DDRCDR.

	DDRCDR																															BASE + 0x002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCS		CE_DDR	DDR_BUSY	DDR_STOP	GATE_EN	CHANGE_EN	FLAG	Reserved																				DDRCDR			
RST	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	DCS	DDR Clock Source Selection. Selects the DDR clock source between APLL output and MPLL output. 00: stop MUX clock output 01: DDR clock source is SCLK_A 10: DDR clock source is MPLL The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
29	CE_DDR	Change enable for DDR. If CE_DDR is 1 , write on DDRCDR will start a frequency changing sequence immediately. If CE_DDR is 0, writes on DDRCDR have no affect	RW
28	DDR_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until DDR_BUSY == 0, then may begin another frequency change.	R

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27	DDR_STOP	When DDR_STOP is 1 and CE_DDR is 1, the DDR clock will stop. When DDR_STOP is 0 and CE_DDR is 1, the DDR clock will continue. Software should wait until DDR_BUSY == 0, then may begin another frequency change. DDR_STOP is prior to DDRCDR.	RW
26	GATE_EN	1'b1: if DDR gives a clock stop request to CPM, and CPM will gate DDR's clock.	RW
25	CHANGE_EN	When this bit set high, CPM will change DDR's clock when CE_DDR is high and FLAG is low.	RW
24	FLAG	Will be set high when DDR gives relative flag Can only be write zero by software	RW
23:4	Reserved	Writing has no effect, Read as zero.	R
3:0	DDRCDR	Divider for DDR Frequency. Specified the DDR memory clock division ratio, which varies from 1 to 16 (division ratio = DDRCDR + 1).	RW

12.4.2.8 HELIX/RADIX clock divider Register(HELIXCDR,0x0030)

HELIX/RADIX clock divider Register (HELIXCDR) is a 32-bit read/write register that specifies the divider of HELIX/RADIX clock. This register is initialized to 0x00000000 only by any reset. Only word access can be used on HELIXCDR.

	HELIXCDR																															BASE + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HELIXCS		CE_HELIX	HELIX_BUSY	HELIX_STOP	Reserved																							HELIXCDR			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	HELIXCS	HELIX/RADIX Clock Source Selection : 00: HELIX/RADIX clock source is SCLK_A 01: HELIX/RADIX clock source is MPLL 10: HELIX/RADIX clock source is VPLL 11: HELIX/RADIX clock source is EPLL It is no glitch free mux. Software should be stop HELIX/RADIX clock, when change this bit.	**RW**
29	CE_HELIX	Change enable for HELIX. If CE_HELIX is 1 , write on HELIXCDR will start a frequency changing sequence immediately. If CE_HELIX is 0, writes on HELIXCDR have no affect	RW
28	HELIX_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has	RW

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		finished., otherwise it indicates the frequency change is on going Software should be wait until HELIX_BUSY == 0, may begin another frequency change.	
27	HELIX_STOP	When HELIX_STOP is 1 and CE_HELIX is 1, the HELIX clock will stop. When HELIX_STOP is 0 and CE_HELIX is 1, the HELIX clock will continue. Software should wait until HELIX_BUSY == 0, may begin another frequency change. HELIX_STOP is prior to HELIXCDR. If system don't use this module, may set this bit to reduce power.	RW
26:4	Reserved	Writing has no effect, Read as zero.	R
3:0	HELIXCDR	Divider for HELIX Frequency. Specified the HELIX clock division ratio, which varies from 1 to 16 (division ratio = HELIXCDR + 1).	RW

12.4.2.9 CPM Scratch Pad Register(CPSPR,0x0034)

The Scratch Pad Register is a 32-bit read/write register that allows software to preserve some critical data . It is not initialized by power on and WDT reset.

	CPSPR																															BASE + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CPPSR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

12.4.2.10 CPM Scratch Pad Protected Register(CPSPPR,0x0038)

The Scratch Pad Protected Register is reset to 0x0000a5a5. When CPSPPR value equals to 0x00005a5a, software can write the CPSPR. or else can't.

	CPSPPR																															BASE + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPSPPR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1

Bits	Name	Description	RW

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31:16	Reserved	Writing has no effect, Read as zero.	R
15:0	CPSPPR	The value is only = 0x00005a5a, software can write the CPSPR.	RW

12.4.2.11 USB Parameter Control Register(USBPCR,0x003C)

The USBPCR is a 32-bit read/write register that allows software to control USB PHY some functions. It is initialized to 0x409919b8.

	USBPCR																															BASE + 0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	USB_MODE	AVLD_REG	IDPULLUP_MASK		Reserved					POR	Reserved																					
RST	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	0	1	1	1	0	0	0

Bits	Name	Description	RW
31	USB_MODE	0: work as USB device 1: work as OTG	RW
30	AVLD_REG	This bit is used to set “avalid”(VBUS above A-device session threshold) signal.	RW
29:28	IDPULLUP_MASK	These 2 bits control “idpullup” signal in otg mode. 2’b1x: “idpullup” always active 2’b01: “idpullup” always active when usb suspend 2’b00: use “idpullup” from otg controller	RW
27:23	Reserved	Writing has no effect, Read as zero.	R
22	POR	This signal resets all test registers and state machines in the USB PHY The POR signal must be asserted for a minimum of 10 µs. 1: reset 0: not reset *Please make sure USB PHY input signals value are correct before assert POR. *The PHYCLOCK will available after POR deasserted 45us..	RW
21:0	Reserved	Writing has no effect, read as zero.	R

12.4.2.12 USB Reset Detect Timer Register(USBRDT,0x0040)

The USBRDT is a 32-bit read/write register, It is initialized to 0x00000004

	USBRDT																															BASE + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				UTMI_RST	Reserved																								VBFIL_EN	IDDIG_EN	IDDIG_REG

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RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, Read as zero.	R
27	UTMI_RST	Utmi_rst: software to reset the usb_phy 0: valid. 1: unvalid.	RW
26:3	Reserved	Writing has no effect, Read as zero.	R
2	VBFIL_EN	1: This bit is enable the VBUS jitter filter time. 0: This bit is enable the iddig pin of control is equal to utmi_iddig of phy at OTG mode.	RW
1	IDDIG_EN	1: This bit is enable the iddig pin of control is equal to IDDIG_REG 0: This bit is enable the iddig pin of control is equal to utmi_iddig of phy at OTG mode.	RW
0	IDDIG_REG	This bit is enable at IDDIG_EN =1. 1: mini-B 0: mini-A	RW

12.4.2.13 USB VBUS Jitter Filter Register(USBVBFIL,0x0044)

The USBVBFIL is a 32-bit read/write register, It is initialized to 0x00FF0080

	USBVBFIL																															BASE + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDDIGFIL																USBVBFIL															
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	IDDIGFIL	These bits controls iddig jitter filter time.	RW
15:0	USBVBFIL	These bits controls VBUS jitter filter time.	RW

12.4.2.14 USB Parameter Control Register1(USBPCR1,0x0048)

The USBPCR1 is a 32-bit read/write register that allows software to control USB PHY some functions. It is initialized to 0x8a800090.

	USBPCR1																															BASE + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	BVLD_REG	IDPULLUP_ZEAR	DPPD	DMPD	Reserved																		Chrgvbus_enable	Dischrgvbus_enable	Reserved							
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	BVLD_REG	This bit is used to set “bvalid”(VBUS above B-device session threshold) signal.	RW
30	IDPULLUP_ZEAR	This bit is used to clear the idpullup to phy. 0: idpullup is 0. 1: idpullup is based on IDPULLUP_MASK and suspendm and usb_mode.	RW
29	DPPD	1: The pull-down resistance on D+ of port is enabled. 0: The pull-down resistance on D+ of port is disabled. Note: This bit is working for uhc.	RW
28	DMPD	1: The pull-down resistance on D- of port is enabled 0: The pull-down resistance on D- of port is disabled. Note: This bit is working for uhc.	RW
27:10	Reserved	Writing has no effect, read as zero.	R
9	Chrgvbus_enable	1: This bit enable chrgvbus of phy equal to chrg_vbus of control at otg_mode. 0: This bit enable chrgvbus of phy equal to 0.	RW
8	Dischrgvbus_enable	1: This bit enable dischrgvbus of phy equal to dischrg_vbus of control at otg_mode. 0: This bit enable dischrgvbus of phy equal to 0.	RW
7:0	Reserved	Writing has no effect, read as zero.	R

12.4.2.15 MACPHY clock divider Register (MACCDR,0x0054)

MAC clock divider Register (MACCDR) is a 32-bit read/write register that specifies the divider of MAC PHY clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on MACCDR.

	MACCDR																															BASE + 0x0054
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MACPCS		CE_MAC	MAC_BUSY	MAC_STOP	Reserved																			MACCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

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31:30	MACPCS	MAC PHY Clock Source Selection. Selects the MAC PHY clock source 00: MAC PHY clock source is SCLK_A 01: MAC PHY clock source is MPLL 10: MAC PHY clock source is VPLL 11: MAC PHY clock source is EPLL It is no glitch free mux.	RW
29	CE_MAC	Change enable for MAC. If CE_MAC is 1 , write on MACCDR ill start a frequency changing sequence immediately. If CE_MAC is 0, writes on MACCDR have no affect	RW
28	MAC_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should wait until MAC_BUSY == 0, may begin another frequency change.	RW
27	MAC_STOP	When MAC_STOP is 1 and CE_MAC is 1, the MAC clock will stop. When MAC_STOP is 0 and CE_MAC is 1, the MAC clock will continue. Software should wait until MAC_BUSY == 0, may begin another frequency change.	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	MACCDR	Divider for MAC PHY Frequency. Specified the MAC device clock division ratio division ratio = MACCDR + 1	RW

12.4.2.16 LCD pixel clock divider Register(LPCDR,0x0064)

LCD pix clock divider Register (LPCDR) is a 32-bit read/write register that specifies the divider of LCD pixel clock (LPCLK). This register is initialized to 0x00000000 by any reset. Only word access can be used on LPCDR.

	LPCDR																															BASE + 0x0064
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LPCS		LTCS	CE_LCD	LCD_BUSY	LCD_STOP	Reserved																		LPCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	LPCS	00: SCLK_A output 01: MPLL output 10: VPLL output 11: EPLL output It is no glitch free mux. Software should be stop pixel clock, when	RW

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		change this bit.	
29	PCLK_SEL	To select the pixclk or ~pixclk 0 : pixclk 1 : ~pixclk	RW
28	CE_LCD	Change enable for LCD. If CE_LCD is 1 , write on LPCDR will start a frequency changing sequence immediately. If CE_LCD is 0, writes on LPCDR have no affect.	RW
27	LCD_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until LCD_BUSY == 0, may begin another frequency change.	R
26	LCD_STOP	When LCD_STOP is 1 and CE_LCD is 1, the LCD clock will stop. When LCD_STOP is 0 and CE_LCD is 1, the LCD clock will continue. Software should wait until LCD_BUSY == 0, may begin another frequency change. LCD_STOP is prior to LPCDR. If system don't use this module, may set this bit to reduce power.	RW
25:8	Reserved	Writing has no effect, read as zero.	R
7:0	LPCDR	Divider for Pixel Frequency. Specified the LCD pixel clock (LPCLK) division ratio, which varies from 1 to 256 (division ratio = LPCDR + 1).	RW

12.4.2.17 MSC0 device clock divider Register(MSC0CDR,0x0068)

MSC0 device clock divider Register (MSC0CDR) is a 32-bit read/write register that specifies the divider of MSC0 device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on MSC0CDR.

	MSC0CDR																															**BASE + 0x0068**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPCS		CE_MSC0	MSC0_BUSY	MSC0_STOP	Reserved											S_CLK0_SEL	Reserved							MSC0CDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

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31:30	MPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: select VPLL clock output 11: select EPLL clock output The clock mux is not free of glitches if clock selection is changed The clock mux output is to MSC0, MSC1. It is source clock of MSC0, MSC1.	RW
29	CE_MSC0	Change enable for MSC0. If CE_MSC0 is 1 , write on MSC0CDR ill start a frequency changing sequence immediately. If CE_MSC0 is 0, writes on MSC0CDR have no affect	RW
28	MSC0_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until MSC0_BUSY == 0, may begin another frequency change.	R
27	MSC0_STOP	When MSC0_STOP is 1 and CE_MSC0 is 1, the MSC0 clock will stop. When MSC0_STOP is 0 and CE_MSC0 is 1, the MSC0 clock will continue. Software should wait until MSC0_BUSY == 0, may begin another frequency change.MSC0_STOP is prior to MSC0CDR. If system don't use this module, may set this bit to reduce power .	RW
26:16	Reserved	Writing has no effect, read as zero.	R
15	S_CLK0_SEL	MSC sample clock selection: 0: Sample clock is 90-degree phase shifted by device clock 1: Sample clock is 180-degree phase shifted by device clock	RW
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	MSC0CDR	Divider for MSC0 Frequency. Specified the MSC0 device clock division ratio division ratio = (MSC0CDR + 1)*2.	RW

12.4.2.18 MSC1 device clock divider Register(MSC1CDR,0x00A4)

MSC1 device clock divider Register (MSC1CDR) is a 32-bit read/write register that specifies the divider of MSC1 device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on MSC1CDR.

	MSC1CDR																															BASE + 0x00A4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		CE_MSC1	MSC1_BUSY	MSC1_STOP	Reserved											S_CLK1_SEL	Reserved							MSC1CDR							

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RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29	CE_MSC1	Change enable for MSC1. If CE_MSC1 is 1 , write on MSC1CDR ill start a frequency changing sequence immediately. If CE_MSC1 is 0, writes on MSC1CDR have no affect	RW
28	MSC1_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until MSC1_BUSY == 0, may go next	R
27	MSC1_STOP	When MSC1_STOP is 1 and CE_MSC1 is 1, the MSC1 clock will stop. When MSC1_STOP is 0 and CE_MSC1 is 1, the MSC1 clock will continue. Software should wait until MSC1_BUSY == 0, may begin another frequency change.MSC1_STOP is prior to MSC1CDR. If system don't use this module, may set this bit to reduce power .	RW
26:16	Reserved	Writing has no effect, read as zero.	R
15	S_CLK1_SEL	MSC1 sample clock selection: 0: Sample clock is 90-degree phase shifted by device clock 1: Sample clock is 180-degree phase shifted by device clock	RW
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	MSC1CDR	Divider for MSC1 Frequency. Specified the MSC1 device clock division ratio division ratio = (MSC1CDR + 1)*2.	RW

12.4.2.19 I2S device clock divider Register (I2SCDR,0x0060)

I2S device clock divider Register (I2SCDR) is a 32-bit read/write register that specifies the divider of I2S device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on I2SCDR.

	I2SCDR																															BASE + 0x0060
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	I2PCS		CE_I2S	I2SDIV_M									I2SDIV_N																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

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31:30	I2PCS	00: SCLK_A output 01: MPLL output 10: VPLL output 11: EPLL output	RW
29	CE_I2S	AIC M/N divider(1) enable.	RW
28:20	I2SDIV_M	Number M of AIC M/N divider(1).	RW
19:0	I2SDIV_N	Number N of AIC M/N divider(1).	RW

Note (1): AIC M/N divider is a decimal divider. The output clock frequency of AIC M/N divider is:

Fout = Fin * M / N.

AIC M/N divider output clock duty cycle is possible not 50%. But adjusting the M and N value, which makes the duty cycle is close to 50%. Error of duty cycle is:

De_p = (ceill(N / M) - (N / M)) / (N / M). ceil: Round toward positive infinity.

and:

De_n = (floor(N / M) - (N / M)) / (N / M). floor: Round toward negative infinity.

Recommend the De_p is less than 5% and De_n is great than -5%.

12.4.2.20 I2S device clock divider Register 1(I2SCDR1,0x0070)

I2S device clock divider Register 1(I2SCDR1) is a 32-bit read/write register that specifies the divider of I2S device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on I2SCDR1.

	I2SCDR1																															BASE + 0x0070
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	I2S_NEN	I2S_DEN	Reserved														I2SDIV_D															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	I2S_NEN	0: The number D of AIC M/N divider is automatic calculate. 1: The number D of AIC M/N divider is set by I2SDIV_D.	RW
30	I2S_DEN	0: I2SDIV_D = I2SDIV_N/2 1: I2SDIV_D = I2SDIV_D	RW
29:20	Reserved	Writing has no effect, read as zero.	R
19:0	I2SDIV_D	The number D of AIC M/N divider(2).	RW

Note (2): General D = N/2.

12.4.2.21 SSI device clock divider Register(SSICDR,0x0074)

SSI device clock divider Register (SSICDR) is a 32-bit read/write register that specifies the divider of

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SSI device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on SSICDR.

	SSICDR																															BASE + 0x0074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSIPCS		SSISCS	CE_SSI	SSI_BUSY	SSI_STOP	Reserved																		SSICDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	SSIPCS	00: select SCLK_A output 01: select MPLL output 10: select VPLL output 11: select EPLL output When SSISCS is equal to 1'b1, the bit is valid and It is direct to SFC module It is no glitch free mux. Software should be stop the module clock, when change this bit.	RW

29	SSISCS	0: EXCLK
		1: PLL_OUT/2
		It is direct ot SSI0/SSI1 module;
		when the SPCS bit is 2'b00, PLL_OUT = SCLK_A/(SSICDR+1);
		when the SPCS bit is 2'b01, PLL_OUT = MPLL/(SSICDR+1);
		when the SPCS bit is 2'b10, PLL_OUT = VPLL/(SSICDR+1);
		when the SPCS bit is 2'b11, PLL_OUT = EPLL/(SSICDR+1);
			RW

28	CE_SSI	Change enable for SSI. 0: writes on SSICDR have no affect. 1: write on SSICDR will start a frequency changing sequence immediately.	RW
27	SSI_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until SSI_BUSY == 0, may begin another frequency change.	R

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26	SSI_STOP	0: When SSI_STOP is 0 and CE_SSI is 1, the SSI clock will continue. 1: When SSI_STOP is 1 and CE_SSI is 1, the SSI clock will stop. Software should wait until SSI_BUSY == 0, may begin another frequency change. SSI_STOP is prior to SSICDR. If system don't use this module, may set this bit to reduce power .	RW
25:8	Reserved	Writing has no effect Read as zero.	R
7:0	SSICDR	Divider for SSI Frequency. Specified the SSI device clock division ratio, which varies from 1 to 256 (division ratio = SSICDR + 1).	RW

12.4.2.22 CIM MCLK clock divider Register(CIMCDR,0x007C)

CIM mclk clock divider Register (CIMCDR) is a 32-bit read/write register that specifies the divider of CIM mclk clock (CIM_MCLK). This register is initialized to 0x00000000 only by any reset. Only word access can be used on CIMCDR.

	CIMCDR																															BASE + 0x007C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CIMPCS		CE_CIM	CIM_BUSY	CIM_STOP	Reserved																			CIMCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	CIMPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: select VPLL clock output 11: select EPLL clock output It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_CIM	Change enable for CIM. If CE_CIM is 1 , write on CIMCDR ill start a frequency changing sequence immediately. If CE_CIM is 0, writes on CIMCDR have no affect	RW

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28	CIM_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until CIM_BUSY == 0, may begin another frequency change.	RW
27	CIM_STOP	When CIM_STOP is 1 and CE_CIM is 1, the CIM clock will stop. When CIM_STOP is 0 and CE_CIM is 1, the CIM clock will continue. Software should wait until CIM_BUSY == 0, may begin another frequency change. CIM_STOP is prior to CIMCDR. If system don't use this module, may set this bit to reduce power .	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	CIMCDR	Divider for CIM MCLK Frequency. Specified the CIM MCLK clock (CIM_MCLK) division ratio, which varies from 1 to 256 (division ratio = CIMCDR + 1). the output clock is "io_setup.cim_mclk_o".	RW

12.4.2.23 ISP clock divider Register(ISPCDR,0x0080)

ISP clock divider Register (ISPCDR) is a 32-bit read/write register that specifies the divider of ISP clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on ISPCDR.

	ISPCDR																															BASE + 0x0080
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ISPCS		CE_ISP	ISP_BUSY	ISP_STOP	Reserved																							ISPCDR			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	ISPCS	00: select SCLK_A output 01: select MPLL output 10: select VPLL output 11: select EPLL output It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_ISP	Change enable for ISP. If CE_ISP is 1 , write on ISPCDR ill start a frequency changing sequence immediately. If CE_ISP is 0, writes on ISPCDR have no affect	RW

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28	ISP_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until ISP_BUSY == 0, may begin another frequency change.	RW
27	ISP_STOP	When ISP_STOP is 1 and CE_ISP is 1, the ISP clock will stop. When ISP_STOP is 0 and CE_ISP is 1, the ISP clock will continue. Software should wait until ISP_BUSY == 0, may begin another frequency change. ISP_STOP is prior to ISPCDR. If system don't use this module, may set this bit to reduce power .	RW
26:4	Reserved	Writing has no effect, read as zero.	R
3:0	ISPCDR	Divider for ISP Frequency. Specified the ISP clock division ratio, which varies from 1 to 16 (division ratio = ISPCDR + 1).	RW

12.4.2.24 EXCLK Drive Strength Register(EXCLK_DS,0x008C)

The EXCLK_DS is a 32-bit read/write register that allows software to control the EXCLK drive strength.

	EXCLK_DS																														BASE + 0x008C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESERVED																														exclk_ds	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Description	RW
30:2	Reserved	Writing has no effect, read as zero.	R
1:0	exclk_ds	Control EXCLK clock drive strength.	RW

12.4.2.25 CPM interrupt Register(CPM_INTR,0x00B0)

The CPM Interrupt Register is a 32-bit read/write register that Description CPM interrupt status.

	CPM_INTR																														BASE + 0x00B0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														VBUS_INTR	ADEV_INTR

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RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	VBUS_INTR	B device insert interrupt.	R
0	ADEV_INTR	A device insert interrupt.	R

12.4.2.26 CPM interrupt enable Register(CPM_INTRE,0x00B4)

The CPM Interrupt Enable Register is a 32-bit read/write register that Enable CPM interrupt.

	CPM_INTRE																															BASE + 0x00B4	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														VBUS_INTRE	ADEV_INTRE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	VBUS_INTRE	B device insert interrupt enable.	RW
0	ADEV_INTRE	A device insert interrupt enable.	RW

12.4.2.27 DDR Clock Gate Register(DRCG,0x00D0)

	DRCG																															BASE + 0x00D0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							DRCG								
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Note: Please refer to DDR and NFI's spec for detail use of this register.

12.4.2.28 Clock Status Register(CPCSR,0x00D4)

Clock status register (CPCSR) is a 32-bit read/write register that specifies the status of CPCCR .This register is initialized to 0x00000000 only by any reset. Only word access can be used on CPCSR.

	CPCSR																															BASE + 0x00D4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	SRC_MUX	CPU_MUX	AHB0_MUX	AHB2_MUX	DDR_MUX	Reserved																									H2DIV_BUSY	H0DIV_BUSY	CDIV_BUSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SRC_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
30	CPU_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
29	AHB0_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
28	AHB2_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
27	DDR_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
26:3	Reserved	Writing has no effect, read as zero.	R
2	H2DIV_BUSY	The bit is a read-only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until H2DIV_BUSY == 0, then may begin another frequency change.	R
1	H0DIV_BUSY	The bit is a read-only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until H0DIV_BUSY == 0, then may begin another frequency change.	R
0	CDIV_BUSY	The bit is a read-only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until CDIV_BUSY == 0, then may begin another frequency change.	R

12.4.2.29 MAC PHY Control Register (MACPHYC,0x00E8)

The MAC PHY Control Register is a 32-bit read/write register that control GMAC interface. It is

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initialized to 0x0000000 0by reset.

	MACPHYC																															BASE + 0x00E8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Mode_sel	MAC_SPEED		Reserved																									SOFT_RST	PHY_INTF		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Mode_sel	0: RMII 1: reserved	RW
30:29	MAC_SPEED	It is only read. 10: 10M 11: 100M	R
28:4	Reserved	Writing has no effect, read as zero.	R
3	SOFT_RST	1:reset GMAC 0:don't reset GMAC	RW
2:0	PHY_INTF	100: RMII 0xx/1x1/110 : reserved	RW

12.5 PLL Operation

The PLL developed as a macro cell for clock generator. It can generate a stable high-speed clock from a slower clock signal. The phase-locked loop (PLL) block is provided as a drop-in functional block that fits in typical standard IO rings (foundry IO ring or 3rd party IP vendor IO ring). The PLL accepts a wide range of input frequencies and can produce a wide range of output frequencies, as detailed in Table 12-3. Several control bits are provided to configure the desired operating mode of the PLL, and these are detailed in Table 12-3. The logical features and data flow of the PLL are illustrated in the block diagram of Figure 12-1.

The PLL block diagram is shown in following figure:

Figure 12-1 Block Diagram of PLL

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Table 12-3 PLL Operational Range

<table>
<tr><th>Pin</th><th>Limitations</th><th>Note</th></tr>
<tr><td>DIVR[5:0]: Reference Divider value</td><td>Input Reference Frequency F_{REF} and post-divide REF F_{PFD} :
5MHz <= F_{REF} <= 200MHz
5MHz <= F_{PFD} <= 200MHz</td><td>DIVR+1 is used by means of F_{REF}/(DIVR+1)</td></tr>
<tr><td>DIVF[8:0] Feedback Divider value</td><td>F_{VCO} 's wide range is
1500MHz <= F_{VCO} <=3000MHz</td><td>(DIVF+1) is used by means of F_{VCO} = 2*F_{REF} (DIVF+1)/(DIVR+1)</td></tr>
<tr><td>DIVQ[2:0] Output divider value(2^{DIVQ})</td><td>DIVQ=0/1/2/3/4/5/6;
2^{DIVQ} =1/2/4/8/16/32/64
Note: DIVQ = 7 is invalid. please don't use it.</td><td>2^{DIVQ} is used by means of FVCO / 2^{DIVQ}</td></tr>
<tr><td>RANGE[2:0] PLL Filter Range</td><td>Settings Range[2:0] and F_{PFD} must maintain the PLL operational ranges specified in the following Table.
<table>
<tr><th>Range[2:0]</th><th>F_{PFD}=F_{REF}/(1+DIVR)</th></tr>
<tr><td>000</td><td>BYPASS</td></tr>
<tr><td>001</td><td>5~10MHz</td></tr>
<tr><td>010</td><td>10~16MHz</td></tr>
<tr><td>011</td><td>16~26MHz</td></tr>
<tr><td>100</td><td>26~42MHz</td></tr>
<tr><td>101</td><td>42~68MHz</td></tr>
<tr><td>110</td><td>68~110MHz</td></tr>
<tr><td>111</td><td>110~200MHz</td></tr>
</table></td><td></td></tr>
</table>

12.5.1 PLL Configuration

PLL Divider Value Setting

There are 3 divider values (N, M and 2^{OD}) to set the PLL output clock frequency PLLOUT:

The PLL output frequency, PLLOUT, is determined by the ratio set between the value set in the input divider and the feedback divider. PLL output frequency PLLOUT is calculated from the following equations:

FBDIV = PLLM+1

REFDIV = PLLN+1

FDIVQ= 2^{PLLOD}

RANGE=PLLRG

FVCO = 2*(FREF * FBDIV / REFDIV)

PLLOUT = FVCO / FDIVQ

= FREF *（PLLM + 1）* 2 /（(PLLN +1)*2^{PLLOD}）

FREF range between 5MHz -200MHz, Both FREF and post-divide FREF must be

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within this range

RANGE must be in accord with post-divide FREF;
FVCO should between 1500MHz – 3000MHz;
PLLOUT range between 25MHz - 3000MHz.

12.5.2 Main Clock Division Change Sequence

Main clock (CCLK, L2CLK, H2CLK, PCLK) frequencies can be changed separately or simultaneously by changing division ratio. Following conditions must be obeyed:

1 the frequency of CCLK must be 1,2,3 or 4 times of the frequency of L2CLK
2 the frequency of H2CLK must be 1 or 2 times of the frequency of PCLK

Don't violate this limitation, otherwise unpredictable error may occur.
Important Note: When cpu enters sleep mode, the apllen must be set to 1.

12.6 Power Manager

In the Low-Power mode, part or whole processor is halted. This will reduce power consumption. The Power Management Controller contains low-power mode control and reset sequence control.

12.6.1 Low-Power Modes and Function

The processor supports six low-power modes and function:

- NORMAL mode

  In Normal mode, all peripherals and the basic blocks including power management block, the CPU core, the bus controller, the memory controller, the interrupt controller, DMA, and the external master may operate completely. But, the clock to each peripheral, except the basic blocks, can be stopped selectively by software to reduce the power consumption.

- DOZE mode

  DOZE mode is entered by setting DOZE bit of LCR to 1. In DOZE mode, clock is burst to CPU core and the clock duty is set by DUTY field of LCR. DOZE mode is canceled by reset, interrupt or clearing DOZE bit to 0. Continuous clock is supplied immediately after DOZE mode is canceled. The other Clocks except CCLK run continuously in DOZE mode.

- IDLE mode

  In IDLE mode, the clock to the CPU core is stopped except the bus controller, the memory controller, the interrupt controller, and the power management block. To exit the IDLE mode, the any interrupts should be activated.

- SLEEP mode

  In SLEEP mode, all clocks except RTC clock are disabled. PLL is disabled also. SLEEP mode is canceled by reset or interrupt. When SLEEP mode is canceled, PLL is restarted , the PLL needs clock stabilization time (PLL lock time). This PLL stabilization time is automatically

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inserted by the internal logic with lock time count register. and all clocks start operating after PLL stability time.

- CLOCK GATE function

  CLOCK GATE function is used to gate specified on-chip module when it is not used. Set specified CLKG0~40 bits in CLKGR will enter specified CLK gate function. CLOCK gate function is canceled by reset or clearing specified CLKGR0~40 to 0.

- Power down Mode

  In order to reduce power leakage, software may shut down power supply for AHB1 and GPS module. When system enters into SLEEP mode, the software may shut down power for J1 according to OPCR.PD bit.

12.6.2 Register Description

All PMC register 32bit access address is physical address.

Table 12-4 Power/Reset Management Controller Registers Map

Name	RW	Reset Value	Address offset	Access Size
LCR	RW	0x0000_0000	0x0004	32
CLKGR0	RW	0x1FFF_FF80	0x0020	32
OPCR	RW	0x0000_1500	0x0024	32
CLKGR1	RW	0x0000_33FF	0x0028	32
SRBC0	RW	0x0000_0000	0x00C4	32
SRBC1	RW	0x0000_0000	0x00AC	32
MESTSEL	RW	0x0000_0000	0x00EC	32
MEMSCR0	RW	0x0104_1041	0x00F0	32
MEMSCR1	RW	0x0000_0001	0x00F4	32
MEMPDR0	RW	0xFFFF_FFFF	0x00F8	32

12.6.2.1 Low Power Control Register(LCR,0x0004)

The Low Power Control Register (LCR) is a 32-bit read/write register that controls low-power mode status. It is initialized to 0x00000000 by any reset.

	LCR																															BASE + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														LPM	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1:0	LPM	Low Power Mode. Specifies which low-power mode will be entered when SLEEP instruction is executed. Bit 1~0: 00: IDLE mode will be entered when SLEEP instruction is executed 01: SLEEP mode will be entered when SLEEP instruction is executed	RW

12.6.2.2 Clock Gate Register 0(CLKGR0,0x0020)

The Clock Gate Register (CLKGR0) is a 32-bit read/write register that controls the CLOCK GATE function of peripherals. It is reset to 0x1FFFFF80.

	CLKGR0																																BASE + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKGR0																															
RST	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CLKGR0	Clock gate Bits. Controls the clock supplies to some peripherals. If set, clock supplies to associated devices are stopped, and registers of the device cannot be accessed also. The reset value of this register reflects the clock gate information of the relative modules. RST 0: After reset period, the clock is not stopped. RST 1: After reset period, the clock is stopped.	RW

Bit	Module	Description
31	DDR	If set, gate the clock.
30	TCU	If set, gate the clock.(pclk)
29	RTC	If set, gate the clock.
28	DES	If set, gate the clock.
27	Reserved	Reserved bit
26	Reserved	Reserved bit
25	MIPI_CSI	If set, gate the clock.
24	LCD	If set, gate the clock.
23	ISP	If set, gate the clock.
22	H1ARB	If set, gate the clock.

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		21	PDMA	If set, gate the clock.
		20	SFC	If set, gate the clock.
		19	SSI1	If set, gate the clock.
		18	Reserved	Reserved bit.
		17	Reserved	Reserved bit.
		16	Reserved	Reserved bit.
		15	UART1	If set, gate the clock.
		14	UART0	If set, gate the clock.
		13	SADC	If set, gate the clock.
		12	DMIC	If set, gate the clock.
		11	AIC	If set, gate the clock.
		10	Reserved	Reserved bit
		9	SMB2	If set, gate the clock.
		8	SMB1	If set, gate the clock.
		7	SMB0	If set, gate the clock.
		6	SSI0	If set, gate the clock.
		5	MSC1	If set, gate the clock.
		4	MSC0	If set, gate the clock.
		3	OTG	If set, gate the clock.
		2	Reserved	Reserved bit
		1	EFUSE	If set, gate the clock.
		0	NEMC	If set, gate the clock.

12.6.2.3 Oscillator and Power Control Register (OPCR,0x0024)

The Oscillator and Power Control Register is a 32-bit read/write register that specifies some special controls to oscillator and analog block. It is initialized to 0x00001500 by reset.

	OPCR																															BASE + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDLE_DIS	Mask_int_req	Reserved	Gate_sclka_bus	Reserved			REQ_MODE	Gate_usbphyclk	Disable_MUX	Reserved		O1ST												SPENDN0	SPENDN1	Reserved	O1SE	Reserved	ERCS	BUS_MODE	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	IDLE_DIS	0: when CPU enters idle mode, CPU clock is stopped 1: When CPU enters idle mode, CPU clock is not stopped	RW
30	MASK_INT	0: interrupt not mask 1: interrupt masked	RW

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		When enters sleep/idle mode, cpu should set MASK_INT 1, hardware will clear.	
29	Reserved	Reserved bit	R
28	GATE_SCLK A_BUS	Gate SCLK_A for AHB0 AHB2 DDR When select MPLL , stop SCLK_A	RW
27:25	Reserved	Reserved bit	R
24	REQ_MODE	0: Before go into sleep mode, CPM send stop req signal to DDR 1: Before go into sleep mode, CPM doesn't send stop req signal to DDR When DDR enters retention mode, software should be set the bit to 1	RW
23	Gate_usbphy clk	cpu set 1 and reset_n is unvalid, To control usbphy's clkgate. 0: disable. 1: when reset_n is unvalid, usbphy's clkgate is valid.	RW
22	Disable_mux	0: sleep mode, glitch free mux clock are stopped 1: sleep mode, glitch free mux clock not stopped	RW
21:20	Reserved	Reserved bit	R
19:8	O1ST	EXCLK Oscillator Stabilize Time. This filed specifies the EXCLK oscillator stabilize time by unit of 16 RTCCLK periods (oscillator stable time O1ST × 16 / 32768) cycles. It is initialized to H'15.	RW
7	SPENDN0	force USB PHY to enter suspend mode when OTG is enable. 0: USB PHY has forced to entered SUSPEND mode 1: USB PHY hasn't forced to entered SUSPEND mode	RW
6	SPENDN1	force USB PHY to enter suspend mode when UHC is enable. 0: USB PHY has forced to entered SUSPEND mode 1: USB PHY hasn't forced to entered SUSPEND mode	RW
5	Reserved	Reserved bit	R
4	O1SE	EXCLK Oscillator Sleep Mode Enable. This filed controls the state of the EXCLK oscillator in Sleep mode. 0: EXCLK oscillator is disabled in Sleep mode 1: EXCLK oscillator is enabled in Sleep mode	RW
3	Reserved	Reserved bit	R
2	ERCS	EXCLK/512 clock and RTCLK clock selection. 0: select EXCLK/512 division ration clock 1: select RTCLK clock the clock only output to CPM SSI TCU INTC_TOP USB.	RW
1	BUS_MODE	The default value is 0 When the value is 1, the BUS access is accelerated. 0: The default value 1: the BUS access is accelerated.	RW
0	Reserved	Reserved bit	R

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12.6.2.4 Clock Gate Register 1(CLKGR1,0x0028)

The Clock Gate Register (CLKGR1) is a 32-bit read/write register that controls the CLOCK GATE function of peripherals. It is reset to 0x000033FF.

	CLKGR1																															BASE + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CLKGR1															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	CLKGR1	Clock gate Bits. Controls the clock supplies to some peripherals. If set, clock supplies to associated devices are stopped, and registers of the device cannot be accessed also. The reset value of this register reflects the clock gate information of the relative modules. RST 0: After reset period, the clock is not stopped. RST 1: After reset period, the clock is stopped.	

Bit	Module	Description
15	CPU	This does not gate any clock, 1'b1: CPM will not give stop request to CPU 1'b0: CPM will give stop request to CPU
14	APB0	This will gate p0clk of some modules on ahb0 whose slave port is APB. such as DDR.
13	Reserved	Reserved bit
12	RADIX	If set, gate the clock.
11	SYS_OST	If set, gate the clock.(hclk and exclk)
10	AHB0	If set, gate the clock.
9	LDC	If set, gate the clock.
8	Mscaler	Reserved bit
7	Reserved	Reserved bit
6	AHB1	If set, gate the clock
5	AES	If set, gate the clock.
4	GMAC	If set, gate the clock.
3	NCU	If set, gate the clock.
2	IPU	If set, gate the clock.

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1	DTRNG	If set, gate the clock	
0	HELIX	If set, gate the clock	

NOTES: you can use XXCDR.XX_STOP, CLKGR.XX or SRBC.XX_STP to stop XX module's clk, and when CLKGR.XX or SRBC XX_STP is set high, CPU can turn into sleep mode successfully, but if only set XXCDR.XX_STOP high, CPU may not turn into sleep mode, because XX module can not give out stop_ack when clk is stopped; CPM will not wait for XX module's stop_ack if you stop it's clk by set CLKGR.XX.

12.6.2.5 Soft Reset and Bus Control Register0 (SRBC0,0x00C4)

The Soft Reset and Bus Control Register is a 32-bit read/write register that control some module reset and bus transmission. It is initialized to 0x0000000 0by reset.

	SRBC0																															BASE + 0x00C4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HELIX_SR	HELIX_STP	HELIX_ACK	RADIX_SR	RADIX_STP	RADIX_ACK	Reserved	IPU_STP	IPU_ACK	ISP_SR	ISP_STP	ISP_ACK	LCD_SR	LCD_STP	LCD_ACK	Reserved	CPU_STP	CPU_ACK	Reserved	OTG1_SR	Reserved	AHB1_STP	AHB1_ACK	AHB2_STP	AHB2_ACK	DDR_STP	DDR0_ACK	Reserved				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	HELIX_SR	0: HELIX does not enter soft reset mode 1: HELIX enters soft reset mode	RW
30	HELIX_STP	Request for HELIX to Stop bus transfer.	RW
29	HELIX_ACK	0: HELIX bus do not finish, need to wait end. 1: HELIX bus stop ack	R
28	RADIX_SR	0: RADIX does not enter soft reset mode 1: RADIX enters soft reset mode	RW
27	RADIX_STP	Request for RADIX to Stop bus transfer.	RW
26	RADIX_ACK	0: RADIX bus do not finish, need to wait end.	R

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		1: RADIX bus stop ack	
25	Reserved	Writing has no effect, read as zero.	R
24	IPU_STP	Request for IPU to Stop bus transfer. Note: Dont be connected to IPU.	RW
23	IPU_ACK	IPU Stop Ack. Note: ipu_ack be connected to 0.	R
22	ISP_SR	0: ISP does not enter soft reset mode 1: ISP enters soft reset mode	RW
21	ISP_STP	Request for ISP to Stop bus transfer.	RW
20	ISP_ACK	ISP Stop Ack.	R
19	LCD_SR	0: LCD does not enter soft reset mode 1: LCD enters soft reset mode	RW
18	LCD_STP	Request for LCD to Stop bus transfer. Note: Dont be connected to LCD.	RW
17	LCD_ACK	LCD Stop Ack. Note: lcd_ack be connected to 0.	R
16	Reserved	Writing has no effect, read as zero.	R
15	CPU_STP	Request for CPU to Stop bus transfer.	RW
14	CPU_ACK	CPU Stop Ack.	R
13	Reserved	Writing has no effect, read as zero.	R
12	OTG1_SR	OTG soft reset	RW
11	Reserved	Writing has no effect, read as zero.	R
10	AHB1_STP	Request for AHB1 to Stop bus transfer.	RW
9	AHB1_ACK	AHB1 Stop Ack.	R
8	AHB2_STP	Request for AHB2 to Stop bus transfer.	RW
7	AHB2_ACK	AHB2 Stop Ack.	R
6	DDR_STP	Request for DDR to Stop bus transfer.	RW
5	DDR_ACK	DDR Stop Ack.	R
4:0	Reserved	Writing has no effect, read as zero.	R

12.6.2.6 Soft Reset and Bus Control Register1 (SRBC1,0x00AC)

The Soft Reset and Bus Control Register is a 32-bit read/write register that control some module reset and bus transmission. It is initialized to 0x0000000 0by reset.

	SRBC1																															BASE + 0x00AC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							LDC_SR	LDC_STP	LDC_ACK	MSCALER_SR	MSCALER_STP	MSCALER_ACK	NCU_SR	NCU_STP	NCU_ACK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:9	Reserved	Reserved bit	R
8	LDC_SR	0: LDC does not enter soft reset mode 1: LDC enters soft reset mode	RW
7	LDC_STP	Request for LDC to Stop bus transfer.	RW
6	LDC_ACK	0: LDC bus do not finish, need to wait end. 1: LDC bus stop ack	R
5	MSCALER_SR	0: MSCALER does not enter soft reset mode 1: MSCALER enters soft reset mode	RW
4	MSCALER_STP	Request for MSCALER to Stop bus transfer.	RW
3	MSCALER_ACK	0: MSCALER bus do not finish, need to wait end. 1: MSCALER bus stop ack	R
2	NCU_SR	0: NCU does not enter soft reset mode 1: NCU enters soft reset mode	RW
1	NCU_STP	Request for NCU to Stop bus transfer.	RW
0	NCU_ACK	0: NCU bus do not finish, need to wait end. 1: NCU bus stop ack	R

12.6.2.7 CPM MEST SEL Register(MESTSEL,0x00EC)

The MEST(Metastable state) SEL Register is a 32-bit signal synchronized register that control num of clock cycle. between module and module.

	mestsel																															BASE + 0x00EC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							MEST_SEL								
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:9	Reserved.	Read as 0, writing has no effect	R
8	AHB2_APB0_MEST_SEL	AHB0 and APB0 0: Signal synchronized by two clock cycles 1: Signal synchronized by three clock cycles	RW
7	AHB2_DDR_MEST_SEL	AHB2 and DDR 0: Signal synchronized by two clock cycles 1: Signal synchronized by three clock cycles	RW

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6	ISP_DDR_MEST_SEL	ISP and DDR 0: Signal synchronized by two clock cycles 1: Signal synchronized by three clock cycles	RW
5	VPU_DDR_MEST_SEL	VPU and DDR 0: Signal synchronized by two clock cycles 1: Signal synchronized by three clock cycles	RW
4	LCD_DDR_MEST_SEL	LCD and DDR 0: Signal synchronized by two clock cycles 1: Signal synchronized by three clock cycles	RW
3	CPU_DDR_MEST_SEL	CPU and DDR 0: Signal synchronized by two clock cycles 1: Signal synchronized by three clock cycles	RW
2	CPU_VPU_MEST_SEL	CPU and VPU 0: Signal synchronized by two clock cycles 1: Signal synchronized by three clock cycles	RW
1	CPU_AHB0_MEST_SEL	CPU and AHB0 0: Signal synchronized by two clock cycles 1: Signal synchronized by three clock cycles	RW
0	CPU_AHB2_MEST_SEL	CPU and AHB2 0: Signal synchronized by two clock cycles 1: Signal synchronized by three clock cycles	RW

12.6.2.8 Memory Speed Control Register 0(MEMSCR0,0x00F0)

The Memory Speed Control Register 0 is a 32-bit read/write register.

	MEMSCR0																															BASE + 0x00F0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		CPU						APB						AHB2						AHB1						AHB0					
RST	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect. Read as zero.	R
29:24	CPU	CPU Memory Speed Control Register	RW
23:18	APB	APB Memory Speed Control Register	RW
17:12	AHB2	AHB2 Memory Speed Control Register	RW
11:6	AHB1	AHB1 Memory Speed Control Register	RW
5:0	AHB0	AHB0 Memory Speed Control Register	RW

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12.6.2.9 Memory Speed Control Register 1(MEMSCR1,0x00F4)

The Memory Speed Control Register 1 is a 32-bit read/write register.

	MEMSCR1																															BASE + 0x00F4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										ISP					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect. Read as zero.	R
5:0	ISP	ISP Memory Speed Control Register	RW

12.6.2.10 Memory Power-Down Register 0(MEMPDR0,0x00F8)

The Memory Power-Down Control Register 0 is a 32-bit.

	MEMPDR0																															BASE + 0x00F8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	ISP	CPU	APB						AHB2							AHB1							AHB0								
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	ISP	Block ISP Memory Power-Down Control	RW
29	CPU	Block CPU Memory Power-Down Control	RW
28:23	APB	Block APB Memory Power-Down Control Bits / Module / Description 28 / UART1 / 27 / UART0 / 26 / SSI1 / 25 / SSI0 /	RW

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		24	DES			
		23	AIC			
22:15	AHB2	Block AHB2 Memory Power-Down Control				RW
		Bits	**Module**	**Description**		
		22	MSC1			
		21	MSC0			
		20	SFC			
		19	GMAC			
		18	USB			
		17	AES			
		16	PDMA			
		15	HBRI			
14:9	AHB1	Block AHB1 Memory Power-Down Control				RW
		Bits	**Module**	**Description**		
		14	LDC			
		13	LCDC			
		12	IPU			
		11	RADIX			
		10	HELIX			
		9	HBRI	Reserved bit		
8:0	AHB0	Block AHB0 Memory Power-Down Control				RW
		Bits	**Module**	**Description**		
		8	MSCALER			
		7	NCU			
		6	DDR_CH6			
		5	DDR_CH5			
		4	DDR_CH4			
		3	DDR_CH3			
		2	DDR_CH0			
		1	DDR_TOP			
		0	HBRI	Reserved bit		

12.6.3 Doze Mode

Firstly, software should set the DUTY bits of LCR. Then set DOZE bit of LCR to 1 to enter doze mode. When slot controller of PMC indicates that the CPU clock's time-slot has expired, CPU is halted but its register contents are retained. During doze mode, program can modify clock duty-cycle according to core resource requirement. Clock control is in increments of approximately 3% (1/31).

Doze is exited by software, interrupt, reset or SLEEP instruction.

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12.6.4 IDLE Mode

In normal mode, when LPM bits in LCR are 0 and SLEEP instruction is executed, the processor enters idle mode. CPU is halted but its register contents are retained All critical application must be finished and peripherals must be configured to generate interrupts when they need CPU attention.

The procedure of entering sleep mode is shown blow:

1 Set LPM bits in LCR to 0.
2 Executes SLEEP instruction.
3 When current operation of CPU core has finished and CPU core is idle, CCLK supply to CPU core is stopped.

IDLE mode is exited by an interrupt (IRQ or on-chip devices) or a reset.

12.6.5 SLEEP Mode

In normal mode, when LPM bits in LCR is 1 and SLEEP instruction is executed, the processor enter SLEEP mode. CPU and on-chip devices are halted, except some wakeup-logic. PLL is shut off. Clock output from CKO pin is also stopped. SDRAM content is preserved by driving into self-refresh state. CPU registers and on-chip devices registers contents are retained.

Before enter SLEEP mode, software should ensure that all peripherals are not running. The procedure of entering SLEEP mode is shown blow:

1 Set LPM bit in LCR to 1.
2 Execute a SLEEP instruction.
3 When current access on system bus complete, the arbiter will not grant any following request. EMC will drive SDRAM from auto-refresh mode to self-refresh mode.
4 When system bus is idle state and SDRAM is self-refresh mode, internal clock supplies are stopped.
5 SLEEP mode can be exited by an interrupt (IRQ or on-chip devices), WDT reset or a poweron reset via the RESETP pin.

12.7 Reset Control Module

12.7.1 Register Description

All RCM register 32bit access address is physical address.

Name	RW	Initial Value	Address	Access Size
RSR	RW	0x0000_000?	0x08	32

12.7.1.1 Reset Status Register (RSR)

The Reset Status Register (RSR) is a 32-bit read/write register which records last cause of reset. Each RSR bit is set by a different source of reset. Please refer to Reset Sequence Control for reset sources

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description.

	RSR																															BASE+0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												HR	Reserved	WR	PR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	?	1

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	HR	Hibernate Reset. Software can only write 0,Write 1 will be ignored	RW
2	Reserved	Writing has no effect, read as zero.	R
1	WR	WDT Reset. When a WDT reset is detected, WR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 will be ignored. 0: WDT reset has not occurred since the last time the software clears this bit 1: WDT reset has occurred since the last time the software clears this bit	RW
0	PR	Power On Reset. When a power-on reset via PRESET pin is detected, PR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 is ignored. 0: Power on reset has not occurred since the last time the software clears this bit 1: Power on reset has occurred since the last time the software clears this bit	RW

12.7.2 Power On Reset

Power on reset is generated when PRESET pin is driven to low. Internal reset is asserted immediately. All pins return to their reset states. The Power on reset is extended to 40MS.

PRESET pin must be held low until power stabilizes and the EXCLK oscillator stabilize. CPU and peripherals are clocked by EXCLK oscillator output directly. PLL is reset to off state. All internal modules are initialized to their predefined reset states.

12.7.3 WDT Reset

WDT reset is generated when WDT overflow. Internal reset is asserted within two RTCCLK cycles. All pins return to their reset states.

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Then WDT reset source is cleared because of internal reset. The internal reset is asserted for about 10 milliseconds. CPU and peripherals are clocked by EXCLK oscillator output directly. PLL is reset to off state.

12.8 Index

Table 12-5 Description of Proprietary Vocabulary

Name	Description
PLL	Phase locked loops
CGU	Clock generate unit

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13 Timer/Counter Unit

13.1 Overview

The TCU (Timer/Counter with PWM output) contains 4 channels of 16-bit programmable timers (timers 0 to 7). They can be used as Timer or PWM.

TCU has the following features:

- There are two modes of TCU for the eight channels
  - TCU1: Channel 0, 3,4,5,6,7
  - TCU2: Channel 1,2
- Two independent channels, each consisting of
  - Counter
  - Data register (FULL and HALF)
  - Control register
- Independent clock for each counter, selectable by software
  - PCLK, EXTAL and RTCCLK can be used as the clock for counter
  - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- FULL interrupt and HALF interrupt can be generated for each channel using the compare data registers
  - Timer 0-7 can be used as PWM (Set the initial signal level)
  - Timer 0-7 has one interrupt in common
  - OST uses interrupt 0, Timer 0-7 uses interrupt 2
- The difference between TCU1 and TCU2
  - TCU1: It cannot work in sleep mode, but operated easily
  - TCU2: It can work in sleep mode, but operated more complicated than TCU1

13.2 Pin Description

Table 13-1 PWM Pins Description

Name	I/O	Description
PWM [7:0]	Output	PWM channel output signals.

13.3 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

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RSW - read and write, but set to 1 by read
RWC - read and write, clear to 0 by write 1, write 0 has no effect
RWS - read and write, set to 1 by write 1, write 0 has no effect
RC - read only, and clear to 0 by read
RS - read only, and set to 1 by read
SPEC - special access method, relate to its description

3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

13.3.1 Register Memory Map

Table 13-2 Registers Memory Map Base Address

Name	Base	Description
TCU	0x10002000	Address Base of TCU

The Timer/Counter Unit is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 13-3 TCU Registers Map

Name	RW	Reset Value	Address offset	Access Size
TCER	R	0x0000_0000	0x10	16
TCSTR	W	0x0000_?0??	0x14	16
TCCLR	W	0x0000_?0??	0x18	16
TSR	R	0x0000_0000	0x1C	32
TFR	R	0x0000_0000	0x20	32
TFSTR	W	0x00??_?0??	0x24	32
TFCLR	W	0x00??_?0??	0x28	32
TSSTR	W	0x000?_?0??	0x2C	32
TMR	R	0x00FF_80FF	0x30	32
TMSTR	W	0x00??_?0??	0x34	32
TMCLR	W	0x00??_?0??	0x38	32
TSCLR	W	0x000?_?0??	0x3C	32
TDFR0	RW	0x0000_????	0x40	16
TDHR0	RW	0x0000_????	0x44	16
TCNT0	RW	0x0000_????	0x48	16
TCSR0	RW	0x0000_0000	0x4C	16
TDFR1	RW	0x0000_????	0x50	16
TDHR1	RW	0x0000_????	0x54	16
TCNT1	RW	0x0000_????	0x58	16
TCSR1	RW	0x0000_0000	0x5C	16
TDFR2	RW	0x0000_????	0x60	16
TDHR2	RW	0x0000_????	0x64	16

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TCNT2	RW	0x0000_????	0x68	16
TCSR2	RW	0x0000_0000	0x6C	16
TDFR3	RW	0x0000_????	0x70	16
TDHR3	RW	0x0000_????	0x74	16
TCNT3	RW	0x0000_????	0x78	16
TCSR3	RW	0x0000_0000	0x7C	16
TDFR4	RW	0x0000_????	0x80	16
TDHR4	RW	0x0000_????	0x84	16
TCNT4	RW	0x0000_????	0x88	16
TCSR4	RW	0x0000_0000	0x8C	16
TDFR5	RW	0x0000_????	0x90	16
TDHR5	RW	0x0000_????	0x94	16
TCNT5	RW	0x0000_????	0x98	16
TCSR5	RW	0x0000_0000	0x9C	16
TDFR6	RW	0x0000_????	0xA0	16
TDHR6	RW	0x0000_????	0xA4	16
TCNT6	RW	0x0000_????	0xA8	16
TCSR6	RW	0x0000_0000	0xAC	16
TDFR7	RW	0x0000_????	0xB0	16
TDHR7	RW	0x0000_????	0xB4	16
TCNT7	RW	0x0000_????	0xB8	16
TCSR7	RW	0x0000_0000	0xBC	16
TSTR	R	0x0000_0000	0xF0	32
TSTSTR	W	0x000?_000?	0xF4	32
TSTCLR	W	0x000?_000?	0xF8	32

13.3.2 Register and Fields Description

13.3.2.1 Timer Counter Enable Register (TCER,0x10)

The TER is a 16-bit read-only register. It contains the counter enable control bits for each channel. It is initialized to 0x0000 by any reset. It can only be set by register TESR and TECR. Since the timer enable control bits are located in the same addresses, two or more timers can be started at the same time.

	TER																															Base + 0x10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSTEN	Reserved							TCEN7	TCEN6	TCEN5	TCEN4	TCEN 3	TCEN 2	TCEN 1	TCEN 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
15	OSTEN	Enable the counter in OST. 0: Stop counting up 1: Begin counting up	R
14:8	Reserved	Writing has no effect, read as zero.	R
7	TCEN 7	Enable the counter in timer 7. 0: Stop counting up 1: Begin counting up	R
6	TCEN 6	Enable the counter in timer 6. 0: Stop counting up 1: Begin counting up	R
5	TCEN 5	Enable the counter in timer 5. 0: Stop counting up 1: Begin counting up	R
4	TCEN 4	Enable the counter in timer 4. 0: Stop counting up 1: Begin counting up	R
3	TCEN 3	Enable the counter in timer 3. 0: Stop counting up 1: Begin counting up	R
2	TCEN 2	Enable the counter in timer 2. 0: Stop counting up 1: Begin counting up	R
1	TCEN 1	Enable the counter in timer 1. 1: Begin counting up 0: Stop counting up	R
0	TCEN 0	Enable the counter in timer 0. 0: Stop counting up 1: Begin counting up	R

13.3.2.2 Timer Counter Enable Set Register (TCSTR,0x14)

The TCSTR is a 32-bit write-only register. It contains the counter enable set bits for each channel. Since the timer enable control set bits are located in the same addresses, two or more timers can be started at the same time.

	TESR																															Base + 0x14
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSTST	Reserved							TCST 7	TCST 6	TCST 5	TCST 4	TCST 3	TCST 2	TCST 1	TCST 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

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Bits	Name	Description	RW
15	OSTST	Set OSTEN bit of TER. 0: Ignore 1: Set OSTEN bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	RW
7	TCST 7	Set TCEN 7 bit of TER. 0: Ignore 1: Set TCEN 7 bit to 1	W
6	TCST 6	Set TCEN 6 bit of TER 0: Ignore. 1: Set TCEN 6 bit to 1	W
5	TCST 5	Set TCEN 5 bit of TER. 0: Ignore 1: Set TCEN 5 bit to 1	W
4	TCST 4	Set TCEN 4 bit of TER. 0: Ignore 1: Set TCEN 4 bit to 1	W
3	TCST 3	Set TCEN 3 bit of TER. 0: Ignore 1: Set TCEN 3 bit to 1	W
2	TCST 2	Set TCEN 2 bit of TER. 0: Ignore 1: Set TCEN 2 bit to 1	W
1	TCST 1	Set TCEN 1 bit of TER. 0: Ignore 1: Set TCEN 1 bit to 1	W
0	TCST 0	Set TCEN 0 bit of TER. 0: Ignore 1: Set TCEN 0 bit to 1	W

13.3.2.3 Timer Counter Enable Clear Register (TCCLR,0x18)

The TECR is a 32-bit write-only register. It contains the counter enable clear bits for each channel. Since the timer enable clear bits are located in the same addresses, two or more timers can be stop at the same time.

	TECR																															
																																Base + 0x18
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSTCL	Reserved							TCCL 7	TCCL 6	TCCL 5	TCCL 4	TCCL 3	TCCL 2	TCCL 1	TCCL 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
15	OSTCL	Set OSTEN bit of TER. 0: Ignore 1: Set OSTEN 5 bit to 0	W
14:8	Reserved	Writing has no effect, read as zero.	RW
7	TCCL 7	Set TCEN 7 bit of TER. 0: Ignore 1: Set TCEN 7 bit to 0	W
6	TCCL 6	Set TCEN 6 bit of TER.	W

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		0: Ignore 1: Set TCEN 6 bit to 0	
5	TCCL 5	Set TCEN 5 bit of TER. 0: Ignore 1: Set TCEN 5 bit to 0	W
4	TCCL 4	Set TCEN 4 bit of TER. 0: Ignore 1: Set TCEN 4 bit to 0	W
3	TCCL 3	Set TCEN 3 bit of TER. 0: Ignore 1: Set TCEN 3 bit to 0	W
2	TCCL 2	Set TCEN 2 bit of TER. 0: Ignore 1: Set TCEN 2 bit to 0	W
1	TCCL 1	Set TCEN 1 bit of TER. 0: Ignore 1: Set TCEN 1 bit to 0	W
0	TCCL 0	Set TCEN 0 bit of TER. 0: Ignore 1: Set TCEN 0 bit to 0	W

13.3.2.4 Timer Stop Register (TSR,0x1C)

The TSR is a 32-bit read-only register. It contains the timer stop control bits for each channel, WDT and OST. It is initialized to 0x00000000 by any reset. It can only be set by register TSSR and TSCR. If set, clock supplies to timer n / WDT / OST is stopped, and registers of the timer / WDT / OST cannot be accessed also.

	TSR																																Base + 0x1C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTS	OSTS	Reserved							STOP7	STOP6	STOP5	STOP4	STOP 3	STOP 2	STOP 1	STOP 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTS	0: The clock supplies to WDT is supplied 1: The clock supplies to WDT is stopped	R
15	OSTS	0: The clock supplies to OST is supplied 1: The clock supplies to OST is stopped	R
14:8	Reserved	Writing has no effect, read as zero.	R
7	STOP 7	0: The clock supplies to timer 7 is supplied 1: The clock supplies to timer 7 is stopped	R
6	STOP 6	0: The clock supplies to timer 6 is supplied 1: The clock supplies to timer 6 is stopped	R
5	STOP 5	0: The clock supplies to timer 5 is supplied 1: The clock supplies to timer 5 is stopped	R

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4	STOP 4	0: The clock supplies to timer 4 is supplied 1: The clock supplies to timer 4 is stopped	R
3	STOP 3	0: The clock supplies to timer 3 is supplied 1: The clock supplies to timer 3 is stopped	R
2	STOP 2	0: The clock supplies to timer 2 is supplied 1: The clock supplies to timer 2 is stopped	R
1	STOP 1	0: The clock supplies to timer 1 is supplied 1: The clock supplies to timer 1 is stopped	R
0	STOP 0	0: The clock supplies to timer 0 is supplied 1: The clock supplies to timer 0 is stopped	R

13.3.2.5 Timer Flag Register (TFR,0x20)

The TFR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It can also be set by register TFSR and TFCR. It is initialized to 0x00000000 by any reset.

	TFR																															Base + 0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFLAG 3	HFLAG 2	HFLAG 1	HFLAG 0	HFLAG 3	HFLAG 2	HFLAG 1	HFLAG 0	OSTFLAG	Reserved							FFLAG 7	FFLAG 6	FFLAG 5	FFLAG 4	FFLAG 3	FFLAG 2	FFLAG 1	FFLAG 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HFLAG 7~0	HALF comparison match flag. (TCNT = TDHR) 0: Comparison not match 1: Comparison match	R
15	OSTFLAG	OST comparison match flag. (OSTCNT = OSTDR) 0: Comparison not match 1: Comparison match	R
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFLAG 7~0	FULL comparison match flag. (TCNT = TDFR) 0: Comparison not match 1: Comparison match	R

13.3.2.6 Timer Flag Set Register (TFSTR,0x24)

The TFSR is a 32-bit write-only register. It contains the comparison match flag set bits for all the channels.

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	TFSR																															Base + 0x24
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFST7	HFST6	HFST5	HFST4	HFST 3	Reserved		HFST 0	OSTFST	Reserved							FFST7	FFST6	FFST5	FFST4	FFST 3	Reserved		FFST 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	0	0	?	?	0	0	0	0	0	0	0	?	?	?	?	?	0	0	?

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:19	HFST 23~19	Set HFLAG n bit of TFR. 0: Ignore 1: Set HFLAG n bit to 1	W
18:17	Reserved	Writing has no effect, read as zero.	R
16	HFST0	Set HFLAG 0 bit of TFR. 0: Ignore 1: Set HFLAG n bit to 1	W
15	OSTFST	Set OSTFLAG n bit of TFR. 0: Ignore 1: Set OSTFLAG n bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:3	FFST 7~3	Set FFLAG n bit of TFR. 0: Ignore 1: Set FFLAG n bit to 1	W
2:1	Reserved	Writing has no effect, read as zero.	R
0	FFST0	Set FFLAG 0 bit of TFR. 0: Ignore 1: Set FFLAG n bit to 1	W

13.3.2.7 Timer Flag Clear Register (TFCLR,0x28)

The TFCR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.

	TFCR																															Base + 0x28
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFCL7	HFCL6	HFCL5	HFCL4	HFCL 3	HFCL 2	HFCL 1	HFCL 0	OSTFCL	Reserved							FFCL7	FFCL6	FFCL5	FFCL4	FFCL 3	FFCL 2	FFCL 1	FFCL 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HFCL 16~23	Set HFLAG n bit of TFR.	W

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		0: Ignore 1: Set FFLAG n bit to 0	
15	OSTFCL	Set OSTFLAG n bit of TFR. 0: Ignore 1: Set OSTFLAG n bit to 0	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFCL 7~0	Set FFLAG n bit of TFR. 0: Ignore 1: Set FFLAG n bit to 0	W

13.3.2.8 Timer Stop Set Register (TSSTR,0x2C)

The TCSR is an 32-bit write-only register. It contains the timer stop set bits for each channel, WDT and OST. Since the timer stop control set bits are located in the same addresses, two or more timers can be started at the same time.

	TSSR																															Base + 0x2C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTSS	OSTSS	Reserved							STPS7	STPS6	STPS5	STPS4	STPS 3	STPS 2	STPS 1	STPS 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTSS	Set WDTS bit of TSR. 0: Ignore 1: Set WDTS bit to 1	W
15	OSTSS	Set OSTS bit of TSR. 0: Ignore 1: Set OSTS bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	R
7	STPS 7	Set STOP 7 bit of TSR. 0: Ignore 1: Set STOP 7 bit to 1	W
6	STPS 6	Set STOP 6 bit of TSR. 0: Ignore 1: Set STOP 6 bit to 1	W
5	STPS 5	Set STOP 5 bit of SR. 0: Ignore 1: Set STOP 5 bit to 1	W

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4	STPS 4	Set STOP 4 bit of TSR. 0: Ignore 1: Set STOP 4 bit to 1	W
3	STPS 3	Set STOP 3 bit of TSR. 0: Ignore 1: Set STOP 3 bit to 1	W
2	STPS 2	Set STOP 2 bit of TSR. 0: Ignore 1: Set STOP 2 bit to 1	W
1	STPS 1	Set STOP 1 bit of SR. 0: Ignore 1: Set STOP 1 bit to 1	W
0	STPS 0	Set STOP 0 bit of TSR. 0: Ignore 1: Set STOP 0 bit to 1	W

13.3.2.9 Timer Mast Register (TMR,0x30)

The TMR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It is initialized to 0x003F003F by any reset. It can only be set by register TMSR and TMCR.

	TMR																															Base + 0x30
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HMASK7	HMASK6	HMASK5	HMASK4	HMASK 3	HMASK 2	HMASK 1	HMASK 0	OSTMASK	Reserved							FMASK7	FMASK6	FMASK5	FMASK4	FMASK 3	FMASK 2	FMASK 1	FMASK 0
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HMASK 23~16	HALF comparison match interrupt mask. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask	R
15	OSTMASK	OST comparison match interrupt mask. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask	R
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMASK 7~0	FULL comparison match interrupt mask. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask	R

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13.3.2.10 Timer Mask Set Register (TMSTR,0x34)

The TMSR is a 32-bit write-only register. It contains the comparison match flag set bits for all the channels.

	TMSR																															Base + 0x34
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HMST7	HMST6	HMST5	HMST4	HMST 3	HMST 2	HMST 1	HMST 0	OSTMST	Reserved							FMST7	FMST6	FMST5	FMST4	FMST 3	FMST 2	FMST 1	FMST 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HMST 23~16	Set HMASK n bit of TMR. 0: Ignore 1: Set HMASK n bit to 1	W
15	OSTMST	Set OSTMASK n bit of TMR. 0: Ignore 1: Set OSTMASK n bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMST 7~0	Set FMASK n bit of TMR. 0: Ignore 1: Set FMASK n bit to 1	W

13.3.2.11 Timer Mask Clear Register (TMCLR,0x38)

The TMCR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.

	TMCR																															Base + 0x38
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HMCL7	HMCL6	HMCL5	HMCL4	HMCL 3	HMCL 2	HMCL 1	HMCL 0	OSTMCL	Reserved							FMCL7	FMCL6	FMCL5	FMCL4	FMCL 3	FMCL 2	FMCL 1	FMCL 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HMCL 23~16	Set HMASK n bit of TMR.	W

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		0: Ignore 1: Set HMASK n bit to 0	
15	OSTMCL	Set OSTMASK n bit of TMR. 0: Ignore 1: Set OSTMASK n bit to 0	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMCL 7~0	Set FMASK n bit of TMR. 0: Ignore 1: Set FMASK n bit to 0	W

13.3.2.12 Timer Stop Clear Register (TSCLR,0x3C)

The TSCR is an 32-bit write-only register. It contains the timer stop clear bits for each channel, WDT and OST. Since the timer stop clear bits are located in the same addresses, two or more timers can be stop at the same time.

	TSCR																															Base + 0x3C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTSC	OSTSC	Reserved							STPC7	STPC6	STPC5	STPC4	STPC 3	STPC 2	STPC 1	STPC 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTSC	Set WDTS bit of TSR. 0: Ignore 1: Set WDTS bit to 0	W
15	OSTSC	Set OSTS bit of TSR. 0: Ignore 1: Set OSTS bit to 0	W
14:8	Reserved	Writing has no effect, read as zero.	R
7	STPC 7	Set STOP 7 bit of TSR. 0: Ignore 1: Set STOP 7 bit to 0	W
6	STPC 6	Set STOP 6 bit of TSR. 0: Ignore 1: Set STOP 6 bit to 0	W
5	STPC 5	Set STOP 5 bit of TSR. 0: Ignore 1: Set STOP 5 bit to 0	W

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4	STPC 4	Set STOP 4 bit of TSR. 0: Ignore 1: Set STOP 4 bit to 0	W
3	STPC 3	Set STOP 3 bit of TSR. 0: Ignore 1: Set STOP 3 bit to 0	W
2	STPC 2	Set STOP 2 bit of TSR. 0: Ignore 1: Set STOP 2 bit to 0	W
1	STPC 1	Set STOP 1 bit of TSR. 0: Ignore 1: Set STOP 1 bit to 0	W
0	STPC 0	Set STOP 0 bit of TSR. 0: Ignore 1: Set STOP 0 bit to 0	W

13.3.2.13 Timer Data FULL Register0(TDFR0,0x40)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDFR0																															Base + 0x40
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.14 Timer Data HALF Register0 (TDHR0,0x44)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDHR0																															Base + 0x44
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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13.3.2.15 Timer Counter0 (TCNT0,0x48)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCNT0																															Base + 0x48
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.16 Timer Control Register0 (TCSR0,0x4C)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCSR0																															Base + 0x4C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				BYPASS	Reserved	SD	INITL	PWM_EN	PWM_IN_EN	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	BYPASS	PWM bypass mode. 1: If RTC_EN = 1, this channel output RTCCLK; If EXT_EN = 1, this channel output EXTAL; Only one of those XXX_EN is permit available during one time. 0: This BYPASS function disable. *Only when you want to let this PWM channel output some special clock (RTCLK and EXTAL clock), you can set this register to 1. Otherwise keep it to 0. When you want to use BYPASS function, not forget offer clock supplies of relate channel (relate to register TSR, TSSR, TSCR).(the current version can not bypass pclk, and when bypass a clk, the relative timer will be stopped to reduce power consumption.)	RW

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<table>
<tr><td>10</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>9</td><td>SD</td><td>Shut Down (SD) the PWM output. It is only used in TCU1 mode.
0: Graceful shutdown
1: Abrupt shutdown
Graceful shutdown: The output level for PWM output will keep the level only after the comparison match of FULL.(when write register to stop the timer, the timer will continue run until full match)
Abrupt shutdown: The output level for PWM output will keep the level as soon as software write to stop the counter.(the counter will stop as soon as software write to stop the counter).</td><td>RW</td></tr>
<tr><td>8</td><td>INITL</td><td>Selects an initial output level for PWM output.
0: Low 1: High</td><td>RW</td></tr>
<tr><td>7</td><td>PWM_EN</td><td>PWM output pin control bit.
0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL
1: PWM pin output enable(only channel0~channel3 are available currently)</td><td>RW</td></tr>
<tr><td>6</td><td>PWM_IN_EN</td><td>PWM input mode enable.
Set to 1 to enable this function.
In this function, PWM pin need to set GPIO as function0 to receive external signal, EXT_EN, RTC_EN, PCK_EN need to set 0.
And TCNT became a counter to count this signal’s both edges.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>1</td><td>RTC_EN</td><td>Select RTCCLK as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>0</td><td>PCK_EN</td><td>Select PCLK as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
</table>

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13.3.2.17 Timer Data FULL Register1 (TDFR1,0x50)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate) But it is not suggested changing when counter is working in TCU2 mode.

	TDFR1																															Base + 0x50
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.18 Timer Data HALF Register1 (TDHR1,0x54)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate) But it is not suggested changing when counter is working in TCU2 mode.

	TDHR1																															Base + 0x54
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.19 Timer Counter1 (TCNT1,0x58)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up.**TCU2:** The counter data can be read out at any time, but you should read TSTR.REALn to check whether the data is real data or not. The data can only be written before counter is started, and the counter clock is pclk. But it can be cleared to 0 by setting TCSR.CLRZ to 1, and if the counter is really cleared, TCSR.CLRZ will be set to 0 by hardware.

	TCNT1																															Base + 0x58
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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13.3.2.20 Timer Control Register1(TCSR1,0x5C)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCSR1																															Base + 0x5C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				BYPASS	CLRZ	SD	INITL	PWM_EN	Reserved	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	BYPASS	PWM bypass mode. 1: If RTC_EN = 1, this channel output RTCCLK; If EXT_EN = 1, this channel output EXTAL; Only one of those XXX_EN is permit available during one time. 0: This BYPASS function disable. *Only when you want to let this PWM channel output some special clock (RTCLK and EXTAL clock), you can set this register to 1. Otherwise keep it to 0. When you want to use BYPASS function, not forget offer clock supplies of relate channel (relate to register TSR, TSSR, TSCR).(the current version can not bypass pclk, and when bypass a clk, the relative timer will be stopped to reduce power consumption.)	RW
10	CLRZ	Clear counter to 0. It is only used in TCU2 mode. Writing 1 to this bit will clear the counter to 0. When the counter is finished setting to 0, it will be cleared by hardware. Writing 0 to this bit will be ignored.	RW
9	SD	Shut Down (SD) the PWM output. It is only used in TCU1 mode. 0: Graceful shutdown 1: Abrupt shutdown Graceful shutdown: The output level for PWM output will keep the level only after the comparison match of FULL.(when write register to stop the timer, the timer will continue run until full match) Abrupt shutdown: The output level for PWM output will keep the level as soon as software write to stop the counter.(the counter will stop as soon as software write to stop the counter).	RW
8	INITL	Selects an initial output level for PWM output. 0: Low 1: High	RW

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7	PWM_EN	PWM output pin control bit. 0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL 1: PWM pin output enable(only channel0~channel3 are available currently)	RW
6	Reserved	Writing has no effect, read as zero.	R
5:3	PRESCALE	These bits select the TCNT count clock frequency. Don't change this field when the channel is running.	RW

Bit 2	Bit1	Bit 0	Description
0	0	0	Internal clock: CLK/1
0	0	1	Internal clock: CLK/4
0	1	0	Internal clock: CLK/16
0	1	1	Internal clock: CLK/64
1	0	0	Internal clock: CLK/256
1	0	1	Internal clock: CLK/1024
110~111			Reserved

2	EXT_EN	Select EXTAL as the timer clock input. 0: Disable 1: Enable	RW
1	RTC_EN	Select RTCCLK as the timer clock input. 0: Disable 1: Enable	RW
0	PCK_EN	Select PCLK as the timer clock input. 0: Disable 1: Enable	RW

13.3.2.21 Timer Data FULL Register2 (TDFR2,0x60)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate) But it is not suggested changing when counter is working in TCU2 mode.

	TDFR2																Base + 0x60															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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13.3.2.22 Timer Data HALF Register2 (TDHR2,0x64)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate) But it is not suggested changing when counter is working in TCU2 mode.

	TDHR2																															Base + 0x64
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.23 Timer Counter2 (TCNT2,0x68)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up.**TCU2:** The counter data can be read out at any time, but you should read TSTR.REALn to check whether the data is real data or not. The data can only be written before counter is started, and the counter clock is pclk. But it can be cleared to 0 by setting TCSR.CLRZ to 1, and if the counter is really cleared, TCSR.CLRZ will be set to 0 by hardware.

	TCNT2																															Base + 0x68
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.24 Timer Control Register2(TCSR2,0x6C)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCSR1																															Base + 0x6C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				BYPASS	CLRZ	SD	INITL	PWM_EN	Reserved	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	BYPASS	PWM bypass mode. 1: If RTC_EN = 1, this channel output RTCCLK; If EXT_EN = 1, this channel output EXTAL; Only one of those XXX_EN is permit available during one time. 0: This BYPASS function disable. *Only when you want to let this PWM channel output some special clock (RTCLK and EXTAL clock), you can set this register to 1. Otherwise keep it to 0. When you want to use BYPASS function, not forget offer clock supplies of relate channel (relate to register TSR, TSSR, TSCR).(the current version can not bypass pclk, and when bypass a clk, the relative timer will be stopped to reduce power consumption.)	RW
10	CLRZ	Clear counter to 0. It is only used in TCU2 mode. Writing 1 to this bit will clear the counter to 0. When the counter is finished setting to 0, it will be cleared by hardware. Writing 0 to this bit will be ignored.	RW
9	SD	Shut Down (SD) the PWM output. It is only used in TCU1 mode. 0: Graceful shutdown 1: Abrupt shutdown Graceful shutdown: The output level for PWM output will keep the level only after the comparison match of FULL.(when write register to stop the timer, the timer will continue run until full match) Abrupt shutdown: The output level for PWM output will keep the level as soon as software write to stop the counter.(the counter will stop as soon as software write to stop the counter).	RW
8	INITL	Selects an initial output level for PWM output. 0: Low 1: High	RW
7	PWM_EN	PWM output pin control bit. 0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL 1: PWM pin output enable(only channel0~channel3 are available currently)	RW
6	Reserved	Writing has no effect, read as zero.	R
5:3	PRESCALE	These bits select the TCNT count clock frequency. Don't change this field when the channel is running.	RW

Bit 2	Bit1	Bit 0	Description
0	0	0	Internal clock: CLK/1
0	0	1	Internal clock: CLK/4
0	1	0	Internal clock: CLK/16
0	1	1	Internal clock: CLK/64

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		1	0	0	Internal clock: CLK/256		
		1	0	1	Internal clock: CLK/1024		
		110~111			Reserved		
2	EXT_EN	Select EXTAL as the timer clock input. 0: Disable 1: Enable					RW
1	RTC_EN	Select RTCCLK as the timer clock input. 0: Disable 1: Enable					RW
0	PCK_EN	Select PCLK as the timer clock input. 0: Disable 1: Enable					RW

13.3.2.25 Timer Data FULL Register3 (TDFR3,0x70)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDFR3																															Base + 0x70
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.26 Timer Data HALF Register3 (TDHR3,0x74)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDHR3																															Base + 0x74
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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13.3.2.27 Timer Counter3 (TCNT3,0x78)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCNT3																															Base + 0x78
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.28 Timer Control Register3(TCSR3,0x7C)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCSR3																															Base + 0x7C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				BYPASS	Reserved	SD	INITL	PWM_EN	PWM_IN_EN	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	BYPASS	PWM bypass mode. 1: If RTC_EN = 1, this channel output RTCCLK; If EXT_EN = 1, this channel output EXTAL; Only one of those XXX_EN is permit available during one time. 0: This BYPASS function disable. *Only when you want to let this PWM channel output some special clock (RTCLK and EXTAL clock), you can set this register to 1. Otherwise keep it to 0. When you want to use BYPASS function, not forget offer clock supplies of relate channel (relate to register TSR, TSSR, TSCR).(the current version can not bypass pclk, and when bypass a clk, the relative timer will be stopped to reduce power consumption.)	RW

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<table>
<tr><td>10</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>9</td><td>SD</td><td>Shut Down (SD) the PWM output. It is only used in TCU1 mode.
0: Graceful shutdown
1: Abrupt shutdown
Graceful shutdown: The output level for PWM output will keep the level only after the comparison match of FULL.(when write register to stop the timer, the timer will continue run until full match)
Abrupt shutdown: The output level for PWM output will keep the level as soon as software write to stop the counter.(the counter will stop as soon as software write to stop the counter).</td><td>RW</td></tr>
<tr><td>8</td><td>INITL</td><td>Selects an initial output level for PWM output.
0: Low 1: High</td><td>RW</td></tr>
<tr><td>7</td><td>PWM_EN</td><td>PWM output pin control bit.
0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL
1: PWM pin output enable(only channel0~channel3 are available currently)</td><td>RW</td></tr>
<tr><td>6</td><td>PWM_IN_EN</td><td>PWM input mode enable.
Set to 1 to enable this function.
In this function, PWM pin need to set GPIO as function0 to receive external signal, EXT_EN, RTC_EN, PCK_EN need to set 0.
And TCNT became a counter to count this signal’s both edges.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>1</td><td>RTC_EN</td><td>Select RTCCLK as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>0</td><td>PCK_EN</td><td>Select PCLK as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
</table>

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13.3.2.29 Timer Data FULL Register4 (TDFR4,0x80)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDFR4																															Base + 0x80
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.30 Timer Data HALF Register4 (TDHR3,0x84)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDHR4																															Base + 0x84
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.31 Timer Counter4 (TCNT4,0x88)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCNT4																															Base + 0x88
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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13.3.2.32 Timer Control Register4(TCSR4,0x8C)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCSR4																															Base + 0x8C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				BYPASS	Reserved	SD	INITL	PWM_EN	PWM_IN_EN	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	BYPASS	PWM bypass mode. 1: If RTC_EN = 1, this channel output RTCCLK; If EXT_EN = 1, this channel output EXTAL; Only one of those XXX_EN is permit available during one time. 0: This BYPASS function disable. *Only when you want to let this PWM channel output some special clock (RTCLK and EXTAL clock), you can set this register to 1. Otherwise keep it to 0. When you want to use BYPASS function, not forget offer clock supplies of relate channel (relate to register TSR, TSSR, TSCR).(the current version can not bypass pclk, and when bypass a clk, the relative timer will be stopped to reduce power consumption.)	RW
10	Reserved	Writing has no effect, read as zero.	R
9	SD	Shut Down (SD) the PWM output. It is only used in TCU1 mode. 0: Graceful shutdown 1: Abrupt shutdown Graceful shutdown: The output level for PWM output will keep the level only after the comparison match of FULL.(when write register to stop the timer, the timer will continue run until full match) Abrupt shutdown: The output level for PWM output will keep the level as soon as software write to stop the counter.(the counter will stop as soon as software write to stop the counter).	RW
8	INITL	Selects an initial output level for PWM output. 0: Low 1: High	RW
7	PWM_EN	PWM output pin control bit. 0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL	RW

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		1: PWM pin output enable(only channel0~channel3 are available currently)	
6	PWM_IN_EN	PWM input mode enable. Set to 1 to enable this function. In this function, PWM pin need to set GPIO as function0 to receive external signal, EXT_EN, RTC_EN, PCK_EN need to set 0. And TCNT became a counter to count this signal's both edges.	RW
5:3	PRESCALE	These bits select the TCNT count clock frequency. Don't change this field when the channel is running.	RW

Bit 2	Bit1	Bit 0	Description
0	0	0	Internal clock: CLK/1
0	0	1	Internal clock: CLK/4
0	1	0	Internal clock: CLK/16
0	1	1	Internal clock: CLK/64
1	0	0	Internal clock: CLK/256
1	0	1	Internal clock: CLK/1024
110~111			Reserved

2	EXT_EN	Select EXTAL as the timer clock input. 0: Disable 1: Enable	RW
1	RTC_EN	Select RTCCLK as the timer clock input. 0: Disable 1: Enable	RW
0	PCK_EN	Select PCLK as the timer clock input. 0: Disable 1: Enable	RW

13.3.2.33 Timer Data FULL Register5 (TDFR5,0x90)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDFR5																															Base + 0x90
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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13.3.2.34 Timer Data HALF Register5 (TDHR5,0x94)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDHR5																															Base + 0x94
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.35 Timer Counter5 (TCNT5,0x98)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCNT5																															Base + 0x98
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.36 Timer Control Register5(TCSR5,0x9C)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCSR5																															Base + 0x9C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				BYPASS	Reserved	SD	INITL	PWM_EN	PWM_IN_EN	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	BYPASS	PWM bypass mode. 1: If RTC_EN = 1, this channel output RTCCLK; If EXT_EN = 1, this channel output EXTAL; Only one of those XXX_EN is permit available during one time. 0: This BYPASS function disable. *Only when you want to let this PWM channel output some special clock (RTCLK and EXTAL clock), you can set this register to 1. Otherwise keep it to 0. When you want to use BYPASS function, not forget offer clock supplies of relate channel (relate to register TSR, TSSR, TSCR).(the current version can not bypass pclk, and when bypass a clk, the relative timer will be stopped to reduce power consumption.)	RW
10	Reserved	Writing has no effect, read as zero.	R
9	SD	Shut Down (SD) the PWM output. It is only used in TCU1 mode. 0: Graceful shutdown 1: Abrupt shutdown Graceful shutdown: The output level for PWM output will keep the level only after the comparison match of FULL.(when write register to stop the timer, the timer will continue run until full match) Abrupt shutdown: The output level for PWM output will keep the level as soon as software write to stop the counter.(the counter will stop as soon as software write to stop the counter).	RW
8	INITL	Selects an initial output level for PWM output. 0: Low 1: High	RW
7	PWM_EN	PWM output pin control bit. 0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL 1: PWM pin output enable(only channel0~channel3 are available currently)	RW
6	PWM_IN_EN	PWM input mode enable. Set to 1 to enable this function. In this function, PWM pin need to set GPIO as function0 to receive external signal, EXT_EN, RTC_EN, PCK_EN need to set 0. And TCNT became a counter to count this signal's both edges.	RW
5:3	PRESCALE	These bits select the TCNT count clock frequency. Don't change this field when the channel is running. Bit 2 / Bit1 / Bit 0 / Description 0 / 0 / 0 / Internal clock: CLK/1 0 / 0 / 1 / Internal clock: CLK/4	RW

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		0	1	0	Internal clock: CLK/16		
		0	1	1	Internal clock: CLK/64		
		1	0	0	Internal clock: CLK/256		
		1	0	1	Internal clock: CLK/1024		
		110~111			Reserved		
2	EXT_EN	Select EXTAL as the timer clock input. 0: Disable 1: Enable					RW
1	RTC_EN	Select RTCCLK as the timer clock input. 0: Disable 1: Enable					RW
0	PCK_EN	Select PCLK as the timer clock input. 0: Disable 1: Enable					RW

13.3.2.37 Timer Data FULL Register6 (TDFR6,0xA0)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDFR6																															Base + 0xA0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.38 Timer Data HALF Register6 (TDHR6,0xA4)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDHR6																															Base + 0xA4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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13.3.2.39 Timer Counter6 (TCNT6,0xA8)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCNT6																															Base + 0xA8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.40 Timer Control Register6(TCSR6,0xAC)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCSR6																															Base + 0xAC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				BYPASS	Reserved	SD	INITL	PWM_EN	PWM_IN_EN	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	BYPASS	PWM bypass mode. 1: If RTC_EN = 1, this channel output RTCCLK; If EXT_EN = 1, this channel output EXTAL; Only one of those XXX_EN is permit available during one time. 0: This BYPASS function disable. *Only when you want to let this PWM channel output some special clock (RTCLK and EXTAL clock), you can set this register to 1. Otherwise keep it to 0. When you want to use BYPASS function, not forget offer clock supplies of relate channel (relate to register TSR, TSSR, TSCR).(the current version can not bypass pclk, and when bypass a clk, the relative timer will be stopped to reduce power consumption.)	RW

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<table>
<tr><td>10</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>9</td><td>SD</td><td>Shut Down (SD) the PWM output. It is only used in TCU1 mode.
0: Graceful shutdown
1: Abrupt shutdown
Graceful shutdown: The output level for PWM output will keep the level only after the comparison match of FULL.(when write register to stop the timer, the timer will continue run until full match)
Abrupt shutdown: The output level for PWM output will keep the level as soon as software write to stop the counter.(the counter will stop as soon as software write to stop the counter).</td><td>RW</td></tr>
<tr><td>8</td><td>INITL</td><td>Selects an initial output level for PWM output.
0: Low 1: High</td><td>RW</td></tr>
<tr><td>7</td><td>PWM_EN</td><td>PWM output pin control bit.
0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL
1: PWM pin output enable(only channel0~channel3 are available currently)</td><td>RW</td></tr>
<tr><td>6</td><td>PWM_IN_EN</td><td>PWM input mode enable.
Set to 1 to enable this function.
In this function, PWM pin need to set GPIO as function0 to receive external signal, EXT_EN, RTC_EN, PCK_EN need to set 0.
And TCNT became a counter to count this signal’s both edges.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>1</td><td>RTC_EN</td><td>Select RTCCLK as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>0</td><td>PCK_EN</td><td>Select PCLK as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
</table>

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13.3.2.41 Timer Data FULL Register7 (TDFR7,0xB0)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDFR7																															Base + 0xB0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.42 Timer Data HALF Register7 (TDHR7,0xB4)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDHR7																															Base + 0xB4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

13.3.2.43 Timer Counter7 (TCNT7,0xB8)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCNT7																															Base + 0xB8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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13.3.2.44 Timer Control Register7(TCSR7,0xBC)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCSR7																																Base + 0xBC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				BYPASS	Reserved	SD	INITL	PWM_EN	PWM_IN_EN	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	BYPASS	PWM bypass mode. 1: If RTC_EN = 1, this channel output RTCCLK; If EXT_EN = 1, this channel output EXTAL; Only one of those XXX_EN is permit available during one time. 0: This BYPASS function disable. *Only when you want to let this PWM channel output some special clock (RTCLK and EXTAL clock), you can set this register to 1. Otherwise keep it to 0. When you want to use BYPASS function, not forget offer clock supplies of relate channel (relate to register TSR, TSSR, TSCR).(the current version can not bypass pclk, and when bypass a clk, the relative timer will be stopped to reduce power consumption.)	RW
10	Reserved	Writing has no effect, read as zero.	R
9	SD	Shut Down (SD) the PWM output. It is only used in TCU1 mode. 0: Graceful shutdown 1: Abrupt shutdown Graceful shutdown: The output level for PWM output will keep the level only after the comparison match of FULL.(when write register to stop the timer, the timer will continue run until full match) Abrupt shutdown: The output level for PWM output will keep the level as soon as software write to stop the counter.(the counter will stop as soon as software write to stop the counter).	RW
8	INITL	Selects an initial output level for PWM output. 0: Low 1: High	RW
7	PWM_EN	PWM output pin control bit. 0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL	RW

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<table>
<tr><td></td><td></td><td>1: PWM pin output enable(only channel0~channel3 are available currently)</td><td></td></tr>
<tr><td>6</td><td>PWM_IN_EN</td><td>PWM input mode enable.
Set to 1 to enable this function.
In this function, PWM pin need to set GPIO as function0 to receive external signal, EXT_EN, RTC_EN, PCK_EN need to set 0. And TCNT became a counter to count this signal's both edges.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don't change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>1</td><td>RTC_EN</td><td>Select RTCCLK as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>0</td><td>PCK_EN</td><td>Select PCLK as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
</table>

NOTE: The input clock of timer and the PCLK should keep to the rules as follows:

Input clock of timer: IN_CLK	**Clock generated from the frequency divider (PRESCALE): DIV_CLK**
PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

13.3.2.45 Timer Status Register (TSTR,0xF0)

The TSTR is a 32-bit read-only register. It contains the status of channel in TCU2 mode. The register can be written by setting register TSTSR and TSTCR.

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	TSTR																																Base + 0xF0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													REAL2	REAL1	Reserved														BUSY2	BUSY1	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	REAL 2	0: The value read from counter 2 is a false value 1: The value read from counter 2 is a real value	R
17	REAL1	0: The value read from counter 1 is a false value 1: The value read from counter 1 is a real value	R
16:3	Reserved	Writing has no effect, read as zero.	R
2	BUSY 2	0: The counter 2 is ready now 1: The counter 2 is busy now	R
1	BUSY1	0: The counter 1 is ready now 1: The counter 1 is busy now	R
0	Reserved	Writing has no effect, read as zero.	R

13.3.2.46 Timer Status Set Register (TSTSTR,0xF4)

The TSTSR is a 32-bit write-only register. It contains the timer status set bits for each channel.

	TSTSR																																Base + 0xF4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													REAL2	REAL1	Reserved														BUSY2	BUSY1	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	REALS 2	Set REAL 2 bit of TSTR. 0: Ignore 1: Set REAL 2 bit to 1	R
17	REALS 1	Set REAL 1 bit of TSTR. 0: Ignore 1: Set REAL 1 bit to 1	R

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16:3	Reserved	Writing has no effect, read as zero.	R
2	BUSYS 2	Set BUSY 2 bit of TSTR. 0: Ignore 1: Set BUSY 2 bit to 1	R
1	BUSYS 1	Set BUSY 1 bit of TSTR. 0: Ignore 1: Set BUSY 1 bit to 1	R
0	Reserved	Writing has no effect, read as zero.	R

13.3.2.47 Timer Status Clear Register (TSTCLR,0xF8)

The TSTCR is a 32-bit write-only register. It contains the timer status clear bits for each channel.

	TSTCR																																Base + 0xF8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													REAL2	REAL1	Reserved														BUSY2	BUSY1	Reserved
RST	.0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	REALC 2	Clear REAL 2 bit of TSTR. 0: Ignore 1: Clear REAL 2 bit to 1	R
17	REALC 1	Clear REAL 1 bit of TSTR. 0: Ignore 1: Clear REAL 1 bit to 1	R
16:3	Reserved	Writing has no effect, read as zero.	R
2	BUSYC 2	Clear BUSY 2 bit of TSTR. 0: Ignore 1: Clear BUSY 2 bit to 1	R
1	BUSYC 1	Clear BUSY 1 bit of TSTR. 0: Ignore 1: Clear BUSY 1 bit to 1	R
0	Reserved	Writing has no effect, read as zero.	R

13.4 Operation

13.4.1 Basic Operation in TCU1 Mode

The value of TDFR should be bigger than TDHR, and the minimum settings are TDHR = 0 and TDFR

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= 1. In this case, the timer output clock cycle is the input clock × 1/2. If TDHR > TDFR, no comparison TFHR signal is generated.

Before the timer counter begin to count up, we need to do as follows:

If you want to use PWM you should set TCSR.PWM_EN to be 0 before you initial TCU.

1 Initial the configuration.
   a Writing TCSR.INITL to initialize PWM output level.
   b Writing TCSR.SD to setting the shutdown mode (Abrupt shutdown or Graceful shutdown).
   c Writing TCSR.PRESCALE to set TCNT count clock frequency.
   d Setting TCNT, TDHR and TDFR.

2 Enable the clock.
   a Writing TCSR.PWM_EN to set whether enable PWM or disable PWM.
   b Writing TCSR.EXT_EN, TCSR.RTC_EN or TCSR.PCK_EN to 1 to select the input clock and enable the input clock. Only one of TCSR.EXT_EN, TCSR.RTC_EN and TCSR.PCK_EN can be set to 1.

After initialize the register of timer, we should start the counter as follows:

3 Enable the counter.
   Setting the TESR.TCST bit to 1 to enable the TCNT.

NOTES: The input clock and PCLK should follow the rules advanced before.

13.4.2 Disable and Shutdown Operation in TCU1 Mode

1 Setting the TECR.TCCL bit to 1 to disable the TCNT.

13.4.3 Basic Operation in TCU2 Mode

The value of TDFR should be bigger than TDHR, and the minimum settings are TDHR = 0 and TDFR = 1. In this case, the timer output clock cycle is the input clock × 1/2. If TDHR > TDFR, no comparison TFHR signal is generated.

Initial state is that TCSR.PRESCALE=0, TCSR.PWM_EN=0 and TCENR=0.

1 Reset the TCU.
   a Writing TCSR.PCK_EN to 1 to select pclk as the input clock.
   b Set TCSR.CLRZ to 1 to clear TCNT or set TCNT to an initial value.
   c Writing TCSR.PCK_EN to 0 to close the input clock.

2 Initial the configuration.
   a Setting TDHR and TDFR.
   b Writing TCSR.INITL to initialize PWM output level (if used PWM).
   c Writing TCSR.PRESCALE to set TCNT count clock frequency.

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d Writing TCSR.EXT_EN, TCSR.RTC_EN or TCSR.PCK_EN to 1 to select the input clock and enable the input clock. Only one of TCSR.EXT_EN, TCSR.RTC_EN and TCSR.PCK_EN can be set to 1.

e Writing TCSR.PWM_EN to set whether enable PWM or disable PWM.

After initialize the register of timer, we should start the counter as follows:

3 Setting the TESR.TCST bit to 1 to enable the TCNT.

NOTES:

1 You can clear the counter when counter is working.
   a Set TCSR.CLRZ to 1 to clear TCNT.
   b Wait till TSTR.BUSY = 0, that is the counter have been cleared.
2 You can enable PWM or disable PWM the counter when counter is working.
   a Set TCSR.PWM_EN to 1 to enable PWM.
   b Set TCSR.PWM_EN to 0 to disable PWM.

13.4.4 Disable and Shutdown Operation in TCU2 Mode

1 Writing TCSR.PWM_EN to 0 to disable PWM.
2 Setting the TECR.TCCL bit to 1 to disable the TCNT.
3 Wait till TSTR.BUSY = 0, that is the reset of counter is finished.

13.4.5 Read Counter in TCU2 Mode

If you want to read the data from register TCNT when the TCU is working, you can check TSTR.REAL whether it is good or not. It is suggested that:

1 If TSTR.REAL==1, the data read is available.
2 If TSTR.REAL==0, reread the counter till TSTR.REAL==1, the data read is available.
3 If TSTR.REAL is always 0, you can read some data, and lose some data that is quick different from the others. Then choose a data from them as the available data.

NOTES:

1 It suggested that (1), (2) is often used when the counter clock is very slow.
2 It suggested that (3) is often used when the counter clock is very fast.

13.4.6 Pulse Width Modulator (PWM)

Timer 0~3 can be used as Pulse Width Modulator (PWM). The PWM can be used to control the back light inverter or adjust bright or contrast of LCD panel.

FULL comparison match signal and HALF comparison match signal can determine an attribute of the PWM_OUT waveform. FULL comparison match signal specifies the clock cycle for the PWM module clock. HALF comparison match signal specifies the duty ratio for the PWM module clock.

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14 Operating System Timer

14.1 overview

This module include 2 channels, sys_ost32(ost1) and sys_ost64(ost2)

- sys_ost32: 32-bit timer, use to generate operating system's time slice.
  - Has counter Full-match interrupt.
  - Counter by an chip external clock(EXCLK), which can be divide by 1,4,16
  - Read by an asynchronous system clock.

- sys_ost64: 64-bit timer.
  - Counter by an chip external clock(EXCLK), which can be divide by 1,4,16
  - Read by an asynchronous system clock

14.2 feature

- There are three speed mode of the counter, it can be 1,4,16 exclk that the counter add 1.
- The time of interrupt signal enable can be control by user, and is also can be mask by user.
- The counter will set to 0 by user or when it is full.
- This module will disable the hready signal indicate it is operating a read.

14.3 register description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by write 0, write 1 has no effect

   RWS - read and write, set to 1 by write 1, write 0 has no effect

   RC - read only, and clear to 0 by read

   RS - read only, and set to 1 by read

   SPEC - special access method, relate to its description
3. Reset Value

   1 - reset to 1

   0 - reset to 0

   ? - value unknown after reset

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14.3.1 Registers Memory Map

Table 14-1 Registers Memory Map Base Address

Name	Base	Description
SYS_OST	0x12000000	Address base of SYS_OST

The SYS_OST is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 14-2 SYS_OST Registers Map

Name	RW	Reset Value	Address offset	Access Size
OSTCCR	RW	0x0000_0000	0x00	32
OSTER	R	0x0000_0000	0x04	32
OSTCR	RW	0x0000_0000	0x08	32
OSTFR	RWC	0x0000_0000	0x0C	32
OSTMR	RW	0x0000_0001	0x10	32
OST1DFR	RW	0xFFFF_FFFF	0x14	32
OST1CNT	R	0x0000_0000	0x18	32
OST2CNTH	R	0x0000_0000	0x1C	32
OST2CNTL	R	0x0000_0000	0x20	32
OST2CNTHBUF	R	0x0000_0000	0x24	32
OSTESR	W	0x0000_0000	0x34	32
OSTECR	W	0x0000_0000	0x38	32

14.3.2 Register and Fields Description

14.3.2.1 Timer Clock Control Register (OSTCCR,0x00)

	OSTCCR																															Base + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												PRESCALE2		PRESCALE1	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect. Read as zero.	R
3:2	PRESCALE 2	These bits select the TCNT count clock frequency for ost2. Don't change this field when the channel is running.	RW

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		Bit1	Bit 0	Description		
		0	0	Internal clock: CLK/1		
		0	1	Internal clock: CLK/4		
		1	0	Internal clock: CLK/16		
		1	1	Reserved		
1:0	PRESCALE 1	These bits select the TCNT count clock frequency for ost1. Don't change this field when the channel is running.				RW
		Bit1	Bit 0	Description		
		0	0	Internal clock: CLK/1		
		0	1	Internal clock: CLK/4		
		1	0	Internal clock: CLK/16		
		1	1	Reserved		

14.3.2.2 Timer Counter Enable Register (OSTER,0x04)

The OSTER is a 32-bit read-only register. It contains the counter enable control bits for both channels. It is initialized to 0x00000000 by any reset. It can only be set by register OSTESR and OSTECR. Since the timer enable control bits are located in the same addresses, two timers can be started at the same time. (Default: disable)

	OSTER																															Base + 0x04	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														OST2EN	OST1EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect. Read as zero.	R
1	OST2EN	Enable the counter in channel2's timer. 0: Stop counting up 1: Begin counting up	R
0	OST1EN	Enable the counter in channel1's timer 0: Stop counting up 1: Begin counting up	R

14.3.2.3 Timer Counter Clear Register (OSTCR,0x08)

The OSTCR is a 32-bit write-only register. It used to clear the two channel .

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	OSTCR																															Base + 0x08	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														OST2CLR	OST1CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	OST2CLR	Clear the counter in channel2's timer. 0: Invalid 1: Set the counter to 0	W
0	OST1CLR	Clear the counter in channel1's timer. 0: Invalid 1: Set the counter to 0	W

14.3.2.4 Timer Flag Register (OSTFR,0x0C)

The OSTFR is a 32-bit read-only register. It contains the comparison match flag bits for both channels. It is initialized to 0x00000000 by any reset.

	TFR																															Base + 0x0C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															FFLAG
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	FFLAG	channel1's FULL comparison match flag. (OST1CNT = OST1DFR) 0: Comparison not match 1: Comparison match	RWC

14.3.2.5 Timer Mask Register (OSTMR,0x10)

The OSTMR is a 32-bit read-only register. It contains the comparison match flag bits for both channels. It is initialized to 0x00000001 by any reset.

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	OST1MR																															Base + 0x10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															FMASK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	FMASK	Channel1's FULL comparison match interrupt mask. 0: Comparison match interrupt be not masked 1: Comparison match interrupt be masked	RW

14.3.2.6 Timer Data FULL Register (OST1DFR,0x14)

The comparison data FULL registers OST1DFR is used to store the data to be compared with the content of the counter OST1CNT.

	OST1DFR																															Base + 0x14
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST1DFR																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

14.3.2.7 Timer Counter (OST1CNT,0x18)

OST1CNT is a 32-bit read/write register. The up-counter OST1CNT can be reset to 0 by software and counts up using the pre-scale output clock. When OST1CNT count up to equal to OST1DFR, it will reset to 0 and continue to count up.

The counter data can be read out at any time. The data can be clear by OSTCR. (Default: indeterminate)

	OST1CNT																															Base + 0x18
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST1CNT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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14.3.2.8 Operating System Timer Counter (OST2CNTH, 0x1C)

The operating system timer counter (OST2CNT) is a 64-bit read/write counter. OST2CNTH is the high 32 bits and OST2CNTL is the low 32 bits. The up-counter OST2CNT can be enable by software and counts up using the pre-scale output clock. When read OST2CNTL, the OST2CNTH is store at OST2CNTBUF, the software can read OST2CNTBUF to get the total 64-bit number.

	OST2CNTH																															Base + 0x1C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST2CNTH																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14.3.2.9 Operating System Timer Counter (OST2CNTL,0x20)

The operating system timer counter (OST2CNT) is a 64-bit read/write counter. OST2CNTH is the high 32 bits and OST2CNTL is the low 32 bits. The up-counter OST2CNT can be enable by software and counts up using the pre-scale output clock. When read OST2CNTL, the OST2CNTH is store at OST2CNTBUF, the software can read OST2CNTBUF to get the total 64-bit number.

	OST2CNTL																															Base + 0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST2CNTL																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14.3.2.10 Operating System Timer Counter high 32 bits buffer (OST2CNTHBUF,0x24)

The operating system timer counter high 32 bits buffer OST2CNTHBUF is used to store the high 32 bits of OSTCNT2 when its lower 32 bits are read by software. This register can be directly read. (Default: indeterminate)

	OST2CNTHBUF																															Base + 0x24
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST2CNTHBUF																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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14.3.2.11 Timer Counter Enable Set Register (OSTESR,0x34)

The OSTESR is a 32-bit write-only register, It used to set register OSTER.

	OSTESR																															Base + 0x34	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														OST2ENS	OST1ENS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	OST2ENS	Enable the counter in channel2's timer. 0: no effect 1: set OSTER.OST2EN to 1	W
0	OST1ENS	Enable the counter in channel1's timer 0: no effect 1: set OSTER.OST1EN to 1	W

14.3.2.12 Timer Counter Enable Clear Register (OSTECR,0x38)

The OSTECR is a 32-bit write-only register, It used to clear register OSTER.

	OSTECR																															Base + 0x38	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														OST2ENC	OST1ENC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	OST2ENC	Disable the counter in channel2's timer. 0: no effect 1: clear OSTER.OST2EN to 0	W
0	OST1ENC	Disable the counter in channel1's timer 0: no effect 1: clear OSTER.OST1EN to 0	W

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14.4 Operation

14.4.1 Basic Operation in channel1

1.Initial the configuration.
Writing OSTCCR.PRESCALE to set OST1CNT OST2CNT count clock frequency.
Writing OSTCR.OST1CLR and OST2CLR to set the begin number to 0.
2.If the test need to mask the interrupt then you will setting the suit bit of OST1MR
If the test need to enable the ost1's interrupt, then you will setting a acceptable value of OST1DFR, then the counter will enable a interrupt when it's count value is equal to the value you set.

3.After initialize the register of timer, we should start the counter as follows:
Setting the OSTESR.OST1EN(and/or OST2EN) bit to 1 to enable the OST1CNT(and/or OST2CNT). Then it will begin to count up.

14.4.2 Stop Operation in channel1

Set the OSTER.OST1EN 0 to disable the OST1CNT.
Set the OSTER.OST2EN 0 to disable the OST2CNT.

14.4.3 modify the pre-scale in channel1

1.It’s not permitted to modify the pre-scale when the counter is running.
2.if you want to modify the pre-scale, you should
first: Setting the OSTER.OST1EN bit to 0 to disable the OST1CNT. Set the OSTER.OST2EN bit to 0 to disable the OSTCNT
second: modify the pre-scale in OSTCCR
third: Setting the OSTESR.TCST bit to 1 to enable the TCNT again. Setting the TESR.OSTST bit to 1 to enable the OSTCNT again.

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15 Interrupt Controller

15.1 Overview

This chapter describes the interrupt controller included in the XBurst Processor, explains its modes of operation, and defines its registers. The interrupt controller controls the interrupt sources available to the processor and contains the location of the interrupt source to allow software to determine source of all interrupts. It also determines whether an IRQ occurs or not and masks the interrupts.

15.2 Features

- Total 64 interrupt sources
- Each interrupt source can be independently enabled
- Priority mechanism to indicate highest priority interrupt
- All the registers are accessed by CPU
- Unmasked interrupts can wake up the chip in sleep mode

15.3 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

15.3.1 Register Memory Map

Table 15-1 Registers Memory Map Base Address

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Name	Base	Description
INTC	0x10001000	Address base of INTC

The INTC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 15-2 INTC Register Map

Name	RW	Reset Value	Address offset	Access Size
ISR	R	0x0000_0000	0x00	32
IMR	RW	0xFFFF_FFFF	0x04	32
IMSR	W	0x????_????	0x08	32
IMCR	W	0x????_????	0x0C	32
IPR	R	0x0000_0000	0x10	32
ISR1	R	0x0000_0000	0x20	32
IMR1	RW	0xFFFF_FFFF	0x24	32
IMSR1	W	0x????_????	0x28	32
IMCR1	W	0x????_????	0x2C	32
IPR1	R	0x0000_0000	0x30	32

15.3.2 Register and Fields Description

15.3.2.1 Interrupt Controller Source Register (ISR,0x00)

This register contains all the interrupts' status. A "1" indicates that the corresponding interrupt is pending . A "0" indicates that the interrupt is not pending now. The register is read only.

	ISR																															Base + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		ISP	Reserved	TCU0	TCU1	TCU2	Reserved	AES	Reserved	USB	LDC	MSCALER	SADC	GPIO0	GPIO1	GPIO2	GPIO3	Reserved			PDMA	SSI0	SSI1	SFC	IPU	LCDC	MIPI_RX	Reserved		AIC	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect. Read as zero.	R
29	ISP	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
28	Reserved	Writing has no effect. Read as zero.	R

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27:25	TCU	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
24	Reserved	Writing has no effect. Read as zero.	R
23	AES	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
22	Reserved	Writing has no effect. Read as zero.	R
21	USB	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
20:19	Reserved	Writing has no effect. Read as zero.	R
18	SADC	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
17:15	GPIO	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
14:11	Reserved	Writing has no effect. Read as zero.	R
10	PDMA	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
9	SSI0	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
8	SSI1	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
7	SFC	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
6	IPU	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
5:2	Reserved	Writing has no effect. Read as zero.	R
1	AIC	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
0	Reserved	Writing has no effect. Read as zero.	R

15.3.2.2 Interrupt Controller Mask Register (IMR,0x04)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor.

Its value can be changed either by writing IMSR and IMCR or by writing itself. The masked interrupts are invisible to the processor.

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	IMR																																Base + 0x04
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		ISP	Reserved	TCU0	TCU1	TCU2	Reserved	AES	Reserved	USB	LDC	MSCALER	SADC	GPIO0	GPIO1	GPIO2	GPIO3	Reserved			PDMA	SSI0	SSI1	SFC	IPU	LCDC	CSI_RX	Reserved		AIC	Reserved
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect. Read as zero.	R
29	ISP	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
28	Reserved	Writing has no effect. Read as zero.	R
27:25	TCU	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
24	Reserved	Writing has no effect. Read as zero.	R
23	AES	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
22	Reserved	Writing has no effect. Read as zero.	R
21	USB	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
20:19	Reserved	Writing has no effect. Read as zero.	R
18	SADC	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
17:15	GPIO	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
14:11	Reserved	Writing has no effect. Read as zero.	R
10	PDMA	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
9	SSI0	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
8	SSI1	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
7	SFC	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW

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6	IPU	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
5:2	Reserved	Writing has no effect. Read as zero.	R
1	AIC	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
0	Reserved	Writing has no effect. Read as zero.	R

15.3.2.3 Interrupt Controller Mask Set Register (IMSR,0x08)

This register is used to set bits in the interrupt mask register. This register is write only.

	IMSR																															Base + 0x08
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		ISP	Reserved	TCU0	TCU1	TCU2	Reserved	AES	Reserved	USB	LDC	MSCALER	SADC	GPIO0	GPIO1	GPIO2	GPIO3	Reserved			PDMA	SSI0	SSI1	SFC	IPU	LCDC	CSI_RX	Reserved		AIC	Reserved
RST	0	0	?	0	?	?	?	0	?	0	?	?	?	?	?	?	?	?	0	0	0	?	?	?	?	?	?	?	0	0	?	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect. Read as zero.	R
29	ISP	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
28	Reserved	Writing has no effect. Read as zero.	R
27:25	TCU	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
24	Reserved	Writing has no effect. Read as zero.	R
23	AES	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
22	Reserved	Writing has no effect. Read as zero.	R
21	USB	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
20:19	Reserved	Writing has no effect. Read as zero.	R

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18	SADC	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
17:15	GPIO	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
14:11	Reserved	Writing has no effect. Read as zero.	R
10	PDMA	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
9	SSI0	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
8	SSI1	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
7	SFC	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
6	IPU	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
5:2	Reserved	Writing has no effect. Read as zero.	R
1	AIC	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
0	Reserved	Writing has no effect. Read as zero.	R

15.3.2.4 Interrupt Controller Mask Clear Register (IMCR,0x0C)

This register is used to clear bits in the interrupt mask register. This register is write only.

	IMCR																															Base + 0x0C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		ISP	Reserved	TCU0	TCU1	TCU2	Reserved	AES	Reserved	USB	LDC	MSCALER	SADC	GPIO0	GPIO1	GPIO2	GPIO3	Reserved			PDMA	SSI0	SSI1	SFC	IPU	LCDC	CSI_RX	Reserved		AIC	Reserved
RST	0	0	?	0	?	?	?	0	?	0	?	?	?	?	?	?	?	?	0	0	0	?	?	?	?	?	?	?	0	0	?	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect. Read as zero.	R
29	ISP	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W

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28	Reserved	Writing has no effect. Read as zero.	R
27:25	TCU	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
24	Reserved	Writing has no effect. Read as zero.	R
23	AES	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
22	Reserved	Writing has no effect. Read as zero.	R
21	USB	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
20:19	Reserved	Writing has no effect. Read as zero.	R
18	SADC	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
17:15	GPIO	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
14:11	Reserved	Writing has no effect. Read as zero.	R
10	PDMA	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
9	SSI0	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
8	SSI1	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
7	SFC	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
6	IPU	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
5:2	Reserved	Writing has no effect. Read as zero.	R
1	AIC	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
0	Reserved	Writing has no effect. Read as zero.	R

15.3.2.5 Interrupt Controller Pending Register (IPR,0x10)

This register contains the status of the interrupt sources after masking.

This register is read only.

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	IPR																																Base + 0x10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		ISP	Reserved	TCU0	TCU1	TCU2	Reserved	AES	Reserved	USB	LDC	MSCALER	SADC	GPIO0	GPIO1	GPIO2	GPIO3	Reserved			PDMA	SSI0	SSI1	SFC	IPU	LCDC	CSI_RX	Reserved		AIC	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect. Read as zero.	R
29	ISP	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
28	Reserved	Writing has no effect. Read as zero.	R
27:25	TCU	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
24	Reserved	Writing has no effect. Read as zero.	R
23	AES	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
22	Reserved	Writing has no effect. Read as zero.	R
21	USB	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
20:19	Reserved	Writing has no effect. Read as zero.	R
18	SADC	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
17:15	GPIO	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
14:11	Reserved	Writing has no effect. Read as zero.	R
10	PDMA	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
9	SSI0	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
8	SSI1	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
7	SFC	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R

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6	IPU	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
5:2	Reserved	Writing has no effect. Read as zero.	R
1	AIC	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
0	Reserved	Writing has no effect. Read as zero.	R

15.3.2.6 Interrupt Controller Source Register (ISR1,0x20)

This register contains all the interrupts' status. A "1" indicates that the corresponding interrupt is pending . A "0" indicates that the interrupt is not pending now. The register is read only.

	ISR1																															Base + 0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	HELIX	PDMAM	I2C0	I2C1	I2C2	Reserved		GMAC	EFUSE	Reserved	DDR	UART0	UART1	Reserved		CPM	HARB0	RADIX	HARB2	Reserved			DMIC	Reserved		MSC0	MSC1	NCU_P	DTRNG	NCU	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect. Read as zero.	R
30	HELIX	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
29	PDMAM	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
28	I2C0	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
27	I2C1	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
26:24	Reserved	Writing has no effect. Read as zero.	R
23	GMAC	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
22	EFUSE	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
21	Reserved	Writing has no effect. Read as zero.	R

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20	DDR	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
19:17	UART	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
16	Reserved	Writing has no effect. Read as zero.	R
15	CPM	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
14	HARB0	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
13	Reserved	Writing has no effect. Read as zero.	R
12	HARB2	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
11:6	Reserved	Writing has no effect. Read as zero.	R
5:4	MSC	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
3	Reserved	Writing has no effect. Read as zero.	R
2	DTRNG	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R
1	Reserved	Writing has no effect. Read as zero.	R
0	RTC	0:The corresponding interrupt source is not pending. 1: The corresponding interrupt source is pending.	R

15.3.2.7 Interrupt Controller Mask Register (IMR1,0x24)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. Its value can be changed either by writing IMSR and IMCR or by writing itself. The masked interrupts are invisible to the processor.

	IMR1																															Base + 0x24
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	HELIX	PDMAM	I2C0	I2C1	I2C2	Reserved		GMAC	EFUSE	Reserved	DDR	UART0	UART1	Reserved		CPM	HARB0	RADIX	HARB2	Reserved			DMIC	Reserved		MSC0	MSC1	NCU_P	DTRNG	NCU	RTC
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Bits	Name	Description	RW
31	Reserved	Writing has no effect. Read as zero.	R
30	HELIX	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
29	PDMAM	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
28	I2C0	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
27	I2C1	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
26:24	Reserved	Writing has no effect. Read as zero.	R
23	GMAC	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
22	EFUSE	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
21	Reserved	Writing has no effect. Read as zero.	R
20	DDR	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
19:17	UART	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
16	Reserved	Writing has no effect. Read as zero.	R
15	CPM	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
14	HARB0	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
13	Reserved	Writing has no effect. Read as zero.	R
12	HARB2	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
11:6	Reserved	Writing has no effect. Read as zero.	R
5:4	MSC	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW
3	Reserved	Writing has no effect. Read as zero.	R
2	DTRNG	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW

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1	Reserved	Writing has no effect. Read as zero.	R
0	RTC	0:The corresponding interrupt is not masked. 1:The corresponding interrupt is masked.	RW

15.3.2.8 Interrupt Controller Mask Set Register (IMSR1,0x28)

This register is used to set bits in the interrupt mask register. This register is write only.

	IMSR1																															Base + 0x28
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	HELIX	PDMAM	I2C0	I2C1	I2C2	Reserved		GMAC	EFUSE	Reserved	DDR	UART0	UART1	Reserved		CPM	HARB0	RADIX	HARB2	Reserved			DMIC	Reserved		MSC0	MSC1	NCU_P	DTRNG	NCU	RTC
RST	0	?	?	?	?	?	0	0	?	?	0	?	?	?	0	0	?	?	?	?	0	0	0	?	0	0	?	?	?	?	?	?

Bits	Name	Description	RW
31	Reserved	Writing has no effect. Read as zero.	R
30	HELIX	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
29	PDMAM	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
28	I2C0	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
27	I2C1	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
26:24	Reserved	Writing has no effect. Read as zero.	R
23	GMAC	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
22	EFUSE	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
21	Reserved	Writing has no effect. Read as zero.	R
20	DDR	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
19:17	UART	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W

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16	Reserved	Writing has no effect. Read as zero.	R
15	CPM	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
14	HARB0	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
13	Reserved	Writing has no effect. Read as zero.	R
12	HARB2	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
11:6	Reserved	Writing has no effect. Read as zero.	R
5:4	MSC	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
3	Reserved	Writing has no effect. Read as zero.	R
2	DTRNG	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W
1	Reserved	Writing has no effect. Read as zero.	R
0	RTC	0:Ignore. 1:Will set the corresponding interrupt mask bit.	W

15.3.2.9 Interrupt Controller Mask Clear Register (IMCR1,0x2C)

This register is used to clear bits in the interrupt mask register. This register is write only.

	IMCR1																															Base + 0x2C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	HELIX	PDMAM	I2C0	I2C1	I2C2	Reserved		GMAC	EFUSE	Reserved	DDR	UART0	UART1	Reserved		CPM	HARB0	RADIX	HARB2	Reserved			DIMC	Reserved		MSC0	MSC1	NCU_P	DTRNG	NCU	RTC
RST	0	?	?	?	?	?	0	0	?	?	0	?	?	?	0	0	?	?	?	?	0	0	0	?	0	0	?	?	?	?	?	?

Bits	Name	Description	RW
31	Reserved	Writing has no effect. Read as zero.	R
30	HELIX	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
29	PDMAM	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W

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28	I2C0	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
27	I2C1	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
26:24	Reserved	Writing has no effect. Read as zero.	R
23	GMAC	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
22	EFUSE	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
21	Reserved	Writing has no effect. Read as zero.	R
20	DDR	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
19:17	UART	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
16	Reserved	Writing has no effect. Read as zero.	R
15	CPM	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
14	HARB0	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
13	Reserved	Writing has no effect. Read as zero.	R
12	HARB2	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
11:6	Reserved	Writing has no effect. Read as zero.	R
5:4	MSC	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
3	Reserved	Writing has no effect. Read as zero.	R
2	DTRNG	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W
1	Reserved	Writing has no effect. Read as zero.	R
0	RTC	0:Ignore. 1:Will clear the corresponding interrupt mask bit.	W

15.3.2.10 Interrupt Controller Pending Register (IPR1,0x30)

This register contains the status of the interrupt sources after masking. This register is read only.

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	IPR1																															Base + 0x30
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	HELIX	PDMAM	I2C0	I2C1	I2C2	Reserved		GMAC	EFUSE	Reserved	DDR	UART0	UART1	Reserved		CPM	HARB0	RADIX	HARB2	Reserved			DMIC	Reserved		MSC0	MSC1	NCU_P	DTRNG	NCU	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect. Read as zero.	R
30	HELIX	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
29	PDMAM	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
28	I2C0	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
27	I2C1	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
26:24	Reserved	Writing has no effect. Read as zero.	R
23	GMAC	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
22	EFUSE	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
21	Reserved	Writing has no effect. Read as zero.	R
20	DDR	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
19:17	UART	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
16	Reserved	Writing has no effect. Read as zero.	R
15	CPM	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
14	HARB0	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
13	Reserved	Writing has no effect. Read as zero.	R
12	HARB2	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R

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11:6	Reserved	Writing has no effect. Read as zero.	R
5:4	MSC	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
3	Reserved	Writing has no effect. Read as zero.	R
2	DTRNG	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R
1	Reserved	Writing has no effect. Read as zero.	R
0	RTC	0:The corresponding interrupt is not active or is masked. 1:The corresponding interrupt is active and is not masked to the processor.	R

15.4 Software Considerations

The interrupt controller is reflecting the status of interrupts sources in the peripheral.

Software should perform the task - determine the interrupt source from in IPRx. In this chip, pending interrupts have two levels in structure. Interrupting module in the system that contains more than one interrupt sources need software to determine how to service it by reading interrupt status registers within it.

In the interrupt handler, the serviced interrupt source needs to be cleared in the interrupting device. In order to make certain the cleared source request status has been reflected at the corresponding IPRx bit, software should wait enough time before exiting interrupt state.

The procedure is described following:

1. Interrupt generated.
2. CPU query interrupt sources, saves the current environment and then goes to interrupt common service routine.
3. Get IPRx.
4. Find the highest priority interrupt and vector it. (The software decides which one has the highest priority)
5. Mask the chosen interrupt by writing the register IMSRx.
6. Enable the system interrupt to allow the interrupt nesting. (software decided)
7. Execute the interrupt handler and unmask it by writing the register IMCRx when exit the handler.
8. CPU restores the saved environment and exits the interrupt state.

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16 Watchdog Timer

16.1 Overview

The watchdog timer is used to resume the processor whenever it is disturbed by malfunctions such as noise and system errors. The watchdog timer can generate the reset signal.

16.2 Features

- Generates WDT reset
- A 16-bit Data register and a 16-bit counter
- Counter clock uses the input clock selected by software
  - PCLK, EXTAL and RTCCLK can be used as the clock for counter
  - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software

16.3 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

16.3.1 Register Memory Map

Table 16-1 Registers Memory Map Base Address

Name	Base	Description
WDT	0x10002000	Address base of WDT

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The WDT is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 16-2 WDT Registers Map

Name	RW	Reset Value	Address offset	Access Size
TDR	RW	0x0000_????	0x00	16
TCER	RW	0x0000_0000	0x04	8
TCNT	RW	0x0000_????	0x08	16
TCSR	RW	0x0000_0000	0x0C	16

16.3.2 Register and Fields Description

16.3.2.1 Watchdog Timer Data Register (TDR,0x00)

The watchdog timer data register TDR is used to store the data to be compared with the content of the watchdog timer up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	TDR																															Base + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

16.3.2.2 Watchdog Enable Register (TCER,0x04)

The TCER is an 8-bit read/write register. It contains the counter enable control bits for watchdog. It is initialized to 0x00 by any reset.

	TCER																															Base + 0x04
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															TCEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	TCEN	Counter enable control.	RW

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		0: Timer stop 1: Timer running	

Note: writing TCEN to be zero can not stop the counter, you must stop it by writing TCU's register TSSR.WDTSS high. That is to say the counter can run when TCEN high and TCU's TSR low, but it can only stop by set TCU's TSR high.

16.3.2.3 Watchdog Timer Counter (TCNT,0x08)

The watchdog timer counter (TCNT) is a 16-bit read/write counter. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDR, the comparison match signal will be generated and a WDT reset is generated. The data can be read out at any time. The counter data can be written at any time. (Default: indeterminate)

	TCNT																															**Base + 0x08**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

16.3.2.4 Watchdog Control Register (TCSR,0x0C)

The TCSR is a 16-bit read/write register. It contains the control bits for WDT. It is initialized to 0x00 by any reset.

	TCSR																															**Base + 0x0C**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:6</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
</table></td><td>RW</td></tr>
</table>

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		0	1	1	Internal clock: CLK/64		
		1	0	0	Internal clock: CLK/256		
		1	0	1	Internal clock: CLK/1024		
		110~111			Reserved		
2	EXT_EN	Select EXTAL as the timer clock input. 1: Enable 0: Disable					RW
1	RTC_EN	Select RTCCLK as the timer clock input. 1: Enable 0: Disable					RW
0	PCK_EN	Select PCLK as the timer clock input. 1: Enable 0: Disable					RW

NOTE: The input clock of timer and the PCLK should keep to the rules as follows:

Input clock of timer: IN_CLK	**Clock generated from the frequency divider (PRESCALE): DIV_CLK**
PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

16.4 Watchdog Timer Function

The following describes steps of using WDT:

1. Setting the PRESCALE of input clock in register TCSR.
2. Set register TDR and TCNT.
3. Select the input clock and enable the input clock in register TCSR.

After initialize the register of timer, we should start the counter as follows:

4. Set TCEN bit in TCER to 1. The counter TCNT begins to count.
5. If TCNT = TDR, a WDT reset will be generated.

NOTES:

1. The input clock and PCLK should follow the rules advanced before.
2. The clock of WDT can be stopped by setting register TSR, and register TSR can only be set by register TSSR or TSCR. The content of register TSR, TSSR and TSCR can be found in TCU spec.

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17 PDMA Controller

17.1 Overview

Programmable DMA controller (PDMAC) is dedicated to smartly transfer data between on-chip peripherals (MSC, AIC, UART, etc.), external memories, and memory-mapped external devices.

17.2 Features

- Support up to 32 independent DMA channels
- Descriptor or No-Descriptor Transfer mode compatible with previous JZ SOC
- Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
- Transfer number of data unit: 1 ~ 2^{24} - 1
- Independent source and destination port width: 8-bit, 16-bit, 32-bit
- Fixed three priorities of channel groups: 0~3: highest; 4~11: mid; 12~31: lowest

17.3 Block Diagram

Figure 17-1 Block Diagram of PDMA

17.4 Register Descriptions

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

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R - Read only
W - Write only
RW - read and write
RCW - read and write, but clear to 0 by read
RSW - read and write, but set to 1 by read
RWC - read and write, clear to 0 by soft write 1, set to 1 by hardware write 1, write 0 has no effect
RWS - read and write, set to 1 by soft write 1, hardware clear to 0, soft write 0 has no effect
RC - read only, and clear to 0 by read
RS - read only, and set to 1 by read
SPEC - special access method, relate to its description

3. Reset Value
1 - Reset to 1
0 - reset to 0
? - Value unknown after reset

17.4.1 Register Memory Map

Table 17-1 Registers Memory Map Base Address

Name	Base	Description
GCR	0x13420000	PDMA global control registers.
Channel n	0x13420000 + n*0x20	PDMA channel n.

NOTES: GCR is Global Control Registers.

The PDMA Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 17-2 DMA Channel Registers Map (n=0~31)

Name	RW	Reset Value	Address offset	Access Size
DSAn	RW	0x????_????	0x00 + n*0x20	32
DTAn	RW	0x????_????	0x04 + n*0x20	32
DTCn	RW	0x00??_????	0x08 + n*0x20	32
DRTn	RW	0x0000_00??	0x0C + n*0x20	32
DCSn	RW	0x????_??00	0x10 + n*0x20	32
DCMn	RW	0x00??_??00	0x14 + n*0x20	32
DDAn	RW	0x????_???0	0x18 + n*0x20	32
DSDn	RW	0x????_????	0x1C + n*0x20	32

NOTES: There is not initial value all DMA Channel Registers, so without initial value to read.

Table 17-3 Global Control Registers Map

Name	RW	Reset Value	Address offset	Access Size
DMAC	RW	0x0000_0000	0x1000	32

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DIRQP	RW	0x0000_0000	0x1004	32
DDB	RWS	0x0000_0000	0x1008	32
DDBS	W	0x0000_0000	0x100C	32
DMACP	RW	0x0000_0000	0x101C	32

17.4.2 Register and Fields Description

17.4.2.1 DMA Source Address (DSAn,0x00,n = 0 ~ 31)

	DSAn																															BASE + 0x00 + (n*0x20)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	SA	Source physical address.	RW

17.4.2.2 DMA Target Address (DTAn,0x04,n = 0 ~ 31)

	DTAn																															BASE + 0x04 + (n*0x20)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	TA	Target physical address.	RW

17.4.2.3 DMA Transfer Count (DTCn,0x08,n = 0 ~ 31)

	DTCn																															BASE + 0x08 + (n*0x20)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TC																							
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Name	Description	RW
31:24	Reserved	Write has no effect, read as zero.	R
23:0	TC	TC records the number of data unit to be transferred. Moreover, when Stride transfer mode is enabled, TC composes of two parts: the lower 16 bits is the number of data unit for sub-block transfer, the higher 8 bits is the number of sub-block. TC automatically counts down to 0 at the end.	RW

17.4.2.4 DMA Request Types (DRTn,0x0C,n = 0 ~ 31)

	DRTn																BASE + 0x0C + (n*0x20)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RT					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?

Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	RT	Transfer request type.	RW

Table 17-4 Transfer Request Types

RT5-0	Description
000000	Reserved.
000001	Reserved.
000010	Reserved.
000011	Reserved.
000100	Reserved.
000101	Reserved.
000110	I2S0 transmit-fifo-empty transfer request.
000111	I2S0 receive-fifo-full transfer request.
001000	Auto-request. (external address → external address)
001001	SADC receive-fifo-full transfer request
001010	Reserved.
001011	Reserved.
001100	Reserved.
001101	Reserved.
001110	Reserved.
001111	Reserved.

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010000	Reserved.
010001	Reserved.
010010	UART1 transmit-fifo-empty transfer request. (external address → UTHR)
010011	UART1 receive-fifo-full transfer request. (URBR → external address)
010100	UART0 transmit-fifo-empty transfer request. (external address → UTHR)
010101	UART0 receive-fifo-full transfer request. (URBR → external address)
010110	SSI0 transmit-fifo-empty transfer request.
010111	SSI0 receive-fifo-full transfer request.
011000	SSI1 transmit-fifo-empty transfer request.
011001	SSI1 receive-fifo-full transfer request.
011010	MSC0 transmit-fifo-empty transfer request.
011011	MSC0 receive-fifo-full transfer request.
011100	MSC1 transmit-fifo-empty transfer request.
011101	MSC1 receive-fifo-full transfer request.
011110	Reserved.
011111	Reserved.
100000	Reserved.
100001	DMIC receive-fifo-full transfer request.
100010	Reserved.
100011	Reserved.
100100	SMB0 transmit-fifo-empty transfer request.
100101	SMB0 receive-fifo-full transfer request.
100110	SMB1 transmit-fifo-empty transfer request.
100111	SMB1 receive-fifo-full transfer request.
101000	Reserved.
101001	Reserved.
101010	Reserved.
101011	Reserved.
101100	Reserved.
101101	Reserved.
101110	DES transmit-fifo-empty transfer request.
101111	DES receive-fifo-full transfer request.
110000 ~ 111111	Reserved.

NOTES:

1 Only auto request can be concurrently set in all channels with different source and target address.

2 For on-chip device DMA request, the corresponding source or target address that map to on-chip device must be set as fixed.

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17.4.2.5 DMA Channel Control/Status (DCSn,0x10,n = 0 ~ 31)

	DCSn																BASE +0x10 + (n*0x20)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDES	DES8	TOC														CDOA								Reserved			AR	TT	HLT	Reserved	CTE
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	NDES	Descriptor or No-Descriptor Transfer Select. 0: Descriptor Transfer; 1: No-descriptor Transfer.	RW
30	DES8	Descriptor 8 Word. 0: 4-word descriptor; 1: 8-word descriptor.	RW
29:16	Reserved	Reserved.	R
15:8	CDOA	Copy of offset address of last completed descriptor from that in DMA command register. (The field is Ignored in No-Descriptor Transfer)	RW
7:5	Reserved	Write has no effect, read as zero.	R
4	AR	Address Error. Hardware set it to 1 and software clear it to 0. 0: no address error; 1: address error occurred.	RWC
3	TT	Transfer Terminate. 0: Descriptor or No-Descriptor DMA transfer does not end 1: No-Link Descriptor or No-Descriptor DMA transfer end	RW
2	HLT	DMA halt. Hardware sets it to 1 when an abnormal case occurs during transfer, then software has to clear it to 0 for re-using the channel later.	RWC
1	Reserved	Reserved.	R
0	CTE	Channel transfer enable: 0: disable; 1: enable.	RW

NOTES:

1. For a working channel, when an address error occurs or an on-going transfer is stopped by software writing 0 to CTE, HLT becomes 1 but TT keeps 0 that denotes an abnormal situation occurs.
2. Software can stop any working channel at any time. However, after setting 0 to CTE, software must read TT, HLT and CTE to ensure the stop behavior has been done for the channel, that is,
   a) TT=0, HALT=0, CTE =1, not halt yet, need polling again
   b) TT=1, HALT=0, CTE=0, the channel just ends its work when software wants to stop it.
   c) TT=0, HALT=1, CTE=0, the channel has been stopped but its transfer not complete yet.

17.4.2.6 DMA Channel Command (DCMn,0x14,n = 0 ~ 31)

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	DCMn																															
																																BASE + 0x14 + (n*0x20)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				SID		DID		SAI	DAI	Reserved		RDIL				SP		DP		Reserved	TSZ			Reserved					STDE	TIE	LINK
RST	0	0	0	0	0	0	0	0	?	?	0	0	?	?	?	?	?	?	?	?	0	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Write has no effect, read as zero	R
27:26	SID	Source identification. Only be used for special channel 0/1. 0: Source is TCSM. 1: Source is BCH (for channel 0) / NEMC (for channel 1) 2: Source is DDR (for channel 1) / Reserved (for channel 0) 3: Reserved.	RW
25:24	DID	Destination identification. Only be used for special channel 0/1. 0: Destination is TCSM. 1: Destination is BCH (for channel 0) / NEMC (for channel 1) 2: Destination is DDR (for channel 1) / Reserved (for channel 0) 3: Reserved.	RW
23	SAI	Source Address Increment. 0: no increment; 1: increment.	RW
22	DAI	Destination Address Increment. 0: no increment; 1: increment.	RW
21:20	Reserved	Write has no effect, read as zero.	R
19:16	RDIL	Recommended data unit size (unit: byte) for triggering device's DMA request when TSZ is autonomy.	RW
15:14	SP	Source port width. 00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved.	RW
13:12	DP	Destination port width. 00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved.	RW
11	Reserved	Write has no effect, read as zero.	R
10:8	TSZ	Transfer Data Size of a data unit. 000: 32-bit; 001: 8-bit; 010: 16-bit; 011: 16-byte; 100: 32-byte; 101: 64-byte; 110: 128-byte; 111: autonomy; Note : When TSZ equal to 3'b111, RDIL is valid.	RW
7:3	Reserved	Write has no effect, read as zero.	R
2	STDE	Stride Disable/Enable. 0: address stride disable; 1: address stride enable.	RW
1	TIE	Transfer Interrupt Enable (TIE). 0: disable interrupt; 1: enable interrupt when TT is set to 1.	RW
0	LINK	Descriptor Link Enable. 0: disable; 1: enable. (the field is ignored in No-Descriptor Transfer mode)	RW

NOTES:

SP and DP are only available for device FIFO or NEMC. But when transfer data between device and DDR memory, must set the port width of DDR side as the same as the device side; however, when

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both source and destination are in DDR memory, both SP and DP must be 32-bit by setting 0.

Table 17-5 Available RDIL

RDIL	Description
0	Reserved
1	Recommended data unit is 1 bytes
2	Recommended data unit is 2 bytes
3	Recommended data unit is 3 bytes
4	Recommended data unit is 4 bytes
5	Recommended data unit is 8 bytes
6	Recommended data unit is 16 bytes
7	Recommended data unit is 32 bytes
8	Recommended data unit is 64 bytes
9	Recommended data unit is 128 bytes
10~15	Reserved

NOTES:

1. if TSZ is autonomy, total bytes to be transferred equal the value of DCTn.TC (so maximum transfer bytes for autonomy are 16MB -1).
2. Programmer must care the detail of the FIFO of the device binding with relative DMA channel to set the correct and best recommended data unit value according to FIFO's data width and depth, refer to following table.

Table 17-6 Detailed description of the FIFO

FIFO form	Best recommended RDIL
8x8bits	4 (half of total entries just accommodate 4 bytes)
8x16bits	5 (half of total entries just accommodate 8 bytes)
32x8bits	6 (half of total entries just accommodate 16 bytes)
16x16bits	6 (half of total entries just accommodate 16 bytes)
64x8bits	7 (half of total entries just accommodate 32 bytes)
64x32bits	9 (half of total entries just accommodate 128 bytes)
128x16bits	9 (half of total entries just accommodate 128 bytes)
128x32bits	9 (because maximum data unit is 128 bytes)

Moreover, programmer must be carefully obey following rules for correctness and best performance concern of DMA transfer:

1. ***auto-request, both source and destination device are DDR memory***. No alignment constraint for address, however, both source port width and destination port width must be set 32bit, and transferred bytes in a bus transaction denoted by TSZ (when TSZ !=7) must not be less than 4. Setting autonomy (TSZ=7) is the best choice for transfer efficiency[*0]
2. ***auto-request, both source and destination device are NEMC***, then
   a) if both source and destination port width are 8bit, no alignment constraint for address, setting

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autonomy (TSZ=7) is the best choice for transfer efficiency.

b) If either source port or destination port width is not 8bit, must not set autonomy to TSZ. The relative source or destination address must be 2-byte (port width is 16bit) or 4-byte (port width is 32bit) aligned. Moreover, the byte number denoted by TSZ must not be less than the least common multiple of the byte number denoted by source port width and destination port width. Larger TSZ means better transfer efficiency.

3. ***auto-request, source device is NEMC while destination device is DDR memory*****,** then
   a) if source port width is 8bit. no alignment constraint for address, setting autonomy (TSZ=7) is the best choice for transfer efficiency.
   b) if source port width is 16bit, source address must be 2-byte aligned and TSZ must be the times of 2-byte (so must not set autonomy to TSZ); no alignment constraint for destination address, larger TSZ means better transfer efficiency.
   c) If source port width is 32bit, source address must be 4-byte aligned and TSZ must be the times of 4-byte (so must not set autonomy to TSZ); no alignment constraint for destination address, larger TSZ means better transfer efficiency.
4. ***auto-request, source device is DDR memory while destination device is NEMC***, then
   a) if destination port width is 8bit, no alignment constraint for address, setting autonomy (TSZ=7) is the best choice for transfer efficiency
   b) if destination port width is 16bit, destination address must be 2-byte aligned and TSZ must be the times of 2-byte (so must not set autonomy to TSZ); no alignment constraint for source address, larger TSZ means better transfer efficiency.
   c) If destination port width is 32bit, destination address must be 4-byte aligned and TSZ must be the times of 4-byte (so must not set autonomy to TSZ); no alignment constraint for source address, larger TSZ means better transfer efficiency.
5. ***external device fifo receive request, destination device is DDR memory***, then no alignment constraint for destination address, and
   a) if non-autonomy (TSZ !=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.
   b) If autonomy (TSZ=7), for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.

6. ***external device fifo receive request, destination device is NEMC***, then
   a) if destination port width is 8bit, no alignment constraint for destination address, and if non-autonomy (TSZ !=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.
      If autonomy (TSZ=7), for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.
   b) If destination port width is 16bit, must not set autonomy to TSZ and destination address must be 2-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not

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exceed the critical value of triggering DMA request[*1] meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.

c) If destination port width is 32bit, must not set autonomy to TSZ and destination address must be 4-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.

7. ***external device fifo transmit request, source device is DDR memory***, then no alignment constraint for source address, and
   a) if destination port width is 8bit, setting autonomy (TSZ=7) is the best choice for transfer efficiency
   b) if destination port width is 16bit, when setting autonomy (TSZ=7), total transferred bytes must be the times of 2-byte, and for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 2-byte; when setting non-autonomy (TSZ!=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 2-byte.
   c) if destination port width is 32bit, when setting autonomy (TSZ=7), total transferred bytes must be the times of 4-byte, and for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 4-byte; when setting non-autonomy (TSZ!=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 4-byte.

8. ***external device fifo transmit request, source device is NEMC***, then
   a) if source port width is 8bit, no alignment constraint for source address, and if non-autonomy (TSZ !=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when destination port width is 16bit or times of 4-byte when destination port width is 32bit.
   If autonomy (TSZ=7), for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when destination port width is 16bit or times of 4-byte when destination port width is 32bit.
   b) If source port width is 16bit, must not set autonomy to TSZ and source address must be 2-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.
   c) If source port width is 32bit, must not set autonomy to TSZ and source address must be 4-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port

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width.

NOTES:

*0 - when TSZ is not autonomy, total bytes to be transferred are bytes represented by TSZ * TC, and each bus transaction can only transfer bytes represented by TSZ, so larger data unit is better for transfer efficiency. But since in practical, in most cases, total bytes to be transferred are not the times of the best data unit, or source and/or destination address violates alignment, thus **setting autonomy for TSZ is recommended** when condition is ok.

*1 - Please refer to relative device's spec for detail information of how to set critical trigger value.

17.4.2.7 DMA Descriptor Address (DDAn,0x18,n = 0 ~ 31)

This register is ignored in No-Descriptor Transfer mode.

	DDAn																															
																	BASE + 0x18 + (n*0x20)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBA																				DOA								Reserved			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0

Bits	Name	Description	RW
31:12	DBA	Descriptor Base Address.	RW
11:4	DOA	Descriptor Offset Address.	RW
3:0	Reserved	Write has no effect, read as zero.	R

17.4.2.8 DMA Stride Difference (DSDn,0x1C,n = 0 ~ 31)

This register is ignored in No-Descriptor Transfer mode.

When address stride transfer mode is enabled in Descriptor mode, after a sub-block's transfer defined in DTCn completes, the source or target stride difference will be added to perform the new sub-block's start address, and the transfer will keep going until the transfer ends which means TC in DTCn reaches 0.

	DSDn																															
																	BASE + 0x1C + (n*0x20)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSD																SSD															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Name	Description	RW
31:16	TSD	Target Stride Difference (next sub-block's start address – current sub-block's end address - 1), value range is -32768 ~ 32767	RW
15:0	SSD	Source Stride Difference (next sub-block's start address – current sub-block's end address - 1), value range is -32768 ~ 32767	RW

17.4.2.9 DMA Control(DMAC,0x1000)

	DMAC																															BASE+0x1000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FMSC	FSSI	FTSSI	FUART	FAIC	Reserved					INTCC					INTCE	Reserved												HLT	AR	CH01	DMAE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	FMSC	0: 0.5-data/clk for MSC on APB;1: 1-data/clk for MSC on APB.	RW
30	FSSI	0: 0.5-data/clk for SSI on APB;1: 1-data/clk for SSI on APB.	RW
29	FTSSI	0: 0.5-data/clk for TSSI on APB;1: 1-data/clk for TSSI on APB.	RW
28	FUART	0: 0.5-data/clk for UART on APB;1: 1-data/clk for UART on APB.	RW
27	FAIC	0: 0.5-data/clk for AIC on APB;1: 1-data/clk for AIC on APB.	RW
26:22	Reserved	Write has no effect, read as zero.	R
21:17	INTCC	Which channel is bound with INTC_IRQ. Only available when INTCE is enabled	RW
16	INTCE	Permit INTC_IRQ to be bound to one of programmable channel. 0: INTC_IRQ is ignored; 1: INTC_IRQ is bound to channel n, n equals to INTCC.	RW
15:4	Reserved	Write has no effect, read as zero.	R
3	HLT	Global halt status, halt occurs in any channel, the bit should be set to 1 by hardware and cleared to 0 by software. 0: no halt occurred 1: halt occurred in one or more channels	RWC
2	AR	Global address error status, address error occurs in any channel, the bit should be set to 1 by hardware and cleared to 0 by software. 0: no address error occurred 1: address error occurred	RWC
1	CH01	Special channel 0 and channel 1 enable. 1 –enable 0 – disable.	RW
0	DMAE	Global DMA enable. 0: disable DMA 1: enable DMA	RW

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NOTES:

1. any of FMSC/FSSI/FTSSI/FUART/FAIC has been set，the corresponding DMA transfer on APB for MSC(MSC1, MSC2), SSI(SSI1), UART0~4, AIC will be in fast mode.
2. DMAE is a global switch, so software must be careful to toggle it from 0 to 1 or 1 to 0. It is **UNPREDICTABLE** to set 0 to DMAE abruptly when some channels are still working.
3. For more detail of CH01, refer to later chapter of special channel 0 and channel 1

17.4.2.10 DMA Interrupt Pending (DIRQP,0x1004)

	DIRQP																															BASE+0x1004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ31	IRQ30	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	IRQn	IRQn denotes pending IRQ to main CPU for corresponding channel. 0: normal DMA transfer is in-progress or the channel is idle 1: an address error occurs (only available for UARTn) or normal DMA transfer done; moreover, if the relative channel is programmable, MCU can only set 1 to it. Hardware can only set 1 to it and main CPU can only set 0 to it.	RW

17.4.2.11 DMA Doorbell (DDB,0x1008)

	DDB																															BASE+0x1008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DBn	DMA Doorbell. Software sets it to 1 and hardware clears it to 0. 0: disable DMA controller to fetch the first descriptor or DMA controller clears it to 0 as soon as it starts to fetch the descriptor 1: Writing 1 to DDS's DBSn bit will set the corresponding DBn bit to 1 and	RWS

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		enable DMA controller to fetch the first descriptor For example, write 0x00000001 to DDS, DB0 bit is set to 1 and enable DMA channel 0 to fetch its first descriptor. Write 0 to DDS, no meaning.	

17.4.2.12 DMA Doorbell Set (DDBS,0x100C)

	DDBS																															BASE+0x100C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBS31	DBS30	DBS29	DBS28	DBS27	DBS26	DBS25	DBS24	DBS23	DBS22	DBS21	DBS20	DBS19	DBS18	DBS17	DBS16	DBS15	DBS14	DBS13	DBS12	DBS11	DBS10	DBS9	DBS8	DBS7	DBS6	DBS5	DBS4	DBS3	DBS2	DBS1	DBS0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DBSn	DMA Doorbell Set for each channel. Read as zero, and when write: 0: ignore 1: Set the corresponding DBn bit to 1	W

17.4.2.13 DMA Channel Programmable (DMACP,0x101C)

	DMACP																															BASE+0x101C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCP31	DCP30	DCP29	DCP28	DCP27	DCP26	DCP25	DCP24	DCP23	DCP22	DCP21	DCP20	DCP19	DCP18	DCP17	DCP16	DCP15	DCP14	DCP13	DCP12	DCP11	DCP10	DCP9	DCP8	DCP7	DCP6	DCP5	DCP4	DCP3	DCP2	DCP1	DCP0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DCPn	Channel programmable enable. 0: compatible with previous JZ SOC; 1: firmware controlled channel	RW

17.5 DMA manipulation

17.5.1 Descriptor Transfer Mode

17.5.1.1 Non-Stride (1-Dimensional) Transfer Mode

To do proper Descriptor DMA transfer in a channel, do following steps:

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1 Check whether the status of DMA controller is available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; and then for expected channel n, ensure that DCSn.AR=0, DCSn.HLT=0, DCSn.TT=0, DTCn=0.
2 guarantee DCSn.NDES=0, and select 4 word or 8 word descriptor by DCSn.DES8.
3 Build descriptor in memory. Write the first descriptor's address in DDAn and the address must be 16Bytes aligned for 4word descriptor and 32Bytes aligned for 8word descriptor, otherwise, the hardware behavior later is **UNPREDICTABLE**. The address includes two parts: Base and Offset address. If the descriptor is linked, the 32-bit address of next descriptor is composed of 20-bit Base address in DDAn and 8-bit Offset address in DESn.CDOA. See Table 17-7 for the detailed descriptor structure.
4 Don't update DRTn manually by software, instead, hardware will manage the request type of descriptor's transfer automatically.
5 Set 1 to the corresponding bit in DDB to initiate descriptor fetch.
6 Set DMAC.DMAE=1 and expected DCSn.CTE=1 to activate channel n.
7 Hardware will automatically clear the corresponding bit in DDB as soon as it starts to fetch the descriptor.
8 Wait for DMA request from peripherals to start channel n's DMA transfer.
9 After DMA transfers described by the current descriptor complete, if current DCMn.LINK =0, then DCSn.TT will be set to 1 immediately. Further, if DCMn.TIE=1, it will issue an interrupt request. However, if DCMn.LINK=1, next descriptor will be automatically fetched to repeat step 8 and 9 but ignore setting DCSn.TT until a final descriptor with settting of DCMn.LINK=0 has been done.
10 When channel n's transfer ends normally (DCSn.TT=1) or abnormally (DCSn.HLT=1), to correctly reuse the channel later, software must close the channel first by setting 0 to DCSn.CTE, and then safely clear DCSn.TT or DCSn.HLT to 0.

Table 17-7 Descriptor Structure

Word	Bit	Name	Function
1st (DES0)	31	Reserved	--
	30	Reserved	--
	29-28	Reserved	--
	27-24	Reserved	--
	23	SAI	Source Address Increment
	22	DAI	Target Address Increment
	21-20	Reserved	--
	19-16	RDIL	Request Detection Interval Length
	15-14	SP	Source port width
	13-12	DP	Target port width
	11	Reserved	--
	10-8	TSZ	Transfer Data Size
	7-3	Reserved	--
	2	STDE	Stride transfer enable
	1	TIE	Transfer Interrupt Enable
	0	LINK	Descriptor Link Enable

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2nd (DES1)	31-0	DSA	Source Address
3rd (DES2)	31-0	DTA	Target Address
4th (DES3)	31-24	DOA	Descriptor Offset address
	23-0	DTC	Transfer Counter
5th (DES4)	31-16	TSD	Target Stride Address
	15-0	SSD	Source Stride Address
6th(DES5)	31-6	Reserved	--
	5-0	DRT	DMA Request Type
7th(DES6)	31-0	Reserved	--
8th(DES7)	31-0	Reserved	--

Figure 17-2 Descriptor Transfer Flow

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17.5.1.2 Stride (2-dimensional) Transfer Mode

Stride transfer mode means total transfer counts are subdivided into dozens of or even hundreds of sub-blocks with same size, and each adjacent two sub-blocks has fixed nonzero address gap between the tail of preceding one and the head of subsequent one.

Figure 17-3 Example for Stride Transfer Mode

Manipulation steps of Stride Transfer Mode are similar to Non-stride Transfer Mode. However, each new sub-block's start address (source or destination) is performed by adding the next adjacent byte address of very completed sub-block's end address to corresponding stride difference.

17.5.2 No-Descriptor Transfer Mode

To do proper No-Descriptor DMA transfer, do following steps:

1. Check whether the status of DMA controller is available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; and then for expected channel n, ensure that DCSn.AR=0, DCSn.HLT=0, DCSn.TT=0, DTCn=0.
2. Forx channel n, initialize DSAn, DTAn, DTCn, DRTn, DCSn, DCMn properly.
3. Set DMAC.DMAE=1 and DCSn.CTE=1 to launch DMA transfer.

For a channel with auto-request (DRTn.RT=0x8), the transfer begins automatically when the DCSn.CTE bit and DMAC.DMAE bit are set to 1. While for a channel with other request types, the transfer does not start until a transfer request is issued and detected.

For any channel n, The DTCn value is decremented by 1 for each successful transaction of a data unit. When the specified number of transfer data unit has been completed (DTCn = 0), the transfer ends normally. Meanwhile if DCMn.TIE=1, corresponding bit of DIRQP will be set to 1 to raise an interrupt request. However, during the transfer, if a DMA address error occurs, the transfer should be suspended, both DCSn.AR and DMAC.AR are set to 1 as well as corresponding bit of DIRQP to raise an interrupt request despite of DCMn.TIE.

Sometimes, for example, an UART parity error occurs for a channel that is transferring data between such UART and another terminal. In the case, both DCSn.HLT and DMAC.HLT are set to 1 and the transfer is suspended. Software should identify halt status by checking such two bits and re-configure DMA to let DMA rerun properly later.

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17.6 DMA Requests

DMA transfer requests are normally generated from either the data transfer source or target, but also they can be issued by on-chip peripherals that are neither the source nor the target. There are two DMA transfer request types: auto-request, and on-chip peripheral request. For any channel n, its transfer request type is determined through DRTn.

17.6.1 Auto Request

When there is no explicit transfer request signal available, for example, memory-to-memory transfer or memory to some on-chip peripherals like GPIO, the auto-request mode allows the DMA to automatically generate a transfer request signal internally. Therefore, when DMA initialization done, once the DMAC.DMAE and DCSn.CTE are set to 1, the transfer begins immediately in channel n which DRTn=0x8.

17.6.2 On-Chip Peripheral Request

In the mode, transfer request signals come from on-chip peripherals or even off-chip devices. When a device issues a peripheral request to its corresponding channel n, the transferred byte number for the request is equals to:

1. byte number determined by the bytes denoted by DCMn.TSZ when DCMn.TSZ != 7
2. byte number determined by the bytes denoted by RDIL when DCMn.TSZ == 7

Be careful that the above number must not exceed the device's expected one otherwise FIFO under-run or over-run may occur. However, if the number is too small than the expected one, DMA's bus efficiency will become worse.

17.7 How to Use Programmable DMA Channel

When system needs to setup one programmable channel for later use of smart data transfer, do following steps:

1. Load elaborate firmware to TCSM, should use physical address 0x13422xxx. Common code fragment of IRQ exception handler must be located at physical address range beginning from 0x13422100.
2. Prepare a DMA channel n using expected transfer mode as description in preceding chapters
3. Must set DCMn.TIE=1 and DMACP.DCPn=1
4. Must ensure DCIRQM.CIRQMn==0
5. Launch the channel n as description in preceding chapters

Now the channel n becomes a working programmable channel. It is the responsibility of local channel IRQ's handler to remove corresponding channel IRQ source by setting 0 to DCSn.TT.

Moreover, if programmer wants to let the channel can be triggered by local soft IRQ, DSIRQM.SIRQMn must be set 0, then at expected moment, the MCU sets 1 to DSIRQP.SIRQn to trigger a soft IRQ. It is the responsibility of this soft IRQ's handler to remove the IRQ by setting 0 to

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DSIRQP.SIRQn.

17.8 Index

Table 17-8 Description of Proprietary Vocabulary

Name	Description
PDMA	Programmable DMA controller

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18 SAR A/D Controller

18.1 Overview

The A/D is CMOS low-power dissipation 10bit touch screen SAR(successive Approximation Register) analog to digital converter. It operates with 3.3V power supply. It is developed as an embedded high resolution ADC targeting to the 40nm CMOS process and has wide application in portable electronic devices, high-end home entertainment center, communication systems and so on.

The SAR A/D controller is dedicated to control A/D to work at two different modes: normal operation mode and repeat sampling. The sampling data can transfer to memory though CPU.

18.2 Features

- 3 Channels
- Resolution: 10-bit
- Integral nonlinearity: ±1 LSB
- Differential nonlinearity: ±2 LSB
- Resolution/speed: up to 1Msps
- Max Clock Frequency: 24MHZ
- Low power dissipation: 1.5mW(worst)
- Support three auxiliary input (Through pin AUX0 to AUX2)
- Pin Description

18.3 Block Diagram

Figure 18-1 Block Diagram of SADC

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18.4 Pins Description

SADC has 3 analog input pin. They are listed and described in.

Table 18-1 SADC Analog Pin

Name	I/O	Description
AUX0	AI	Auxiliary Input
AUX1	AI	Auxiliary Input
AUX2	AI	Auxiliary Input

18.5 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

Register Address = Base + Address offset

1. The registers can be read and written by APB bus
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

18.5.1 Register Memory Map

Table 18-2 Registers Memory Map Base Address

Name	Base	Description
SADC	0x10070000	Address base of SADC

The SAR A/D Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

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Table 18-3 SADC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
ADENA	RW	0x8000	0x0000	16
ADCFG	RW	0x0000_0001	0x0004	32
ADCTRL	RW	0xFF	0x0008	8
ADSTATE	RW	0x00	0x000C	8
ADATA0	RW	0x0000_0000	0x0010	32
ADATA1	RW	0x0000_0000	0x0014	32
ADCLK	RW	0x0004_1000	0x0020	32
ADSTB	RW	0x0000	0x0024	16
ADRETM	RW	0x0000_0000	0x0028	32

18.5.2 Register and Fields Description

18.5.2.1 ADC Enable Register (ADENA,0x0000)

The register ADENA is used to trigger A/D to work.

	ADENA																																
																																	BASE + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																POWRR	Pow_opt_	Reserved				REPTEN	Reserved						AUX2EN	AUX1EN	AUX0EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15	POWER	SADC Power control bit. 1: SADC power down 0: SADC power on When POWER is set from 1 to 0, you should wait at least 2ms to enable SADC.	RW
14	POW_OPT	Power optimize enable 1: enable 0: disable	RW
13:10	Reserved	Writing has no effect. Read as zero.	R
9	REPTEN	Repeat sampling enable	RW
8:3	Reserved	Writing has no effect.	RW

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		Read as zero.	
2	AUX2EN	AUX2 Enable Control.	RW
1	AUX1EN	AUX1 Enable Control.	RW
0	AUX0EN	AUX0 Enable Control.	RW

Note:

When two or more channel enable, the controller will sampling all the enabled channel from low to high.

18.5.2.2 ADC Configure Register (ADCFG,0x0004)

The register ADCFG is used to Sadc's PHY testmode and rst_n to work.

	ADCFG																															BASE + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADC_TRIM																Reserved															ADC_RST
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:16	ADC_TRIM	Connection to SAR_ADC's PHY for control SAR_ADC's PHY saradc_ana_reg, only used in adc testmode. please keep the value to 16'h0.	R
15:1	Reserved	Writing has no effect, read as zero.	RW
0	ADC_RST	Connection to ADC's PHY for control SAR_ADC's PHY saradc_rst_n 0: soft reset valid 1: soft reset unvalid	RW

18.5.2.3 ADC Control Register (ADCTRL,0x0008)

The register ADCTRL is used to control A/D to work.

	ADCTRL																															BASE + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													ARDYM2	ARDYM1	ARDYM0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

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Bits	Name	Description	RW
31:3	Reserved	Writing has no effect. Read as zero.	RW
2	ARDYM2	AUX2 data ready interrupt mask. 0: enabled 1: masked	RW
1	ARDYM1	AUX1 data ready interrupt mask. 0: enabled 1: masked	RW
0	ARDYM0	AUX0 data ready interrupt mask. 0: enabled 1: masked	RW

18.5.2.4 ADC Status Register (ADSTATE,0x000C)

The register ADSTATE is used to keep the status of A/D.

	ADSTATE																															BASE + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													ARDY2	ARDY1	ARDY0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect. Read as zero.	R
2	ARDY2	AUX2 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RW
1	ARDY1	AUX1 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC
0	ARDY0	AUX0 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC

18.5.2.5 ADC AUX Data Register (ADATA0,0x0010)

The read-only ADATA0 is a 32-bit register, it keep the sample data.

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	ADATA0																															BASE + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						ADATA1										Reserved						ADATA0									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect. Read as zero.	R
25:16	ADATAH	Data of AUX1. When write to the register, DATA will be clear to 0.	RW
15:10	Reserved	Writing has no effect. Read as zero.	R
9:0	ADATAL	Data of AUX0. When write to the register, DATA will be clear to 0.	RW

18.5.2.6 ADC AUX Data Register (ADATA1,0x0014)

	ADATA1																															BASE + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						ADATA2									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved	Writing has no effect. Read as zero.	R
9:0	ADATAL	Data of AUX2. When write to the register, DATA will be clear to 0.	RW

The measured voltage V_{AUX} (V_{AUX1} and V_{AUX2}) is as follows:

$$V_{SAD} = \frac{ADATA}{1024} \bullet VREF_ADC$$

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18.5.2.7 ADC Clock Divide Register (ADCLK,0x0020)

The register ADCLK is used to set the A/D's clock dividing number.

	ADCLK																															BASE + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKDIV_MS																CLKDIV_US								CLKDIV							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CLKDIV_MS	Dividing number to get ms clock from ADC clock. ms_clk = us_clk / (CLK_MS +1)	RW
15:8	CLKDIV_US	Dividing number to get us clock from ADC clock. us_clk = adc_clk / (CLKDIV_US+1) 0 ≤CLKDIV_10 ≤127	RW
7:0	CLKDIV	Dividing number to get ADC clock from device clock. The A/D works at the frequency between 20KHz and 200KHz. If CLKDIV = N, Then the freq of adc_clk = dev_clk / (N+1). 0 ≤ N ≤ 255	RW

18.5.2.8 ADC Stable Register (ADSTB,0x0024)

ADC Stable register is used for delay some ADC clock cycle to wait ADC stable when sampling AUX voltage.

	ADSTB																															BASE + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																STABLE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

18.5.2.9 ADC REPEAT TIME Register (ADRETM,0x0028)

ADC REPEAT TIME register is used to set the sampling VBAT delay time when ADENA.REPEN is set to 1, and the repeat sampling wait time is RETTIME multiply clk_ms.

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	ADRETM																																
																																	BASE + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RETIME																																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

18.6 SAR A/D Controller Guide

The following describes steps of using SAR-ADC.

18.6.1 Power Down Mode

1 When initial value of ADENA POWER is 1, the state of SADC is in power down state.

2 When you want to use SADC, you should first set ADENA.POWERON to 0 to power on SADC. And wait for at least 2ms, then you can enable required AUX.

3 When you want to power down SADC to get lower power, you should disable AUX, and then set ADENA.POWER to 1.

18.6.2 AUX Sample Operation

1 Set ADCLK.CLKDIV, ADCLK.CLKDIV_US and ADCLK.CLKDIV_MS to set A/D clock frequency.

2 Set ADENA.AUXn(0-2) to 1 to enable the channel.

3 When ADSTATE.VRDYn(0-2) = 1, you can read the sample data from corresponding ADVDATn(0-2). And the AUXEN will be set to 0 auto.

18.7 Index

Table 18-4 Description of Proprietary Vocabulary

Name	Description
SADC	SAR A/D controller

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19 Real Time Clock

19.1 Overview

The Real-Time Clock (RTC) unit can be operated in either chip main power is on or the main power is down but the RTC power is still on. In this case, the RTC power domain consumes only a few micro watts power.

The RTC contains a real time, alarm logic and the power down and wakeup control logic.

19.2 Features

- Embedded 32768Hz oscillator for 32k clock generation with an external 32k crystal
- RTCLK selectable from the oscillator or from the divided clock of EXCLK, so that 32k crystal can be absent if the hibernating mode is not needed
- 32-bits second counter
- Programmable and adjustable counter to generate accurate 1 Hz clock
- Alarm interrupt, 1Hz interrupt
- Stand alone power supply, work in hibernating mode
- Power down controller
- Alarm wakeup
- External pin wakeup with up to 2s glitch filter

19.3 Block Diagram

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19.4 Pins Description

RTC has 6 signal IO pins and 2 power pin. They are listed and described in.

Pin Names	Pin Loc	IO	IO Cell Char.	Pin Description	Power
RTCLK		AI	32768Hz	RTCLK: 32768 clock input or OSC input	VDDRTC33
XRTCLK		AO		XRTCLK: OSC output	VDDRTC33
PWRON		O		PWRON: Power on/off control of main power	VDDRTC33
WKUP_		I	Schmitt	WKUP_: Wake signal after main power down	VDDRTC33
PPRST_		I	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDDRTC33
VDDRTC33		P		VDDRTC33: 3.3V power for RTC and hibernating mode controlling that never power down (normally you can use 1.8V instead to reduce power consumption)	-
VDDRTC11		P		VDDRTC11: 1.1V power for RTC core that never power down	-

RTCLK pin. need input 32.768KHz rtc clock. If do not use any clock, hibernate mode will be NOT available any more, and the time will lose if power down.

PWRON pin: this pin is used to control the main power on/off. Output high voltage means on and low voltage means off.

WKUP_ pin: hibernating mode wakeup input. (low active)

PPRST_ pin: This pin should be set to low voltage only in two cases.

- When RTC power is turned on. (so that whole chip is power on)
- A RESET-KEY is pressed.

19.5 Registers Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. The registers can be read and written by APB bus
3. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by write 1, write 0 has no effect

   RWS - read and write, set to 1 by write 1, write 0 has no effect

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RC - read only, and clear to 0 by read

RS - read only, and set to 1 by read

SPEC - special access method, relate to its description

4. Reset Value

1 - reset to 1

0 - reset to 0

? - value unknown after reset

19.5.1 Register Memory Map

Table 19-1 Registers Memory Map Base Address

Name	Base	Description
RTC	0x10003000	Address base of RTC

The Real Time Clock is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 19-2 Real Time Clock Registers Map

Name	RW	Reset Value	Address offset	Access Size
RTCCR	RW	0x0000_00??*[1]*[2]	0x0000	32
RTCSR	RW	0x????_????	0x0004	32
RTCSAR	RW	0x????_????	0x0008	32
RTCGR	RW	0x0???_????	0x000C	32

NOTES:

1 *[1]: Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

2 *[2]: The reset value can be either of 0x00000081, 0x00000091, 0x00000089, 0x00000099.

Table 19-3 Registers for hibernating mode

Name	RW	Reset Value	Address offset	Access Size
HCR	RW	0x0000_0000*[1]	0x0020	32
HWFCR	RW	0x0000_???0	0x0024	32
HRCR	RW	0x0000_0800	0x0028	32
HWCR	RW	0x2D52_D2D0*[1]	0x002C	32
HWRSR	RW	0x0000_0???*[1]	0x0030	32
HSPR	RW	0x????_????	0x0034	32
WENR	RW	0x0000_0000	0x003C	32
WKUPPINCR	RW	0x0001_0064	0x0048	32

NOTE:

*[1]: Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

All these registers, include those for real time clock and for hibernating mode control, except otherwise stated, are implemented in RTCLK clock domain. When write to these registers, it needs about 1 ~ 2

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RTCLK cycles to actually change the register's value and needs another RTCLK cycle to allow the next write access. A bit RTCCR.WRDY is used to indicate it. When RCR.WRDY is 1, it means the previous write is finished, a right value can be read from the target register, and a new write access can be issued. So before any write access, please make sure RCR.WRDY = 1.

19.5.2 Register and Fields Description

19.5.2.1 RTC Control Register (RTCCR, 0x0000)

RTCCR contains bits to configure the real time clock features. Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

	RTCCR																															BASE + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								WRDY	1HZ	1HZIE	AF	AIE	AE	SELEXC	RTCE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1*[1]	0	0*[1]	?	0	?	0*[1]	1

NOTE:

*[1]: These bits are reset in all resets: PPRST_ input pin reset, hibernating reset and WDT reset.

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	WRDY	Write ready flag. It is 0 when a write is currently processing and the value has not been written to the writing target register. No write to any RTC registers can be issued in this case, or the result is undefined. The read value from the target register is also undefined. The reading is meaningful and another write can be issued when it is 1. This bit is read only and write to it is ignored.	R
6	1HZ	1Hz flag. This bit is set by hardware once every 1 second through the 1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored.	RW
5	1HZIE	1Hz interrupt enable. Writing to this bit takes effect immediately without delay. 1HZIE — Description 0 — 1Hz interrupt is disabled. 1 — 1Hz interrupt is enabled. RTC issues interrupt when 1HZ bit is set.	RW
4	AF	Alarm flag. This bit is set by hardware when alarm match (RTCSR = RTCSAR) is found and alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored. Writing to this bit takes effect	RW

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<table>
<tr><td></td><td></td><td>immediately.</td><td></td></tr>
<tr><td>3</td><td>AIE</td><td>Alarm interrupt enable.
<table>
<tr><th>AIE</th><th>Description</th></tr>
<tr><td>0</td><td>Alarm interrupt is disabled.</td></tr>
<tr><td>1</td><td>Alarm interrupt is enabled. RTC issues interrupt when AF is set.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>AE</td><td>Alarm enable.
<table>
<tr><th>AE</th><th>Description</th></tr>
<tr><td>0</td><td>Alarm function is disabled.</td></tr>
<tr><td>1</td><td>Alarm function is enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>1</td><td>SELEXC</td><td>The divided EXCLK is selected as RTCLK in rtc-hiber module.
<table>
<tr><th>SELEXC</th><th>Description</th></tr>
<tr><td>0</td><td>OSC32K or RTCLK input clock is selected as RTCLK in rtc-hiber module.</td></tr>
<tr><td>1</td><td>The divided EXCLK is selected as RTCLK in rtc -hiber module.</td></tr>
</table>
NOTE: If do not use any 32Khz clock (either input clock or using crystal), hibernate mode will be NOT available any more, and the time will lose if power down.
CPM.OPCR.ERCS must be 0, when using SELEXC = 1.
When the main chip power down, SELEXC will be 0 in internal circuit, in this time, RTCLK will use OSC32K clock.</td><td>RW</td></tr>
<tr><td>0</td><td>RTCE</td><td>Real time clock enable.
<table>
<tr><th>RTCE</th><th>Description</th></tr>
<tr><td>0</td><td>Real time clock function is disabled.</td></tr>
<tr><td>1</td><td>Real time clock function is enabled.</td></tr>
</table></td><td>RW</td></tr>
</table>

19.5.2.2 RTC Second Register (RTCSR, 0x0004)

RTCSR is a 32-bit width second counter. It can be read and write by software. It is increased by 1 at every 1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). When read, it should be read continued more than once and take the value if the adjacent results are the same. RTCSR is not initialized by any reset.

	RTCSR																															BASE + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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19.5.2.3 RTC Second Alarm Register (RTCSAR, 0x0008)

RTCSAR serves as a second alarm register. Alarm flag (RTCCR.AF) is set to 1 when the RTCSR equals the RTCSAR in the condition of alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). RTCSAR can be read and write by software and is not initialized by any reset.

	RTCSAR																															BASE + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSAR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

19.5.2.4 RTC Regulator Register (RTCGR, 0x000C)

RTCGR is serves as the real time clock regulator, which is used to adjust the interval of the 1Hz pulse.

	RTCGR																															BASE + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LOCK	Reserved					ADJC										NC1HZ															
RST	0*[1]	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

NOTE:

*[1]: This bit is reset in all resets: PPRST_ input pin reset, hibernating reset and WDT reset.

Bits	Name	Description	RW
31	LOCK	Lock bit. This bit is used to safeguard the validity of the data written into the RTCGR register. Once it is set, write to RTCGR is ignored. This bit can only be set by software and cleared by (any type of) resets. **LOCK** / **Description** 0: Write to RTCGR is allowed. 1: Write to RTCGR is forbidden.	RW
30:26	Reserved	Writing has no effect. Read as zero.	R
25:16	ADJC	This field specifies how many times it needs to add one 32kHz cycle for the 1Hz pulse interval in every 1024 1Hz pulses. In other words, among every 1024 1Hz pulses, ADJC number of them are trigged in	RW

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		every (NC1HZ + 2) 32kHz clock cycles, (1024 – ADJC) number of them are trigged in every (NC1HZ + 1) 32kHz clock cycles.	
15:0	NC1HZ	This field specifies the number plus 1 of the working 32kHz clock cycles are contained in the 1Hz pulse interval. In other words, 1Hz pulse is trigged every (NC1HZ + 1) 32kHz clock cycles, if RTCGR.ADJC = 0.	RW

19.5.2.5 Hibernate Control Register (HCR, 0x0020)

HCR contains the bit to control the main chip power on/off. Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset.

	HCR																															BASE + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															PD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	PD	Power down or power on bit. Besides writing by CPU, this bit will be set to 1 if an unknown reason main power supply off is detected. This bit controls the PWRON pin level. When co-working with some external components, this bit is used for power management of this chip. It is supposed when 1 is written to this bit, the main power supply of the chip, except RTC power, will be shut down immediately. After this bit is set to 1, all registers in RTC module, except RTCCR.1HZ and RTCCR.1HZIE, cannot be changed by write access. This bit is cleared by reset pin reset and hibernating reset. The later one is asserted by wakeup procedure. **PD** / **PWRON** / **Description** 0 / VDDRTC33 / No power down, keep power on. 1 / 0 V / Power down enable, turn power off.	RW

19.5.2.6 HIBERNATE mode Wakeup Filter Counter Register (HWFCR, 0x0024)

The HIBERNATE mode Wakeup Filter Counter Register (HWFCR) is a 32-bit read/write register .It filter the glitch generated by a dedicated wakeup pin. The HWFCR is not initialized by any reset.

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	HWFCR																															BASE + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HWFCR											Reserved				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:5	HWFCR	Wakeup pin effective minimum time in number of 32 RTCLK cycles, used as glitch filter logic. Maximum of 2 seconds if the RTCLK is 32768Hz If this value is configured to 0, and the WKUP pin keeps low longer than 15 RTCLK periods, it will wakes up RTC from Hibernate. The glitch filter time equals to HWFCR*32 RTCLK period.	RW
4:0	Reserved	Writing has no effect, read as zero.	R

19.5.2.7 Hibernate Reset Counter Register (HRCR, 0x0028)

The Hibernate Reset Counter Register is a 32-bit read/write register that specifies hibernate reset assertion time. The HRCR is initialized by PPRST_ .

	HRCR																															BASE + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	HRCR				Reserved										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:15	Reserved	Writing has no effect, read as zero.	R
14:11	HRCR	HIBERNATE Reset asserting time. Number of 2048 RTCLK cycles. Default value 0x1, assert 125 ms. Maximum 1 second if the RTCLK is 32768Hz. If this value is configured to 0, it will generate 2048 RTCLK HIBERNATE Reset, about 62.5 milliseconds.	RW
10:0	Reserved	Writing has no effect, read as zero.	R

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19.5.2.8 HIBERNATE Wakeup Control Register (HWCR, 0x002C)

The HIBERNATE Wakeup Control Register is a 32-bit read/write register that controls real time clock alarm wake up enable. The reset value only for PPRST_ .

	HWCR																															BASE + 0x002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															EALM
RST	0	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	0	0*[1]

NOTE:

*[1]: This bit is reset in PPRST_ input pin reset and hibernating reset .

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	EALM	RTC Alarm wakeup enable. 0: disable 1: enable	RW

19.5.2.9 HIBERNATE Wakeup Status Register (HWRSR, 0x0030)

The HIBERNATE Wakeup Status Register is a 32-bit read/write register that reflects wakeup status bits.

	HWRSR																															BASE + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							APD	Reserved		HR	PPR	Reserved		PIN	ALM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	1*[2]	1*[1]	0	0	?	?

NOTES:

*[1]: This reset value only for PPRST_. It is undefined in case of other resets.

*[2]: This reset value only for HRST_. It is undefined in case of other resets.

Bits	Name	Description	RW
31:9	Reserved	Writing has no effect, read as zero.	R
8	APD	Accident power down. When the software has not set to HIBERNATE state, the core power is down, then an accident power down is detected. APD is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored.	RW

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		HR — **Description** 0 — Accident power down has not occurred since the last time the software clears this bit. 1 — Accident power down has occurred since the last time the software clears this bit.	
7:6	Reserved	Writing has no effect, read as zero.	R
5	HR	Hibernate Reset. When a Hibernate reset detected, HR is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored. **HR** — **Description** 0 — Hibernate reset has not occurred since the last time the software clears this bit. 1 — Hibernate reset has occurred since the last time the software clears this bit.	RW
4	PPR	PAD PIN Reset. When a PPRST_ is detected, PPR is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored. **PPR** — **Description** 0 — PPRST_ reset has not occurred since last time the software clears this bit. 1 — PPRST_ reset has occurred since last time the software clears this bit.	RW
3:2	Reserved	Writing has no effect, read as zero.	R
1	PIN	Wakeup Pin Status bit. The bit is cleared when chip enters hibernating mode. It is set when exit the hibernating mode by wakeup pin. This bit can only be written with 0. Write with 1 is ignored.	RW
0	ALM	RTC Alarm Status bit. The bit is cleared when chip enters hibernating mode. It is set when exit the hibernating mode by alarm. This bit can only be written with 0. Write with 1 is ignored.	RW

19.5.2.10 Hibernate Scratch Pattern Register (HSPR, 0x0034)

This is a scratch register used to hold a pattern. The software can check the pattern is kept to know whether RTC power has ever been down and whether it is needed to setup the real time clock.

	HSPR																															BASE + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Name	Description	RW
31:0	PAT	The pattern.	RW

19.5.2.11 Write Enable Pattern Register (WENR, 0x003C)

This is a write protect register to may the rtc registers can write only in certain condition.

	WENR																																BASE + 0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WEN	Reserved															WENPAT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WEN	The write enable flag. If the WENPAT is 0xA55A then this bit will be 1. When the WEN changes to 1, the RTCCR, RTCSR, RTCSAR, RTCGR, HCR, HWFCR, HRCR, HWCR, HWRSR, HSPR registers could be changed. But RTCCR.SELEXC, RTCCR.HZIE, RTCCR.WRDY may change in any time. This bit is read only and write to it is ignored. This bit only reset by PPRST_ and HRST_. There is an exception, when system does NOT have RTC 32Khz crystal. MUST write 1 to RTCCR.SELEXC before write to any value to any other registers. <table><tr><th>WEN</th><th>Description</th></tr><tr><td>0</td><td>Other RTC registers is locked, write these registers will be ignored.</td></tr><tr><td>1</td><td>Other RTC registers can be changed.</td></tr></table>	R
30:16	Reserved	Writing has no effect, read as zero.	R
15:0	WENPAT	The write enable pattern. Before writing any value to RTCCR, RTCSR, RTCSAR, RTCGR, HCR, HWFCR, HRCR, HWCR, HWRSR, HSPR registers, write 0xA55A to WENPAT to set these register writable. If this value is ok, WEN will change to 1. But RTCCR.SELEXC and RTCCR.HZIE are writable in any time. These bits are write-only, always read as 0.	W

19.5.2.12 WKUP_PIN_RST control register (WKUPPINCR, 0x0048)

This is a register used to control the enable and set the judge time to reset the chip when extend press

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the WKUP pin. The are only initialized by PPRST_ and HRST_.

	WKUPPINCR																															BASE + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													VOL_SEL	OSC_BYP	OSC_EN	Reserved								P_JUD_LEN				P_RST_EN			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	VOL_SEL	Oscillate voltage select 1: Select 1.8V 0: Select 2.5V or higher.	RW
17	OSC_BYP	Oscillate bypass 1: Enable 0: Disable	RW
16	OSC_EN	Oscillate enable 1: Enable 0: Disable	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:4	P_JUD_LEN	WKUP up pin extend press length judge value The judge time equals to FLT_LEN multiply RTC 1HZ period, and only the active press length equal or greater than judge time, the chip reset can assert.	RW
3: 0	P_RST_EN	Enable extend press WKUP pin to reset chip others: disable 4'hB: enable	RW

19.6 Operation Flow

19.6.1 Registers Access

19.6.1.1 Registers Read

All registers can read directly, but the RTCSR and RTCSAR should be read continued more than once and take the value if the adjacent results are the same. Please check and make sure RTCCR.WRDY equals to 1 before execute a register read.

19.6.1.2 Registers Write

Only the RTCCR.SELEXC, RTCCR.HZIE, RTCGR.LOCK, WENR.WENPAT bits can write directly.

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Others bits need following the below procedure

1) Check RTCCR.WRDY, make sure it equals to 1
2) Write 0xa55a to WENR register to enable other registers write.
3) Waiting WENR.WEN change to 1
4) Check RTCCR.WRDY, make sure it equals to 1
5) Write the target register
6) Waiting RTCCR.WRDY equals to 1 to make sure the current write processing was finished.

19.6.2 Power On Timing Diagram

The RTC power on procedure like Figure 19-1.

Figure 19-1 Core Power On

19.6.3 HIBERNATE Mode

The purpose of hibernate mode is to save the power. When in hibernate mode, CORE will no power consumption.

If you want to use hibernate mode, please first make sure RTCCR.SELEXC is 0.
When Software writes 1 to PD bit of HCR, the system at once enters HIBERNATE mode. The powers of CORE and IO are disconnected by PWRON pin, no power consumption in core and IO. When a wakeup event occurs, the core enters normal mode through a hibernate reset.

19.6.3.1 Procedure to Enter HIBERNATE mode

Before enter HIBERNATE mode, software must complete following steps:

1 Finish the current operation and preserve all data to flash.
2 Configure the wake-up sources properly by configure HWCR.
3 Set HIBERNATE MODE. (Set PD bit in HCR to 1)

19.6.3.2 Procedure to Wake-up from HIBERNATE mode

1 The internal hibernate reset signal will be asserted if one of the wake-up sources is issued.
2 Check RSR to determine what caused the reset.

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3 Check PIN/ALM bits of HWRSR in order to know whether or not the power-up is caused by which wake-up from HIBERNATE mode.
4 Configure the SDRAM memory controller.
5 Recover the data from flash.

19.6.4 Time Regulation

Because of the inherent inaccuracy of crystal and other variables, the time counter may be inaccurate. This requires a slight adjustment. The application processor, through the RTCGR, lets you adjust the 1Hz time base to an error of less than 1ppm. Such that if the Hz clock were set to be 1Hz, there would be an error of less than 5 seconds per month.

To determine the value programmed into the RTCGR, you must first measure the output frequency at the oscillator multiplex (approximately 32 kHz) using an accurate time base, such as a frequency counter. This clock is externally visible by selecting the alternate function of GPIO.
To gain access to the clock, program this pin as an output and then switch to the alternate function. To trim the clock, divide the output of the oscillator by an integer value and fractional adjust it by periodically deleting clocks from the stream driving this integer divider.

After the true frequency of the oscillator is known, it must be split into integer and fractional portions. The integer portion of the value (minus one) is loaded into the NC1HZ field of the RTCGR.

The fractional part of the adjustment is done by periodically deleting clocks from the clock stream driving the Hz divider. The trim interval period is hardwired to be 1024 1Hz clock cycles (approximately 17 minutes). The number of clocks (represented by ADJC field of RTCGR) are deleted from the input clock stream per trim interval. If ADJC is programmed to be zero, then no trim operations occur and the RTC is clocked with the raw 32 kHz clock. The relationship between the Hz clock frequency and the nominal 32 kHz clock (f1 and f32K, respectively) is shown in the following equation.

$$f1 = \frac{2^{10} \times (NC1HZ + 1)}{2^{10} \times (NC1HZ + 1) + ADJC} \times \frac{f32k}{NC1HZ + 1}$$

f1 = actual frequency of 1Hz clock
f32k = frequency of either 32.768KHz crystal output or 3.6864MHz crystal output further divided down to 32.914KHz

19.6.5 Clock select

There could be two clock input to RTC internal clock called rtclk. One is OSC32k clock; the other is EXCLK/512.
The software MUST make sure the RTC run in valid clock configuration.

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Table 19-4 Clock select registers

RTCCR.SELEXC	CPM.ERCS	Description	Valid
0	0	RTC use OSC32K clock.	OK
0	1		OK
1	0	RTC use EXCLK/512 clock.	OK
1	1	RTC will lost clock. (Not Valid)	NO

Figure 19-2 RTC clock selection path

Changing RTCLK sequence:

1. There are both 32KHz crystal and 24Mhz EXCLK crystal connected, so RTCLK input path has 32Khz clock.

   In this case, there is no need to change internal clock, so do NOT change SELEXC all the time.

2. There is no 32KHz crystal connected but only 24Mhz EXCLK crystal connected, so RTCLK input path has no clock.

   In this case, should flow the sequence below to change internal clock:

   a Set OPCR.ERCS of CPM to 1; close EXCLK/512 to RTC.
   b Set CLKGR.RTC of CPM to 0; open PCLK to RTC.
   c Set RTCCR.SELEXC to 1; change internal clock to EXCLK/512.
   d Wait two clock period of clock.
   e Clear OPCR.ERCS of CPM to 0; open EXCLK/512 to RTC.
   f Configure all RTC registers but RTCCR.SELEXC.
   g Check RTCCR.SELEXC == 1.
   h IF YES, finish this sequence; IF NO, do step (a) again.

NOTE: If using HIBERNATE mode, MUST have both 32KHz crystal (or input 32Khz clock) and 24Mhz EXCLK crystal connected, or RTC time will be insignificant.

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20 EFUSE Slave Interface (EFUSE)

20.1 Overview

The EFUSE is a parallel-in/parallel-out Electrical Fuse Macro which has 1024bits internal nonvolatile one-time programmable EFUSE storage.

The EFUSE is provided 1024 programmable bit, Total 1024 bits are separated into eighteen segments as below table.

Segment	1	2	3	4	5	6	7	8
Bits	96	32	16	8	8	16	16	832

Each segment function as below declare:
Segment 1: Ingenic CHIP ID
Segment 2: User ID
Segment 3: SARADC Calibration data
Segment 4: Trim data
Segment 5: Programming protect
Segment 6: Ingenic CPUID
Segment 7: Special Use
Segment 8: Customer reserved

Each segment can be programmed separately.
Each segment has a protect bit, which has higher priority than program segment selection.

Programming frequency is wide, and programming time can adjust use the EFUSE register.

Initial value of EFUSE is 0, when programmed to 1, it doesn't able to program back to 0 anymore.
Do not attempt to program any bit that already programmed to 1, such action will result unpredictable status to whole EFUSE block.

Programming voltage supply pin VDDQ:

- In program mode, supply VDDQ with 1.5V.
  Maximum accumulative time for VDDQ pin exposed under 1.5V+/-10% should be less than 100 millisecond.
- In read mode, leave VDDQ to 0V.

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20.2 Registers Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

20.2.1 Registers Memory Map

Table 20-1 Registers Memory Map Base Address

Name	Base	Description
EFUSE	0x13540000	Address base of EFUSE

The EFUSE Slave Interface is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 20-2 EFUSE Register Map

Name	RW	Reset Value	Address Offset	Access Size
EFUCTRL	RW	0x0080_0000	0x0000	32
EFUCFG	RW	0x0000_0000	0x0004	32
EFUSTATE	RW	0x0000_??01	0x0008	32
EFUDATA	RW	0x0000_0000	0x000C	32

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20.2.2 Registers and Fields Description

20.2.2.1 EFUSE Control Register (EFUCTRL, 0x0000)

	EFUCTRL																													BASE + 0x0000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						Address					Reserved					PG_EN	Reserved													WR_EN	RD_EN
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Please keep these bits at reset value.	R
25:21	Address	Indicate the start address wants to program or read Aligned to Byte	RW
20:16	Reserved	Writing has no effect, read as zero.	RW
15	PG_EN	Programming EFUSE enable 1: Enable 0: Disable	RW
14:2	Reserved	Writing has no effect, read as zero.	RW
1	WR_EN	Write data to EFUSE data buffer enable 1: Enable 0: Disable This bit will change to 0 automatically when write procedure done	RW
0	RD_EN	Read data from EFUSE data buffer enable 1: Enable 0: Disable This bit will change to 0 automatically when read procedure done	RW

20.2.2.2 EFUSE Configure Register (EFUCFG, 0x0004)

	EFUCFG																													BASE + 0x0004	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT_EN	Reserved							RD_ADJ				RD_STROBE				WR_ADJ				Reserved			WR_STROBE								
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31	INT_EN	Interrupt enable when read/write EFUSE done. 1: Enable 0: Disable	RW
30:24	Reserved	Writing has no effect, read as zero.	R
23:20	RD_ADJ	Adjust number of h2clk cycles when EFUSE reading unsigned value, h2clk period multiply (RD_ADJ + 1) should greater than 25 ns.	RW
19:16	RD_STROBE	Adjust number of h2clk cycles when EFUSE reading STROBE Signed value, h2clk period multiply(RD_ADJ +RD_STROBE+1) should greater than 20 ns.	RW
15:12	WR_ADJ	Adjust number of h2clk cycles when EFUSE programming unsigned value, h2clk period multiply (WR_ADJ + 1) should greater than 20 ns.	RW
11:0	WR_STROBE	Adjust number of h2clk cycles when EFUSE programming STROBE Signed value, h2clk period multiply(WR_ADJ + 2000 + WR_STROBE) should between 9.8us and 10.2us, typical 10us	RW

20.2.2.3 EFUSE Status Register (EFUSTATE, 0x0008)

	EFUSTATE																BASE + 0x0008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPUID_PR	TRIM2_PR	INST_PRT	DISJATG	TRIM1_PR	TRIM0_PR	CUT_PRT	CHIPI_PRT	Reserved						WR_DONE	RD_DONE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15	CPUID_PRT	CPU id segment write protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
14	WDT_EN	Watchdog enable 1: enable watchdog function 0: disable watchdog function	R
13	CUST_PRT	Customer segment write protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R

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12	DISJATG	Disable JTAG enable 1: disable JTAG 0: enable JTAG	R
11	TRIM_PRT	Trim segment write protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
10	SADC_PRT	Sadc calibration segment write protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
9	USERID_PRT	User ID segment write protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
8	CHIPID_PRT	CHIP ID segment protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
7:2	Reserved	Writing has no effect, read as zero.	RW
1	WR_DONE	Write data to EFUSE operate done flag 1: done 0: not done *This bit only can write to 0, and write to 0 will clear this flag.	RW
0	RD_DONE	Read EFUSE data operate done flag 1: done 0: not done *This bit only can write to 0, and write to 0 will clear this flag	RW

20.2.2.4 EFUSE Data Register (EFUDATA, 0x000C)

	EFUDATA																															BASE + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	DATA	EFUSE DATA register.	RW

NOTE:

1. The EFUSE 1024 bits are mapped to chip memory address, from 0x13540200 to 0x1354027F.
2. The EFUSE 1024 programmable bits are separated into eighteen segments as below table. The first

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Segment used to store Ingenic chip id, second segment used to store user id, third segment used to store sadc calibration data, fourth segment used to store trim data, fifth segment store segment protect bit, sixth segment store cpu id, seventh segment reserved for ingenic special use, the last segment reserved for customer use.

Segment	1	2	3	4	5	6	7	8
Mapped Address (Byte)	200 | 20B	20C | 20F	210 | 211	212 | 212	213 | 213	214 | 215	216 | 217	218 | 27F
Aligned To Word	00 | 02	03 | 03	04 | 04	04 | 04	04 | 04	05 | 05	05 | 05	06 | 1F
Bits	96	32	16	8	8	16	16	832

3. The protect bit segment store others segment write protect bit, if protect bit programmed to 1, corresponding segment can not be able to program. The protect bit map as below table.

	Bit	Mapped To EFUSE Status Register
The Protect bit Segment	7	CPUID_PRT
	6	WDT_EN
	5	CUST_PRT
	4	DISJTAG
	3	TRIM_PRT
	2	SADC_PRT
	1	USERID_PRT
	0	CHIPID_PRT

4. The EFUSE can program one word at each time.
5. The EFUSE space aligned to word, directly mapped to EFUDATA register when reading and programming. In program operate, the EFUDATA bit '1' will programming into efuse, and the bit '0' will ignore.

20.3 Flow

20.3.1 Program EFUSE Flow

1. Set EFUCFG register(reading and programming timing).
2. Write want program data to EFUDATA register.
3. Set control register, indicate want to program address.
4. Write control register PG_EN bit to 1
5. Connect VDDQ pin to 2.5V
6. Write control register WR_EN bit to 1
7. Wait status register WR_DONE set to 1.

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8. Disconnect VDDQ pin from 2.5V.
9. Write control register PG_EN bit to 0.

NOTE:

*[1]: Do NOT pre-charge VDDQ too early before EFUSE program started.

The maximum 2.5V supply time to VDDQ must be strictly controlled less than 1sec.

Use on-chip counter and GPIO to coordinate external supply source.

20.3.2 Read EFUSE Flow

1. Set EFUCFG register(reading and programming timing).
2. Set control register to indicate what to read data address.
3. Set read enable register.
4. Wait status register RD_DONE set to 1 or EFUSE interrupted, software application can read EFUDATA register.

NOTE:

*[1]: EFSUE controller will read EFUSE protect bit segment, CPUID segment and Special segment automatically when chip reset, and update the EFUSE state register.

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Section 6

PERIPHERALS

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21 General-Purpose I/O Ports(GPIO)

21.1 Overview

General Purpose I/O Ports (GPIO) is used in generating and capturing application-specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As input, pull up/down can be enabled/disabled for the port and the port also can be configured as level or edge tripped interrupt source.

21.2 Features

- Each port can be configured as an input, an output or an alternate function port.
- Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering, and every interrupt source can be masked independently.
- Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled.
- GPIO output 4 interrupts, each group had an interrupt to INTC(Interrupt Controller).

21.3 About GPIO Port Summary Table

1) In the GPIO port summary, different pad type will determine different pad characteristics. such as the types of SRP_BI_SDS_33V_STB and STP_BI_016_1833V_SD3, it just have pull up/down/hiZ enable , schmitt trigger enable,drive strength ,slew rate, power-on-start and receiver enabel control port.
2) Each Pad can configured as four module function.
3) GROUP A PA30 it's not GPIO port, but in X1830 it will used with RTC to realize wakeup operate.

Table 21-1 GPIO port summary table illustration

PAD_ID	PAD_TYPE	PULL_RST	SMT_RST	DS_RST	FUNC0	FUNC1	FUNC2	FUNC3
PA00	TYPEA	HIZ	1	2mA	sd0(io-0)	msc0_d0(io-0)	(i-0)	(i-0)
PA01	TYPEB	PU	0	4mA	sd2(io-0)	msc0_d1(io-0)	ssi0_dt(io-0)	sfc_dt(io-0)
PA02	TYPEA	PD	1	8mA	sd2(io-0)	msc0_d2(io-0)	ssi0_dr(io-0)	sfc_dr(io-0)
Group number	Instance pad type name (different type will decide GPIO function)	Pad pull enable active value. 00: HIZ 01: pull up(PU) 10: pull down(PD) 11: repeater	Pad schmitt trigger enable: 1: schmitt trigger enable. 0: schmitt trigger disnable..	Pad Drive Strength control: 00:2mA 01:4mA 10:8mA 11: 12mA	In table, each function column will expression one module port using relationship. such as the pad PA00, the FUNC0 "sd0_(io-0)", "sd0" means the NEMC module data port 0, "io" means function as I/O, "0" means when configure as other functions, GPIO supply value 0 to this function port.			

Note: 1.TYPEA = SRP_BI_SDS_33V_STB; TYPEB=STP_BI_016_1833V_SD3..
2. Feature "PULL_RST" means after reset default pull value.

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21.3.1 GPIO Port A Summary

Table 21-2 GPIO Port A summary

<PAD_ID>	PAD_MNAME	PAD_TYPE	CTRL_TYP	PULL_RST	SMT_RST	DS_RST	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
PA00			C3				(i-0)	(i-0)	(i-0)	(i-0)
PA01			C3				(i-0)	(i-0)	(i-0)	(i-0)
PA02			C3				(i-0)	(i-0)	(i-0)	(i-0)
PA03			C3				(i-0)	(i-0)	(i-0)	(i-0)
PA04			C3				(i-0)	(i-0)	(i-0)	(i-0)
PA05			C3				(i-0)	(i-0)	(i-0)	(i-0)
PA06		TYPEA	C3	HIZ	0	8mA	(i-0)	dvp_d6_i(i-0)	(i-0)	(i-0)
PA07		TYPEA	C3	HIZ	0	8mA	(i-0)	dvp_d7_i(i-0)	(i-0)	(i-0)
PA08		TYPEA	C3	HIZ	0	8mA	(i-0)	dvp_d8_i(i-0)	(i-0)	(i-0)
PA09		TYPEA	C3	HIZ	0	8mA	(i-0)	dvp_d9_i(i-0)	(i-0)	(i-0)
PA10		TYPEA	C3	HIZ	0	8mA	(i-0)	dvp_d10_i(i-0)	(i-0)	(i-0)
PA11		TYPEA	C3	PU	0	8mA	(i-0)	dvp_d11_i(i-0)	(i-0)	(i-0)
PA12		TYPEA	C3	PU	0	8mA	(i-0)	smb0_sda(io-1)	(i-0)	(i-0)
PA13		TYPEA	C3	PU	0	8mA	(i-0)	smb0_sck(io-1)	(i-0)	(i-0)
PA14		TYPEA	C3	HIZ	0	8mA	(i-0)	dvp_pclk_i(i-0)	(i-0)	(i-0)
PA15		TYPEA	C3	HIZ	0	8mA	(i-0)	dvp_mclk_o(o)	(i-0)	(i-0)
PA16		TYPEA	C3	HIZ	0	8mA	(i-0)	dvp_hsync_i(i-0)	(i-0)	(i-0)
PA17		TYPEA	C3	HIZ	0	8mA	(i-0)	dvp_vsync_i(i-0)	(i-0)	(i-0)
PA18	GPIO	TYPEA	C3	HIZ	0	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PA19	GPIO	TYPEA	C3	HIZ	1	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PA20	GPIO	TYPEA	C3	HIZ	1	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PA21			C3				(i-0)	(i-0)	(i-0)	(i-0)
PA22	GPIO	TYPEA	C3	PU	1	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PA23		TYPEA	C3	PU	0	8mA	(i-0)	sfc_dt(io-0)	(i-0)	(i-0)
PA24		TYPEA	C3	PU	0	8mA	(i-0)	sfc_dr(io-0)	(i-0)	(i-0)
PA25		TYPEA	C3	PU	0	8mA	(i-0)	sfc_gpc(io-0)	(i-0)	(i-0)
PA26		TYPEA	C3	PU	0	8mA	(i-0)	sfc_ce1(io-0)	(i-0)	(i-0)
PA27		TYPEA	C3	PU	0	8mA	(i-0)	sfc_clk(io-0)	(i-0)	(i-0)
PA28		TYPEA	C3	PU	0	8mA	(i-0)	sfc_ce0(io-0)	(i-0)	(i-0)
PA29			C3				(i-0)	(i-0)	(i-0)	(i-0)
PA30	wake_up		C3				(i-0)	(i-0)	(i-0)	(i-0)
PA31			C3				(i-0)	(i-0)	(i-0)	(i-0)

Note:

1. PA18,PA19,PA20,PA22 just used as GPIO, no function banding in those PAD.
2. GROUP A PA30 binding port WKUP from non-GPIO PAD, it used GPIO's logic to realized wakeup interrupt function with RTC module.
3. TYPEA is equal to MSRP_BI_SDS_33V_STB; PA15's slew rate(SR) is fast mode, other PADs's slew rate is slow mode.
4. Delete PA00-PA05 pins and replace them with INNO-MIPI-PADs.

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21.3.2 GPIO Port B Summary

Table 21-3 GPIO Port B summary

<PAD_ID>	PAD_NAME	PAD_TYPE	CTRL_TYPEP	PULL_RST	SMT_RST	DS_RST	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
PB00		TYPEA	C3	HIZ	0	8mA	msc0_d0(io-1)	(i-0)	sd0(io-0)	(i-0)
PB01		TYPEA	C3	HIZ	0	8mA	msc0_d1(io-1)	(i-0)	sd1(io-0)	(i-0)
PB02		TYPEA	C3	HIZ	0	8mA	msc0_d2(io-1)	(i-0)	sd2(io-0)	(i-0)
PB03		TYPEA	C3	HIZ	0	8mA	msc0_d3(io-1)	(i-0)	sd3(io-0)	(i-0)
PB04		TYPEA	C3	HIZ	0	8mA	msc0_clk_o(o)	(i-0)	sd4(io-0)	(i-0)
PB05		TYPEA	C3	HIZ	0	8mA	msc0_cmd(io-0)	(i-0)	sd5(io-0)	(i-0)
PB06		TYPEA	C3	HIZ	0	8mA	gmac_txclk_i(i-0)	(i-0)	sd6(io-0)	(i-0)
PB07		TYPEA	C3	HIZ	0	8mA	gmac_phy_clk_o(o)	(i-0)	sd7(io-0)	(i-0)
PB08		TYPEA	C3	HIZ	0	8mA	gmac_txen_o(o)	(i-0)	(i-0)	(i-0)
PB09		TYPEA	C3	HIZ	0	8mA	gmac_rxdv_i(i-0)	(i-0)	(i-0)	(i-0)
PB10		TYPEA	C3	PD	0	8mA	gmac_mdck_o(o)	(i-0)	(i-0)	(i-0)
PB11		TYPEA	C3	PU	0	8mA	gmac_mdio(io-0)	(i-0)	(i-0)	(i-0)
PB12			C3							
PB13		TYPEA	C3	HIZ	0	8mA	gmac_txd0_o(o)	(i-0)	sa0_o(o)	(i-0)
PB14		TYPEA	C3	HIZ	0	8mA	gmac_txd1_o(o)	(i-0)	sa1_o(o)	(i-0)
PB15		TYPEA	C3	HIZ	0	8mA	gmac_rxd0_i(i-0)	(i-0)	sa2_o(o)	(i-0)
PB16		TYPEA	C3	HIZ	0	8mA	gmac_rxd1_i(i-0)	(i-0)	(i-0)	(i-0)
PB17		TYPEA	C3	PD	0	8mA	pwm0_o(o)	(i-0)	(i-0)	(i-0)
PB18		TYPEA	C3	PD	0	8mA	pwm1_o(o)	clk32k_out_o(o)	(i-0)	(i-0)
PB19		TYPEA	C3	PU	0	8mA	uart0_rxd_i(i-1)	tdi_i(i-0)	(i-0)	(i-0)
PB20		TYPEA	C3	HIZ	0	8mA	uart0_cts_i(i-1)	(i-0)	(i-0)	(i-0)
PB21		TYPEA	C3	HIZ	0	8mA	uart0_rts_o(o)	(i-0)	(i-0)	(i-0)
PB22		TYPEA	C3	HIZ	0	8mA	uart0_txd_o(o)	tdo_o(o)	(i-0)	(i-0)
PB23		TYPEA	C3	HIZ	0	8mA	uart1_txd_o(o)	tck_i(i-0)	(i-0)	(i-0)
PB24		TYPEA	C3	PU	0	8mA	uart1_rxd_i(i-1)	tms_i(i-0)	cs1_o(o)	(i-0)
PB25		TYPEA	C3	PU	0	8mA	smb1_sda(io-1)	(i-0)	cs2_o(o)	(i-0)
PB26		TYPEA	C3	PU	0	8mA	smb1_sck(io-1)	(i-0)	rd_o(o)	(i-0)
PB27	GPIO	TYPEA	C3	HIZ	1	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PB28	GPIO	TYPEA	C3	HIZ	1	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PB29	GPIO	TYPEA	C3	HIZ	1	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PB30	GPIO	TYPEA	C3	HIZ	1	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PB31	GPIO	TYPEA	C3	PD	0	8mA	(i-0)	(i-0)	(i-0)	(i-0)

Note:

1. PB19,PB22,PB23,PB24 after power reset will stay in the device 1 mode, those PAD used as JTAG when X1830 power reset default.
2. PB27,PB28,PB29,PB30,PB31 just used as GPIO, no function banding in those PAD
3. TYPEA is equal to MSRP_BI_SDS_33V_STB

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21.3.3 GPIO Port C Summary

Table 21-4 GPIO Port C summary

<PAD_I	PAD_MNAME	PAD_TYPE	CTRL_TYPEP	PULL_RST	SMT_RST	DS_RST	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
PC00	BOOT_SEL0	TYPEA	C3	PU	0	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PC01	BOOT_SEL1	TYPEA	C3	PD	0	8mA	(i-0)	(i-0)	(i-0)	(i-0)
PC02		TYPEA	C3	HIZ	0	8mA	msc1_clk_o(o)	(i-0)	(i-0)	(i-0)
PC03		TYPEA	C3	HIZ	0	8mA	msc1_cmd(io-0)	(i-0)	(i-0)	(i-0)
PC04		TYPEA	C3	HIZ	0	8mA	msc1_d0(io-1)	(i-0)	(i-0)	(i-0)
PC05		TYPEA	C3	HIZ	0	8mA	msc1_d1(io-1)	(i-0)	(i-0)	(i-0)
PC06		TYPEA	C3	HIZ	0	8mA	msc1_d2(io-1)	(i-0)	(i-0)	(i-0)
PC07		TYPEA	C3	HIZ	0	8mA	msc1_d3(io-1)	(i-0)	(i-0)	(i-0)
PC08		TYPEA	C3	PD	1	8mA	pwm2_o(o)	flash_storbe_in_i(i-0)	dmic_clk_o(o)	(i-0)
PC09		TYPEA	C3	PD	1	8mA	pwm3_o(o)	flash_out_o(o)	(i-0)	(i-0)
PC10			C3				(i-0)	(i-0)	(i-0)	(i-0)
PC11		TYPEA	C3	HIZ	0	8mA	ssi0_dr_i(i-0)	pwm0_o(o)	(i-0)	(i-0)
PC12		TYPEA	C3	HIZ	0	8mA	ssi0_dt_o(o)	pwm1_o(o)	(i-0)	(i-0)
PC13		TYPEA	C3	HIZ	0	8mA	ssi0_gpc_o(o)	pwm2_o(o)	(i-0)	(i-0)
PC14		TYPEA	C3	HIZ	0	8mA	ssi0_ce1_o(o)	pwm3_o(o)	(i-0)	(i-0)
PC15		TYPEA	C3	HIZ	0	8mA	ssi0_clk_o(o)	pwm4_o(o)	(i-0)	(i-0)
PC16		TYPEA	C3	PU	0	8mA	ssi0_ce0_o(o)	pwm5_o(o)	(i-0)	(i-0)
PC17		TYPEA	C3	HIZ	1	8mA	drv_vbus_o(o)	pwm6_o(o)	(i-0)	(i-0)
PC18		TYPEA	C3	HIZ	1	8mA	i2s_dac_lrck(io-0)	pwm7_o(o)	(i-0)	(i-0)
PC19		TYPEA	C3	HIZ	0	8mA	i2s_sdto_o(o)	ssi1_dt_o(o)	(i-0)	(i-0)
PC20		TYPEA	C3	HIZ	0	8mA	i2s_sdti_i(i-0)	ssi1_dr_i(i-0)	(i-0)	(i-0)
PC21		TYPEA	C3	HIZ	0	8mA	i2s_adc_lrck(io-0)	ssi1_gpc_o(o)	(i-0)	(i-0)
PC22		TYPEA	C3	HIZ	0	8mA	i2s_adc_bclk(io-0)	ssi1_ce1_o(o)	(i-0)	(i-0)
PC23		TYPEA	C3	HIZ	0	8mA	i2s_mclk_o(o)	ssi1_clk_o(o)	(i-0)	(i-0)
PC24		TYPEA	C3	PU	1	8mA	i2s_dac_bclk(io-0)	ssi1_ce0_o(o)	wait_i(i-1)	(i-0)
PC25		TYPEA	C3	PD	0	8mA	pwm4_o(o)	(i-0)	dmic_dat0_i(i-0)	(i-0)
PC26		TYPEA	C3	PD	0	8mA	pwm5_o(o)	(i-0)	dmic_dat1_i(i-0)	(i-0)
PC27		TYPEA	C3	PD	0	8mA	pwm6_o(o)	smb2_sda(io-1)	(i-0)	(i-0)
PC28		TYPEA	C3	PD	0	8mA	pwm7_o(o)	smb2_sck(io-1)	(i-0)	(i-0)
PC29			C3				(i-0)	(i-0)	(i-0)	(i-0)
PC30			C3				(i-0)	(i-0)	(i-0)	(i-0)
PC31			C3				(i-0)	(i-0)	(i-0)	(i-0)

Note:

1. PC00 used as BOOT_SEL0 input during boot.
2. PC01 used as BOOT_SEL1 input during boot.
3. TYPEA is equal to MSRP_BI_SDS_33V_STB.

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21.3.4 GPIO Port D Summary

Table 21-5 GPIO Port D summary

<PAD_ID>	PAD_MNAME	PAD_TYPE	CTRL_TYPEP	PULL_RST	SMT_RST	DS_RST	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
PD00			C3				(i-0)	(i-0)	(i-0)	(i-0)
PD01			C3				(i-0)	(i-0)	(i-0)	(i-0)
PD02		TYPEA	C3	HIZ	0	8mA	tft_d2_o(o)	slcd_d0_o(o)	ssi1_dt_o(o)	(i-0)
PD03		TYPEA	C3	HIZ	0	8mA	tft_d3_o(o)	slcd_d1_o(o)	ssi1_dr_i(i-0)	(i-0)
PD04		TYPEA	C3	HIZ	0	8mA	tft_d4_o(o)	slcd_d2_o(o)	ssi1_gpc_o(o)	(i-0)
PD05		TYPEA	C3	HIZ	0	8mA	tft_d5_o(o)	slcd_d3_o(o)	ssi1_ce1_o(o)	(i-0)
PD06		TYPEA	C3	HIZ	0	8mA	tft_d6_o(o)	slcd_d4_o(o)	ssi1_clk_o(o)	(i-0)
PD07		TYPEA	C3	PU	0	8mA	tft_d7_o(o)	slcd_d5_o(o)	ssi1_ce0_o(o)	(i-0)
PD08		TYPEA	C3	HIZ	0	8mA	lcd_pclk_o(o)	(i-0)	(i-0)	(i-0)
PD09		TYPEA	C3	HIZ	0	8mA	tft_de_o(o)	slcd_wr_o(o)	(i-0)	(i-0)
PD10			C3				(i-0)	(i-0)	(i-0)	(i-0)
PD11			C3				(i-0)	(i-0)	(i-0)	(i-0)
PD12		TYPEA	C3	HIZ	0	8mA	tft_d10_o(o)	slcd_d6_o(o)	(i-0)	(i-0)
PD13		TYPEA	C3	HIZ	0	8mA	tft_d11_o(o)	slcd_d7_o(o)	(i-0)	(i-0)
PD14		TYPEA	C3	HIZ	0	8mA	tft_d12_o(o)	slcd_d8_o(o)	(i-0)	(i-0)
PD15		TYPEA	C3	HIZ	0	8mA	tft_d13_o(o)	slcd_d9_o(o)	(i-0)	(i-0)
PD16		TYPEA	C3	HIZ	0	8mA	tft_d14_o(o)	slcd_d10_o(o)	(i-0)	(i-0)
PD17		TYPEA	C3	HIZ	0	8mA	tft_d15_o(o)	slcd_d11_o(o)	(i-0)	(i-0)
PD18		TYPEA	C3	PU	0	8mA	tft_vsync_o(o)	slcd_cs_o(o)	(i-0)	(i-0)
PD19		TYPEA	C3	HIZ	0	8mA	tft_hsync_o(o)	slcd_te_i(i-0)	(i-0)	(i-0)
PD20			C3				(i-0)	(i-0)	(i-0)	(i-0)
PD21			C3				(i-0)	(i-0)	(i-0)	(i-0)
PD22		TYPEA	C3	HIZ	0	8mA	tft_d18_o(o)	slcd_d12_o(o)	(i-0)	(i-0)
PD23		TYPEA	C3	HIZ	0	8mA	tft_d19_o(o)	slcd_d13_o(o)	(i-0)	(i-0)
PD24		TYPEA	C3	HIZ	0	8mA	tft_d20_o(o)	slcd_d14_o(o)	(i-0)	(i-0)
PD25		TYPEA	C3	HIZ	0	8mA	tft_d21_o(o)	slcd_d15_o(o)	(i-0)	(i-0)
PD26		TYPEA	C3	HIZ	0	8mA	tft_d22_o(o)	slcd_rdy_i(i-0)	(i-0)	(i-0)
PD27		TYPEA	C3	HIZ	0	8mA	tft_d23_o(o)	slcd_dc_o(o)	(i-0)	(i-0)
PD28			C3				(i-0)	(i-0)	(i-0)	(i-0)
PD29			C3				(i-0)	(i-0)	(i-0)	(i-0)
PD30			C3				(i-0)	(i-0)	(i-0)	(i-0)
PD31			C3				(i-0)	(i-0)	(i-0)	(i-0)

Note: 1. TYPEA is equal to MSRP_BI_SDS_33V_STB

21.3.5 GPIO Port Z - Shadow Group

The group is a dummy group which is not mapping to any on-chip ports. It is used to avoid 3rd (intermittent) state error during configuration. Please refer for detailed information.

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21.4 Registers Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1) Register Address = Base + Address offset
2) Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3) Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset
4) Not all the register will be use in this chapter, please review the chapter of "Function Overview" for more detail.
5) Table 21-7 GPIO Registers Group Map

Name	RW	Description	Reset Value	Address Offset	Access Size
GPIO PORT A					
PAPINL	R	PORTA PIN Level Register	0x????_????	0x0000	32
PAINT	RW	PORTA Interrupt Register	0x0000_0000	0x0010	32
PAINTS	W	PORTA Interrupt Set Register	0x0000_0000	0x0014	32
PAINTC	W	PORTA Interrupt Clear Register	0x0000_0000	0x0018	32
PAMSK	RW	PORTA Interrupt Mask Register	0x1FDF_FFFF	0x0020	32
PAMSKS	W	PORTA Interrupt Mask Set Register	0x0000_0000	0x0024	32
PAMSKC	W	PORTA Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PAPAT1	RW	PORTA Pattern 1 Register	0x1FDF_FFFF	0x0030	32
PAPAT1S	W	PORTA Pattern 1 Set Register	0x0000_0000	0x0034	32
PAPAT1C	W	PORTA Pattern 1 Clear Register	0x0000_0000	0x0038	32
PAPAT0	RW	PORTA Pattern 0 Register	0x0000_0000	0x0040	32
PAPAT0S	W	PORTA Pattern 0 Set Register	0x0000_0000	0x0044	32
PAPAT0C	W	PORTA Pattern 0 Clear Register	0x0000_0000	0x0048	32
PAFLG	R	PORTA FLAG Register	0x0000_0000	0x0050	32
PAFLGC	RC	PORTA FLAG Clear Register	0x0000_0000	0x0058	32
PAGFCFG0	RW	PORTA Glitch Filter Configure 0	0x0000_0000	0x0070	32

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PAGFCFG0S	W	PORTA Glitch Filter Configure 0 Set	0x0000_0000	0x0074	32
PAGFCFG0C	W	PORTA Glitch Filter Configure 0 Clear	0x0000_0000	0x0078	32
PAGFCFG1	RW	PORTA Glitch Filter Configure 1	0x0000_0000	0x0080	32
PAGFCFG1S	W	PORTA Glitch Filter Configure 1 Set	0x0000_0000	0x0084	32
PAGFCFG1C	W	PORTA Glitch Filter Configure 1 Clear	0x0000_0000	0x0088	32
PAGFCFG2	RW	PORTA Glitch Filter Configure 2	0x0000_0000	0x0090	32
PAGFCFG2S	W	PORTA Glitch Filter Configure 2 Set	0x0000_0000	0x0094	32
PAGFCFG2C	W	PORTA Glitch Filter Configure 2 Clear	0x0000_0000	0x0098	32
PAGFCFG3	RW	PORTA Glitch Filter Configure 3	0x0000_0000	0x00A0	32
PAGFCFG3S	W	PORTA Glitch Filter Configure 3 Set	0x0000_0000	0x00A4	32
PAGFCFG3C	W	PORTA Glitch Filter Configure 3 Clear	0x0000_0000	0x00A8	32
PAVDDIO	RW	PORTA VDDIO-SEL Register	0x0000_0001	0x0100	32
PAVDDIOS	W	PORT A VDDIO-SEL Set Register	0x0000_0000	0x0104	32
PAVDDIOC	W	PORTA VDDIO-SEL Clear Register	0x0000_0000	0x0108	32
PAPEL	RW	PORTA Driver Disabled State Register0	0x0540_0000	0x0110	32
PAPELS	W	PORTA Driver Disabled State Set Register0	0x0000_0000	0x0114	32
PAPELC	W	PORTA Driver Disabled State Clear Register0	0x0000_0000	0x0118	32
PAPEH	RW	PORTA Driver Disabled State Register1	0x0155_5000	0x0120	32
PAPEHS	W	PORTA Driver Disabled State Set Register1	0x0000_0000	0x0124	32
PAPEHC	W	PORTA Driver Disabled State Clear Register1	0x0000_0000	0x0128	32
PADSL	RW	PORTA Drive Strength Register0	0xAAAA_AAAA	0x0130	32
PADSLS	W	PORTA Drive Strength Set Register0	0x0000_0000	0x0134	32
PADSLC	W	PORTA Drive Strength Clear Register0	0x0000_0000	0x0138	32
PADSH	RW	PORTA Drive Strength Register1	0x02AA_A2AA	0x0140	32
PADSHS	W	PORTA Drive Strength Set Register1	0x0000_0000	0x0144	32
PADSHC	W	PORTA Drive Strength Clear Register1	0x0000_0000	0x0148	32
PASR	RW	PORTA Slew Rate Register	0x1FDF_FFFF	0x0150	32
PASRS	W	PORTA Slew Rate Set Register	0x0000_0000	0x0154	32
PASRC	W	PORTA Slew Rate Clear Register	0x0000_0000	0x0158	32
PASMT	RW	PORTA Schmitt Trigger Register	0x0058_0000	0x0160	32
PASMTS	W	PORTA Schmitt Trigger Set Register	0x0000_0000	0x0164	32
PASMTC	W	PORTA Schmitt Trigger Clear Register	0x0000_0000	0x0168	32
PAIE	RW	PORTA Receiver enable state Register	0x1FDF_FFFF	0x0180	32
PAIES	W	PORTA Receiver enable state Set Register	0x0000_0000	0x0184	32
PAIEC	W	PORTA Receiver enable state Clear Register	0x0000_0000	0x0188	32
GPIO PORT B					

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PBPINL	R	PORTB PIN Level Register	0x????_????	0x0000	32
PBINT	RW	PORTB Interrupt Register	0x0000_0000	0x0010	32
PBINTS	W	PORTB Interrupt Set Register	0x0000_0000	0x0014	32
PBINTC	W	PORTB Interrupt Clear Register	0x0000_0000	0x0018	32
PBMSK	RW	PORTB Interrupt Mask Register	0xFE37_EFFF	0x0020	32
PBMSKS	W	PORTB Interrupt Mask Set Register	0x0000_0000	0x0024	32
PBMSKC	W	PORTB Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PBPAT1	RW	PORTB Pattern 1 Register	0xFE37_EFFF	0x0030	32
PBPAT1S	W	PORTB Pattern 1 Set Register	0x0000_0000	0x0034	32
PBPAT1C	W	PORTB Pattern 1 Clear Register	0x0000_0000	0x0038	32
PBPAT0	RW	PORTB Pattern 0 Register	0x01C8_0000	0x0040	32
PBPAT0S	W	PORTB Pattern 0 Set Register	0x0000_0000	0x0044	32
PBPAT0C	W	PORTB Pattern 0 Clear Register	0x0000_0000	0x0048	32
PBFLG	R	PORTB FLAG Register	0x0000_0000	0x0050	32
PBFLGC	RC	PORTB FLAG Clear Register	0x0000_0000	0x0058	32
PBGFCFG0	RW	PORTB Glitch Filter Configure 0	0x0000_0000	0x0070	32
PBGFCFG0S	W	PORTB Glitch Filter Configure 0 Set	0x0000_0000	0x0074	32
PBGFCFG0C	W	PORTB Glitch Filter Configure 0 Clear	0x0000_0000	0x0078	32
PBGFCFG1	RW	PORTB Glitch Filter Configure 1	0x0000_0000	0x0080	32
PBGFCFG1S	W	PORTB Glitch Filter Configure 1 Set	0x0000_0000	0x0084	32
PBGFCFG1C	W	PORTB Glitch Filter Configure 1 Clear	0x0000_0000	0x0088	32
PBGFCFG2	RW	PORTB Glitch Filter Configure 2	0x0000_0000	0x0090	32
PBGFCFG2S	W	PORTB Glitch Filter Configure 2 Set	0x0000_0000	0x0094	32
PBGFCFG2C	W	PORTB Glitch Filter Configure 2 Clear	0x0000_0000	0x0098	32
PBGFCFG3	RW	PORTB Glitch Filter Configure 3	0x0000_0000	0x00A0	32
PBGFCFG3S	W	PORTB Glitch Filter Configure 3 Set	0x0000_0000	0x00A4	32
PBGFCFG3C	W	PORTB Glitch Filter Configure 3 Clear	0x0000_0000	0x00A8	32
PBPEL	RW	PORTB Driver Disabled State Register0	0x0060_0000	0x0110	32
PBPELS	W	PORTB Driver Disabled State Set Register0	0x0000_0000	0x0114	32
PBPELC	W	PORTB Driver Disabled State Clear Register0	0x0000_0000	0x0118	32
PBPEH	RW	PORTB Driver Disabled State Register1	0x8015_0068	0x0120	32
PBPEHS	W	PORTB Driver Disabled State Set Register1	0x0000_0000	0x0124	32
PBPEHC	W	PORTB Driver Disabled State Clear Register1	0x0000_0000	0x0128	32
PBDSL	RW	PORTB Drive Strength Register0	0xA8AA_AAAA	0x0130	32
PBDSLS	W	PORTB Drive Strength Set Register0	0x0000_0000	0x0134	32
PBDSLC	W	PORTB Drive Strength Clear Register0	0x0000_0000	0x0138	32
PBDSH	RW	PORTB Drive Strength Register1	0xAAAA_AAAA	0x0140	32
PBDSHS	W	PORTB Drive Strength Set Register1	0x0000_0000	0x0144	32

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PBDSHC	W	PORTB Drive Strength Clear Register1	0x0000_0000	0x0148	32
PBSR	RW	PORTB Slew Rate Register	0xFFFF_EFFF	0x0150	32
PBSRS	W	PORTB Slew Rate Set Register	0x0000_0000	0x0154	32
PBSRC	W	PORTB Slew Rate Clear Register	0x0000_0000	0x0158	32
PBSMT	RW	PORTB Schmitt Trigger Register	0x7800_0000	0x0160	32
PBSMTS	W	PORTB Schmitt Trigger Set Register	0x0000_0000	0x0164	32
PBSMTC	W	PORTB Schmitt Trigger Clear Register	0x0000_0000	0x0168	32
PBIE	RW	PORTB Receiver enable state Register	0xFFFF_EFFF	0x0180	32
PBIES	W	PORTB Receiver enable state Set Register	0x0000_0000	0x0184	32
PBIEC	W	PORTB Receiver enable state Clear Register	0x0000_0000	0x0188	32
GPIO PORT C					
PCPINL	R	PORTC PIN Level Register	0x????_????	0x0000	32
PCINT	RW	PORTC Interrupt Register	0x0000_0000	0x0010	32
PCINTS	W	PORTC Interrupt Set Register	0x0000_0000	0x0014	32
PCINTC	W	PORTC Interrupt Clear Register	0x0000_0000	0x0018	32
PCMSK	RW	PORTC Interrupt Mask Register	0x01FF_FBFF	0x0020	32
PCMSKS	W	PORTC Interrupt Mask Set Register	0x0000_0000	0x0024	32
PCMSKC	W	PORTC Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PCPAT1	RW	PORTC Pattern 1 Register	0x01FF_FBFF	0x0030	32
PCPAT1S	W	PORTC Pattern 1 Set Register	0x0000_0000	0x0034	32
PCPAT1C	W	PORTC Pattern 1 Clear Register	0x0000_0000	0x0038	32
PCPAT0	RW	PORTC Pattern 0 Register	0x0000_0000	0x0040	32
PCPAT0S	W	PORTC Pattern 0 Set Register	0x0000_0000	0x0044	32
PCPAT0C	W	PORTC Pattern 0 Clear Register	0x0000_0000	0x0048	32
PCFLG	R	PORTC FLAG Register	0x0000_0000	0x0050	32
PCFLGC	RC	PORTC FLAG Clear Register	0x0000_0000	0x0058	32
PCGFCFG0	RW	PORTC Glitch Filter Configure 0	0x0000_0000	0x0070	32
PCGFCFG0S	W	PORTC Glitch Filter Configure 0 Set	0x0000_0000	0x0074	32
PCGFCFG0C	W	PORTC Glitch Filter Configure 0 Clear	0x0000_0000	0x0078	32
PCGFCFG1	RW	PORTC Glitch Filter Configure 1	0x0000_0000	0x0080	32
PCGFCFG1S	W	PORTC Glitch Filter Configure 1 Set	0x0000_0000	0x0084	32
PCGFCFG1C	W	PORTC Glitch Filter Configure 1 Clear	0x0000_0000	0x0088	32
PCGFCFG2	RW	PORTC Glitch Filter Configure 2	0x0000_0000	0x0090	32
PCGFCFG2S	W	PORTC Glitch Filter Configure 2 Set	0x0000_0000	0x0094	32
PCGFCFG2C	W	PORTC Glitch Filter Configure 2 Clear	0x0000_0000	0x0098	32
PCGFCFG3	RW	PORTC Glitch Filter Configure 3	0x0000_0000	0x00A0	32
PCGFCFG3S	W	PORTC Glitch Filter Configure 3 Set	0x0000_0000	0x00A4	32
PCGFCFG3C	W	PORTC Glitch Filter Configure 3 Clear	0x0000_0000	0x00A8	32
PCPEL	RW	PORTC Driver Disabled State Register0	0x000A_0009	0x0110	32
PCPELS	W	PORTC Driver Disabled State Set	0x0000_0000	0x0114	32

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		Register0			
PCPELC	W	PORTC Driver Disabled State Clear Register0	0x0000_0000	0x0118	32
PCPEH	RW	PORTC Driver Disabled State Register1	0x02A9_0001	0x0120	32
PCPEHS	W	PORTC Driver Disabled State Set Register1	0x0000_0000	0x0124	32
PCPEHC	W	PORTC Driver Disabled State Clear Register1	0x0000_0000	0x0128	32
PCDSL	RW	PORTC Drive Strength Register0	0xAA8A_AAAA	0x0130	32
PCDSLS	W	PORTC Drive Strength Set Register0	0x0000_0000	0x0134	32
PCDSLC	W	PORTC Drive Strength Clear Register0	0x0000_0000	0x0138	32
PCDSH	RW	PORTC Drive Strength Register1	0x02AA_AAAA	0x0140	32
PCDSHS	W	PORTC Drive Strength Set Register1	0x0000_0000	0x0144	32
PCDSHC	W	PORTC Drive Strength Clear Register1	0x0000_0000	0x0148	32
PCSR	RW	PORTC Slew Rate Register	0x1FFF_FBFF	0x0150	32
PCSRS	W	PORTC Slew Rate Set Register	0x0000_0000	0x0154	32
PCSRC	W	PORTC Slew Rate Clear Register	0x0000_0000	0x0158	32
PCSMT	RW	PORTC Schmitt Trigger Register	0x0106_0300	0x0160	32
PCSMTS	W	PORTC Schmitt Trigger Set Register	0x0000_0000	0x0164	32
PCSMTC	W	PORTC Schmitt Trigger Clear Register	0x0000_0000	0x0168	32
PCIE	RW	PORTC Receiver enable state Register	0x1FFF_FBFF	0x0180	32
PCIES	W	PORTC Receiver enable state Set Register	0x0000_0000	0x0184	32
PCIEC	W	PORTC Receiver enable state Clear Register	0x0000_0000	0x0188	32
GPIO PORT D					
PDPINL	R	PORTD PIN Level Register	0x????_????	0x0000	32
PDINT	RW	PORTD Interrupt Register	0x0000_0000	0x0010	32
PDINTS	W	PORTD Interrupt Set Register	0x0000_0000	0x0014	32
PDINTC	W	PORTD Interrupt Clear Register	0x0000_0000	0x0018	32
PDMSK	RW	PORTD Interrupt Mask Register	0x0FCF_F3FC	0x0020	32
PDMSKS	W	PORTD Interrupt Mask Set Register	0x0000_0000	0x0024	32
PDMSKC	W	PORTD Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PDPAT1	RW	PORTD Pattern 1 Register	0x0FCF_F3FC	0x0030	32
PDPAT1S	W	PORTD Pattern 1 Set Register	0x0000_0000	0x0034	32
PDPAT1C	W	PORTD Pattern 1 Clear Register	0x0000_0000	0x0038	32
PDPAT0	RW	PORTD Pattern 0 Register	0x0000_0000	0x0040	32
PDPAT0S	W	PORTD Pattern 0 Set Register	0x0000_0000	0x0044	32
PDPAT0C	W	PORTD Pattern 0 Clear Register	0x0000_0000	0x0048	32
PDFLG	R	PORTD FLAG Register	0x0000_0000	0x0050	32
PDFLGC	RC	PORTD FLAG Clear Register	0x0000_0000	0x0058	32
PDGFCFG0	RW	PORTD Glitch Filter Configure 0	0x0000_0000	0x0070	32

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PDGFCFG0S	W	PORTD Glitch Filter Configure 0 Set	0x0000_0000	0x0074	32
PDGFCFG0C	W	PORTD Glitch Filter Configure 0 Clear	0x0000_0000	0x0078	32
PDGFCFG1	RW	PORTD Glitch Filter Configure 1	0x0000_0000	0x0080	32
PDGFCFG1S	W	PORTD Glitch Filter Configure 1 Set	0x0000_0000	0x0084	32
PDGFCFG1C	W	PORTD Glitch Filter Configure 1 Clear	0x0000_0000	0x0088	32
PDGFCFG2	RW	PORTD Glitch Filter Configure 2	0x0000_0000	0x0090	32
PDGFCFG2S	W	PORTD Glitch Filter Configure 2 Set	0x0000_0000	0x0094	32
PDGFCFG2C	W	PORTD Glitch Filter Configure 2 Clear	0x0000_0000	0x0098	32
PDGFCFG3	RW	PORTD Glitch Filter Configure 3	0x0000_0000	0x00A0	32
PDGFCFG3S	W	PORTD Glitch Filter Configure 3 Set	0x0000_0000	0x00A4	32
PDGFCFG3C	W	PORTD Glitch Filter Configure 3 Clear	0x0000_0000	0x00A8	32
PDPEL	RW	PORTD Driver Disabled State Register0	0x0000_4000	0x0110	32
PDPELS	W	PORTD Driver Disabled State Set Register0	0x0000_0000	0x0114	32
PDPELC	W	PORTD Driver Disabled State Clear Register0	0x0000_0000	0x0118	32
PDPEH	RW	PORTD Driver Disabled State Register1	0x0000_0010	0x0120	32
PDPEHS	W	PORTD Driver Disabled State Set Register1	0x0000_0000	0x0124	32
PDPEHC	W	PORTD Driver Disabled State Clear Register1	0x0000_0000	0x0128	32
PDDSL	RW	PORTD Drive Strength Register0	0xAA0A_AAA0	0x0130	32
PDDSLS	W	PORTD Drive Strength Set Register0	0x0000_0000	0x0134	32
PDDSLC	W	PORTD Drive Strength Clear Register0	0x0000_0000	0x0138	32
PDDSH	RW	PORTD Drive Strength Register1	0x00AA_A0AA	0x0140	32
PDDSHS	W	PORTD Drive Strength Set Register1	0x0000_0000	0x0144	32
PDDSHC	W	PORTD Drive Strength Clear Register1	0x0000_0000	0x0148	32
PDSR	RW	PORTD Slew Rate Register	0x0FCF_F3FC	0x0150	32
PDSRS	W	PORTD Slew Rate Set Register	0x0000_0000	0x0154	32
PDSRC	W	PORTD Slew Rate Clear Register	0x0000_0000	0x0158	32
PDSMT	RW	PORTD Schmitt Trigger Register	0x0000_0000	0x0160	32
PDSMTS	W	PORTD Schmitt Trigger Set Register	0x0000_0000	0x0164	32
PDSMTC	W	PORTD Schmitt Trigger Clear Register	0x0000_0000	0x0168	32
PDIE	RW	PORTD Receiver enable state Register	0x0FCF_F3FC	0x0180	32
PDIES	W	PORTD Receiver enable state Set Register	0x0000_0000	0x0184	32
PDIEC	W	PORTD Receiver enable state Clear Register	0x0000_0000	0x0188	32
Shadow Register Group PZ					
PzINTS	W	Shadow Interrupt Set Register	0x0000_0000	0x0014	32
PzINTC	W	Shadow Interrupt Clear Register	0x0000_0000	0x0018	32
PzMSKS	W	Shadow Interrupt Mask Set Register	0x0000_0000	0x0024	32

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PzMSKC	W	Shadow Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PzPAT1S	W	Shadow Interrupt Pattern 1 Set Register	0x0000_0000	0x0034	32
PzPAT1C	W	Shadow Interrupt Pattern 1 Clear Register	0x0000_0000	0x0038	32
PzPAT0S	W	Shadow Interrupt Pattern 0 Set Register	0x0000_0000	0x0044	32
PzPAT0C	W	Shadow Interrupt Pattern 0 Clear Register	0x0000_0000	0x0048	32
PzGID2LD	W	PORT Group ID to be load from PZ Register	0x0000_0000	0x00F0	32

Note: 1. Pz**** in the description of register is use for shadow operation for other groups, more details will description as follow chapters.

21.4.1.1 PORT PIN Level Registers (PxPINL,0x0000)

PAPINL,PBPINL,PCPINL and PDPINL are four 32-bit PORT PIN level registers. They are read-only registers.

	PxPINL																															**Base + 0x0000**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PINL31	PINL30	PINL29	PINL28	PINL27	PINL26	PINL25	PINL24	PINL23	PINL22	PINL21	PINL20	PINL19	PINL18	PINL17	PINL16	PINL15	PINL14	PINL13	PINL12	PINL11	PINL10	PINL09	PINL08	PINL07	PINL06	PINL05	PINL04	PINL03	PINL02	PINL01	PINL00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PINL n	Where n = 0 ~ 31 and PBPINL n = PBPINL0 ~ PBPINL31. The PORTB PIN level can be read by reading PINL n bit in register PBPINL.	R

Note:

1. In the table, "x" represents the group A,B,C and D behind the description of similar.

21.4.1.2 PORT Interrupt Registers (PxINT,0x0010)

PAINT,PBINT,PCINT and PDINT are four 32-bit PORT interrupt registers.

	PxINT																															**Base + 0x0010**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT31	INT30	INT29	INT28	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT30	INT19	INT18	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10	INT09	INT08	INT07	INT06	INT05	INT04	INT03	INT02	INT01	INT00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W

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31:0	INT n	Where n = 0 ~ 31 and INT n = INT31 ~ INT00. Interrupt enable. 0: Corresponding pin is used as device functions or normal gpio 1: Corresponding pin is used as interrupt	RW

21.4.1.3 PORT Interrupt Set Registers (PxINTS,0x0014)

PAINTS,PBINTS,PCINTS and PDINTS are four 32-bit PORT interrupt set registers.

	PxINTS																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTS31	INTS30	INTS29	INTS28	INTS27	INTS26	INTS25	INTS24	INTS23	INTS22	INTS21	INTS20	INTS19	INTS18	INTS17	INTS16	INTS15	INTS14	INTS13	INTS12	INTS11	INTS10	INTS09	INTS08	INTS07	INTS06	INTS05	INTS04	INTS03	INTS02	INTS01	INTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INTS n	Writing 1 to INTS n will set INT n to 1 in register PBINT. Writing 0 to INTS n will no use.	W

21.4.1.4 PORT Interrupt Clear Registers (PxINTC,0x0018)

PAINTC,PBINTC,PCINTC and PDINTC are four 32-bit PORT interrupt clear registers.

	PxINTC																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC31	INTC30	INTC29	INTC28	INTC27	INTC26	INTC25	INTC24	INTC23	INTC22	INTC21	INTC20	INTC19	INTC18	INTC17	INTC16	INTC15	INTC14	INTC13	INTC12	INTC11	INTC10	INTC09	INTC08	INTC07	INTC06	INTC05	INTC04	INTC03	INTC02	INTC01	INTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INTC n	Writing 1 to INTC n will set INT n to 0 in register PxINT. Writing 0 to INTC n will no use.	W

21.4.1.5 PORT Mask Registers (PxMSK,0x0020)

PAMSK,PBMSK,PCMSK and PDMSK are four 32-bit PORT mask registers.

	PxMSK	Base + 0x0020

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSK31	MSK30	MSK29	MSK28	MSK27	MSK26	MSK25	MSK24	MSK23	MSK22	MSK21	MSK20	MSK19	MSK18	MSK17	MSK16	MSK15	MSK14	MSK13	MSK12	MSK11	MSK10	MSK09	MSK08	MSK07	MSK06	MSK05	MSK04	MSK03	MSK02	MSK01	MSK00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	MSK n	Where n = 0 ~ 31 and MSK n = MSK31 ~ MSK0. When INT n = 1: 0: Enable the pin as an interrupt source 1: Disable the pin as an interrupt source When INT n = 0: 0: Corresponding pin will be used as device function 1: Corresponding pin will be used as gpio	RW

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.1.6 PORT Mask Set Registers (PxMSKS,0x0024)

PAMSKS,PBMSKS,PCMSKS and PDMSKS are four 32-bit PORT mask set registers.

	PxMSKS																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKS31	MSKS30	MSKS29	MSKS28	MSKS27	MSKS26	MSKS25	MSKS24	MSKS23	MSKS22	MSKS21	MSKS20	MSKS19	MSKS18	MSKS17	MSKS16	MSKS15	MSKS14	MSKS13	MSKS12	MSKS11	MSKS10	MSKS09	MSKS08	MSKS07	MSKS06	MSKS05	MSKS04	MSKS03	MSKS02	MSKS01	MSKS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	MSKS n	Writing 1 to MSKS n will set MSK n to 1 in register PBMSK. Writing 0 to MSKS n will no use.	W

21.4.1.7 PORT Mask Clear Registers (PxMSKC,0x0028)

PAMSKC,PBMSKC,PCMSKC and PDMSKC are four 32-bit PORT mask clear registers.

	PxMSKC																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	MSKC31	MSKC30	MSKC29	MSKC28	MSKC27	MSKC26	MSKC25	MSKC24	MSKC23	MSKC22	MSKC21	MSKC20	MSKC19	MSKC18	MSKC17	MSKC16	MSKC15	MSKC14	MSKC13	MSKC12	MSKC11	MSKC10	MSKC09	MSKC08	MSKC07	MSKC06	MSKC05	MSKC04	MSKC03	MSKC02	MSKC01	MSKC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	MSKC n	Writing 1 to MSKC n will set MSK n to 0 in register PBMSK. Writing 0 to MSKC n will no use.	W

21.4.1.8 PORT PAT1/Direction Registers (PxPAT1,0x0030)

PAPAT1,PBPAT1,PCPAT1 and PDPAT1 are four 32-bit PORT PAttern1/direction registers.

	PxPAT1																															**Base + 0x0030**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT131	PAT130	PAT129	PAT128	PAT127	PAT126	PAT125	PAT124	PAT123	PAT122	PAT121	PAT120	PAT119	PAT118	PAT117	PAT116	PAT115	PAT114	PAT113	PAT112	PAT111	PAT110	PAT109	PAT108	PAT107	PAT106	PAT105	PAT104	PAT103	PAT102	PAT101	PAT100
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PAT1 n	Where n = 0 ~ 31 and PBPAT1 n = PAT131 ~ PAT10. When INT n = 1 (Interrupt function): 0: Level trigger interrupt 1: Edge trigger interrupt When INT n = 0 and MSK = 0 (Device function): 0: Corresponding pin is used as device 0 or device 1 function 1: Corresponding pin is used as device 2 or device 3 function When INT n = 0 and MSK = 0 (GPIO function): 0: Corresponding pin is used as gpio output 1: Corresponding pin is used as gpio input	RW

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.1.9 PORT PAT1/Direction Set Registers (PxPAT1S,0x0034)

PAPAT1S,PBPAT1S, PCPAT1S and PDPAT1S are four 32-bit PORT PATtern1 or direction set registers.

	PxPAT1S																															**Base + 0x0034**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	PAT1S31	PAT1S30	PAT1S29	PAT1S28	PAT1S27	PAT1S26	PAT1S25	PAT1S24	PAT1S23	PAT1S22	PAT1S21	PAT1S20	PAT1S19	PAT1S18	PAT1S17	PAT1S16	PAT1S15	PAT1S14	PAT1S13	PAT1S12	PAT1S11	PAT1S10	PAT1S09	PAT1S08	PAT1S07	PAT1S06	PAT1S05	PAT1S04	PAT1S03	PAT1S02	PAT1S01	PAT1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT1S n	Writing 1 to PAT1S n will set PAT1 n to 1 in register PBPAT1. Writing 0 to PAT1S n will no use.	W

21.4.1.10 PORT PAT1/Direction Clear Registers (PxPAT1C,0x0038)

PAPAT1C,PBPAT1C,PCPAT1C,PDPAT1C are four 32-bit PORT PATtern1 or direction clear registers.

	PxPAT1S,																															**Base + 0x0038**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1C31	PAT1C30	PAT1C29	PAT1C28	PAT1C27	PAT1C26	PAT1C25	PAT1C24	PAT1C23	PAT1C22	PAT1C21	PAT1C20	PAT1C19	PAT1C18	PAT1C17	PAT1C16	PAT1C15	PAT1C14	PAT1C13	PAT1C12	PAT1C11	PAT1C10	PAT1C09	PAT1C08	PAT1C07	PAT1C06	PAT1C05	PAT1C04	PAT1C03	PAT1C02	PAT1C01	PAT1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT1C n	Writing 1 to PAT1C n will set PAT1 n to 0 in register PBPAT1. Writing 0 to PAT1C n will no use.	W

21.4.1.11 PORT PAT0/Data Registers (PxPAT0,0x0040)

PAPAT0,PBPAT0,PCPAT0 and PDPAT0 are four 32-bit PORT PATtern0 or data registers.

	PxPAT0,																															**Base + 0x0040**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT031	PAT030	PAT029	PAT028	PAT027	PAT026	PAT025	PAT024	PAT023	PAT022	PAT021	PAT020	PAT019	PAT018	PAT017	PAT016	PAT015	PAT014	PAT013	PAT012	PAT011	PAT010	PAT009	PAT008	PAT007	PAT006	PAT005	PAT004	PAT003	PAT002	PAT001	PAT000
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PAT0 n	Where n = 0 ~ 31 and PAT0 n = PAT00 ~ PAT031. When INTn = 1 and PAT1 = 0:	RW

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		0: Port is low level triggered interrupt input 1: Port is low high triggered interrupt input When INTn = 1 and PAT1 = 1: 0: Port is falling edge triggered interrupt input 1: Port is rising edge triggered interrupt input When INTn = 0 and MSK = 0 and PAT1 = 0: 0: Port is pin of device 0 1: Port is pin of device 1 When INTn = 0 and MSK = 0 and PAT1 = 1: 0: Port is pin of device 2 1: Port is pin of device 3 When INTn = 0 and MSK = 1 and PAT1 = 0: 0: Port is GPIO output 0 1: Port is GPIO output 1	

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.1.12 PORT PAT0/Data Set Registers (PxPAT0S,0x0044)

PAPAT0S,PBPAT0S,PCPAT0S and PDPAT0S are four 32-bit PORT PATtern0 or data set registers.

	PxPAT0S																															**Base + 0x0044**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0S31	PAT0S30	PAT0S29	PAT0S28	PAT0S27	PAT0S26	PAT0S25	PAT0S24	PAT0S23	PAT0S22	PAT0S21	PAT0S20	PAT0S19	PAT0S18	PAT0S17	PAT0S16	PAT0S15	PAT0S14	PAT0S13	PAT0S12	PAT0S11	PAT0S10	PAT0S09	PAT0S08	PAT0S07	PAT0S06	PAT0S05	PAT0S04	PAT0S03	PAT0S02	PAT0S01	PAT0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT0S n	Writing 1 to PBPAT0S n will set PAT0 n to 1 in register PBPAT0. Writing 0 to PBPAT0S n will no use.	W

21.4.1.13 PORT PAT0/Data Clear Registers (PxPAT0C,0x0048)

PAPAT0C,PBPAT0C,PCPAT0C and PDPAT0C are four 32-bit PORT PATtern 0 or data clear registers.

	PxPAT0C																															**Base + 0x0048**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	PAT0C31	PAT0C30	PAT0C29	PAT0C28	PAT0C27	PAT0C26	PAT0C25	PAT0C24	PAT0C23	PAT0C22	PAT0C21	PAT0C20	PAT0C19	PAT0C18	PAT0C17	PAT0C16	PAT0C15	PAT0C14	PAT0C13	PAT0C12	PAT0C11	PAT0C10	PAT0C09	PAT0C08	PAT0C07	PAT0C06	PAT0C05	PAT0C04	PAT0C03	PAT0C02	PAT0C01	PAT0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT0C n	Writing 1 to PAT0C n will set PAT0 n to 0 in register PBPAT0. Writing 0 to PAT0C n will no use.	W

21.4.1.14 PORT FLAG Registers (PxFLG,0x0050)

PAFLG,PBFLG,PCFLG and PDFLG are four 32-bit PORT flag registers. They are read-only registers.

	PxFLG																															**Base + 0x0050**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAG31	FLAG30	FLAG29	FLAG28	FLAG27	FLAG26	FLAG25	FLAG24	FLAG23	FLAG22	FLAG21	FLAG20	FLAG19	FLAG18	FLAG17	FLAG16	FLAG15	FLAG14	FLAG13	FLAG12	FLAG11	FLAG10	FLAG09	FLAG08	FLAG07	FLAG06	FLAG05	FLAG04	FLAG03	FLAG02	FLAG01	FLAG00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	FLAG n	Where n = 0 ~ 31 and FLAG n = FLAG00 ~ FLAG31. FLAG n is interrupt flag bit for checking the interrupt whether to happen. When GPIO is used as interrupt function and the interrupt happened, the FLAG n in PBFLG will be set to 1.	R

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.1.15 PORT FLAG Clear Registers (PxFLGC,0x0058)

PAFLGC,PBFLGC,PCFLGC and PDFLGC are four 32-bit PORT flag clear registers. They are read-only registers.

	PxFLGC																															**Base + 0x0058**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	FLAGC31	FLAGC30	FLAGC29	FLAGC28	FLAGC27	FLAGC26	FLAGC25	FLAGC24	FLAGC23	FLAGC22	FLAGC21	FLAGC20	FLAGC19	FLAGC18	FLAGC17	FLAGC16	FLAGC15	FLAGC14	FLAGC13	FLAGC12	FLAGC11	FLAGC10	FLAGC09	FLAGC08	FLAGC07	FLAGC06	FLAGC05	FLAGC04	FLAGC03	FLAGC02	FLAGC01	FLAGC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	FLAGC n	When GPIO is used as interrupt function and when write 1 to the bit, the bit FLAG n in PBFLG will be cleared.	RC

21.4.1.16 PORT GLITCH FILTER Configure Register 0 (PxGFCFG0,0x0070)

PAGFCFG0,PBGFCFG0,PCGFCFG0 and PDGFCFG0 are four 32-bit PORT glitch filter control bit 0 registers.

	PxGFCFG0																															**Base + 0x0070**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG031	GFCFG030	GFCFG029	GFCFG028	GFCFG027	GFCFG026	GFCFG025	GFCFG024	GFCFG023	GFCFG022	GFCFG021	GFCFG020	GFCFG019	GFCFG018	GFCFG017	GFCFG016	GFCFG015	GFCFG014	GFCFG013	GFCFG012	GFCFG011	GFCFG010	GFCFG009	GFCFG008	GFCFG007	GFCFG006	GFCFG005	GFCFG004	GFCFG003	GFCFG002	GFCFG001	GFCFG000
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG0 n	Where n = 0 ~ 31 and GFCFG0 n = GFCFG00 ~ GFCFG031. GFCFG0 n is used for suppress the glitch filter on port signal bit 0 value . 0: glitch filter control signal bit 0 value is 0 1: glitch filter control signal bit 0 value is 1	RW

Note:

1. Not every PBD support glitch filter control, please check out Function Overview chapter for details.

21.4.1.17 PORT GLITCH FILTER Configure Set Register 0 (PxGFCFG0S,0x0074)

PAGFCFG0S,PBGFCFG0S,PCGFCFG0S and PDGFCFG0S are four 32-bit PORT glitch filter control bit 0 set registers.

	PxGFCFG0S																															**Base + 0x0074**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	GFCFG0S31	GFCFG0S30	GFCFG0S29	GFCFG0S28	GFCFG0S27	GFCFG0S26	GFCFG0S25	GFCFG0S24	GFCFG0S23	GFCFG0S22	GFCFG0S21	GFCFG0S20	GFCFG0S19	GFCFG0S18	GFCFG0S17	GFCFG0S16	GFCFG0S15	GFCFG0S14	GFCFG0S13	GFCFG0S12	GFCFG0S11	GFCFG0S10	GFCFG0S09	GFCFG0S08	GFCFG0S07	GFCFG0S06	GFCFG0S05	GFCFG0S04	GFCFG0S03	GFCFG0S02	GFCFG0S01	GFCFG0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG0S n	Writing 1 to GFCFG0S n will set glitch filter control signal GFCFG0 n to 0 in register PBGFCFG0. Writing 0 to GFCFG0S n will no use.	W

21.4.1.18 PORT GLITCH FILTER Configure Clear Register 0 (PxGFCFG0C,0x0078)

PAGFCFG0C,PBGFCFG0C,PCGFCFG0C and PDGFCFG0C are four 32-bit PORT glitch filter control bit 0 clear registers.

	PxGFCFG0C																															**Base + 0x0078**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG0C31	GFCFG0C30	GFCFG0C29	GFCFG0C28	GFCFG0C27	GFCFG0C26	GFCFG0C25	GFCFG0C24	GFCFG0C23	GFCFG0C22	GFCFG0C21	GFCFG0C20	GFCFG0C19	GFCFG0C18	GFCFG0C17	GFCFG0C16	GFCFG0C15	GFCFG0C14	GFCFG0C13	GFCFG0C12	GFCFG0C11	GFCFG0C10	GFCFG0C09	GFCFG0C08	GFCFG0C07	GFCFG0C06	GFCFG0C05	GFCFG0C04	GFCFG0C03	GFCFG0C02	GFCFG0C01	GFCFG0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG0C n	Writing 1 to GFCFG0C n will clear glitch filter control signal GFCFG0 n to 0 in register PxGFCFG0. Writing 0 to GFCFG0C n will no use.	W

21.4.1.19 PORT GLITCH FILTER Configure Register 1 (PxGFCFG1,0x0080)

PAGFCFG1,PBGFCFG1,PCGFCFG1 and PDGFCFG1 are four 32-bit PORT glitch filter control bit 1 registers.

	PxGFCFG1																															**Base + 0x0080**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG131	GFCFG130	GFCFG129	GFCFG128	GFCFG127	GFCFG126	GFCFG125	GFCFG124	GFCFG123	GFCFG122	GFCFG121	GFCFG120	GFCFG119	GFCFG118	GFCFG117	GFCFG116	GFCFG115	GFCFG114	GFCFG113	GFCFG112	GFCFG111	GFCFG110	GFCFG109	GFCFG108	GFCFG107	GFCFG106	GFCFG105	GFCFG104	GFCFG103	GFCFG102	GFCFG101	GFCFG100

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RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG1 n	Where n = 0 ~ 31 and GFCFG1 n = GFCFG10 ~ GFCFG131. GFCFG1 n is used for suppress the glitch filter on port signal bit 1 value . 0: glitch filter control signal bit 1 value is 0 1: glitch filter control signal bit 1 value is 1	RW

Note:

1. Not every PBD support glitch filter control, please check out Function Overview chapter for details.

21.4.1.20 PORT GLITCH FILTER Configure Register 1 (PxGFCFG1S,0x0084)

PAGFCFG1S,PBGFCFG1S,PCGFCFG1S and PDGFCFG1S are four 32-bit PORT glitch filter control bit 1 set registers.

	PxGFCFG1S																															**Base + 0x0084**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG1S31	GFCFG1S30	GFCFG1S29	GFCFG1S28	GFCFG1S27	GFCFG1S26	GFCFG1S25	GFCFG1S24	GFCFG1S23	GFCFG1S22	GFCFG1S21	GFCFG1S20	GFCFG1S19	GFCFG1S18	GFCFG1S17	GFCFG1S16	GFCFG1S15	GFCFG1S14	GFCFG1S13	GFCFG1S12	GFCFG1S11	GFCFG1S10	GFCFG1S09	GFCFG1S08	GFCFG1S07	GFCFG1S06	GFCFG1S05	GFCFG1S04	GFCFG1S03	GFCFG1S02	GFCFG1S01	GFCFG1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG1S n	Writing 1 to GFCFG1S n will set glitch filter control signal GFCFG1 n to 0 in register PBGFCFG1. Writing 0 to GFCFG1S n will no use.	W

21.4.1.21 PORT GLITCH FILTER Configure Register 1 (PxGFCFG1C,0x0088)

PAGFCFG1C,PBGFCFG1C,PCGFCFG1C and PDGFCFG1C are four 32-bit PORT glitch filter control bit 1 clear registers.

	PxGFCFG1C																															**Base + 0x0088**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG1C31	GFCFG1C30	GFCFG1C29	GFCFG1C28	GFCFG1C27	GFCFG1C26	GFCFG1C25	GFCFG1C24	GFCFG1C23	GFCFG1C22	GFCFG1C21	GFCFG1C20	GFCFG1C19	GFCFG1C18	GFCFG1C17	GFCFG1C16	GFCFG1C15	GFCFG1C14	GFCFG1C13	GFCFG1C12	GFCFG1C11	GFCFG1C10	GFCFG1C09	GFCFG1C08	GFCFG1C07	GFCFG1C06	GFCFG1C05	GFCFG1C04	GFCFG1C03	GFCFG1C02	GFCFG1C01	GFCFG1C00

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RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG1C n	Writing 1 to GFCFG1C n will clear glitch filter control signal GFCFG1 n to 0 in register PBGFCFG1. Writing 0 to GFCFG1C n will no use.	W

21.4.1.22 PORT GLITCH FILTER Configure Register 2 (PxGFCFG2,0x0090)

PAGFCFG2,PBGFCFG2,PCGFCFG2 and PDGFCFG2 are four 32-bit PORT glitch filter control bit 2 registers.

	PxGFCFG2																															**Base + 0x0090**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG231	GFCFG230	GFCFG229	GFCFG228	GFCFG227	GFCFG226	GFCFG225	GFCFG224	GFCFG223	GFCFG222	GFCFG221	GFCFG220	GFCFG219	GFCFG218	GFCFG217	GFCFG216	GFCFG215	GFCFG214	GFCFG213	GFCFG212	GFCFG211	GFCFG210	GFCFG209	GFCFG208	GFCFG207	GFCFG206	GFCFG205	GFCFG204	GFCFG203	GFCFG202	GFCFG201	GFCFG200
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG2 n	Where n = 0 ~ 31 and GFCFG2 n = GFCFG20 ~ GFCFG231. GFCFG2 n is used for suppress the glitch filter on port signal bit 2 value . 0: glitch filter control signal bit 2 value is 0 1: glitch filter control signal bit 2 value is 1	RW

Note:

1. Not every PBD support Schmitt Trigger Control, please check out Function Overview chapter for details.

21.4.1.23 PORT GLITCH FILTER Configure Set Register 2 (PxGFCFG2S,0x0094)

PAGFCFG2S,PBGFCFG2S,PCGFCFG2S and PDGFCFG2S are four 32-bit PORT glitch filter control bit 2 set registers.

	PxGFCFG2S																															**Base + 0x0094**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG2S31	GFCFG2S30	GFCFG2S29	GFCFG2S28	GFCFG2S27	GFCFG2S26	GFCFG2S25	GFCFG2S24	GFCFG2S23	GFCFG2S22	GFCFG2S21	GFCFG2S20	GFCFG2S19	GFCFG2S18	GFCFG2S17	GFCFG2S16	GFCFG2S15	GFCFG2S14	GFCFG2S13	GFCFG2S12	GFCFG2S11	GFCFG2S10	GFCFG2S09	GFCFG2S08	GFCFG2S07	GFCFG2S06	GFCFG2S05	GFCFG2S04	GFCFG2S03	GFCFG2S02	GFCFG2S01	GFCFG2S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:0	GFCFG2S n	Writing 1 to GFCFG2S n will set glitch filter control signal GFCFG2 n to 0 in register PBGFCFG2. Writing 0 to GFCFG2S n will no use.	W

21.4.1.24 PORT GLITCH FILTER Configure Clear Register 2 (PxGFCFG2C,0x0098)

PAGFCFG2C,PBGFCFG2C,PCGFCFG2C and PDGFCFG2C are four 32-bit PORT glitch filter control bit 2 clear registers.

	PxGFCFG2C																															Base + 0x0098
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG2C31	GFCFG2C30	GFCFG2C29	GFCFG2C28	GFCFG2C27	GFCFG2C26	GFCFG2C25	GFCFG2C24	GFCFG2C23	GFCFG2C22	GFCFG2C21	GFCFG2C20	GFCFG2C19	GFCFG2C18	GFCFG2C17	GFCFG2C16	GFCFG2C15	GFCFG2C14	GFCFG2C13	GFCFG2C12	GFCFG2C11	GFCFG2C10	GFCFG2C09	GFCFG2C08	GFCFG2C07	GFCFG2C06	GFCFG2C05	GFCFG2C04	GFCFG2C03	GFCFG2C02	GFCFG2C01	GFCFG2C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG2C n	Writing 1 to GFCFG2C n will clear glitch filter control signal GFCFG2 n to 0 in register PBGFCFG2. Writing 0 to GFCFG2C n will no use.	W

21.4.1.25 PORT GLITCH FILTER Configure Register 3 (PxGFCFG3,0x00A0)

PAGFCFG3,PBGFCFG3,PCGFCFG3 and PDGFCFG3 are four 32-bit PORT glitch filter control bit 3 registers.

	PxGFCFG3																															Base + 0x00A0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG331	GFCFG330	GFCFG329	GFCFG328	GFCFG327	GFCFG326	GFCFG325	GFCFG324	GFCFG323	GFCFG322	GFCFG321	GFCFG320	GFCFG319	GFCFG318	GFCFG317	GFCFG316	GFCFG315	GFCFG314	GFCFG313	GFCFG312	GFCFG311	GFCFG310	GFCFG309	GFCFG308	GFCFG307	GFCFG306	GFCFG305	GFCFG304	GFCFG303	GFCFG302	GFCFG301	GFCFG300
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG3 n	Where n = 0 ~ 31 and GFCFG3 n = GFCFG30 ~ GFCFG331. GFCFG3 n is used for suppress the glitch filter on port signal bit 3 value . 0: glitch filter control signal bit 3 value is 0	RW

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		1: glitch filter control signal bit 3 value is 1	

Note:

1. Not every PBD support glitch filter control, please check out Function Overview chapter for details.

21.4.1.26 PORT GLITCH FILTER Configure Set Register 3 (PxGFCFG3S,0x00A4)

PAGFCFG3S,PBGFCFG3S,PCGFCFG3S and PDGFCFG3S are four 32-bit PORT glitch filter control bit 3 set registers.

	PxGFCFG3S																															Base + 0x00A4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG3S31	GFCFG3S30	GFCFG3S29	GFCFG3S28	GFCFG3S27	GFCFG3S26	GFCFG3S25	GFCFG3S24	GFCFG3S23	GFCFG3S22	GFCFG3S21	GFCFG3S20	GFCFG3S19	GFCFG3S18	GFCFG3S17	GFCFG3S16	GFCFG3S15	GFCFG3S14	GFCFG3S13	GFCFG3S12	GFCFG3S11	GFCFG3S10	GFCFG3S09	GFCFG3S08	GFCFG3S07	GFCFG3S06	GFCFG3S05	GFCFG3S04	GFCFG3S03	GFCFG3S02	GFCFG3S01	GFCFG3S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG3S n	Writing 1 to GFCFG3S n will set glitch filter control signal GFCFG3 n to 0 in register PBGFCFG3. Writing 0 to GFCFG3S n will no use.	W

21.4.1.27 PORT GLITCH FILTER Configure Clear Register 3 (PxGFCFG3C,0x00A8)

PAGFCFG3C,PBGFCFG3C,PCGFCFG3C and PDGFCFG3C are four 32-bit PORT glitch filter control bit 3 clear registers.

	PxGFCFG3C																															Base + 0x00A8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG3S31	GFCFG3S30	GFCFG3S29	GFCFG3S28	GFCFG3S27	GFCFG3S26	GFCFG3S25	GFCFG3S24	GFCFG3S23	GFCFG3S22	GFCFG3S21	GFCFG3S20	GFCFG3S19	GFCFG3S18	GFCFG3S17	GFCFG3S16	GFCFG3S15	GFCFG3S14	GFCFG3S13	GFCFG3S12	GFCFG3S11	GFCFG3S10	GFCFG3S09	GFCFG3S08	GFCFG3S07	GFCFG3S06	GFCFG3S05	GFCFG3S04	GFCFG3S03	GFCFG3S02	GFCFG3S01	GFCFG3S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG3C n	Writing 1 to GFCFG3C n will clear glitch filter control signal GFCFG3 n to 0 in register PBGFCFG3. Writing 0 to GFCFG3C n will no use.	W

These four registers used for suppress the glitch on port signal. The range of glitch width is:
1 x pclk ~ 15 x pclk

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<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>R/W</th></tr>
<tr><td>4</td><td>GFCFGn</td><td>Glitch Filter Configure Register for each PBD, digital filter which mask upto 15 pclk cycle's unstable input signal
<table>
<tr><th>GFCFG3</th><th>GFCFG2</th><th>GFCFG1</th><th>GFCFG0</th><th>Drive Strength Level</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>(disable)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1 pclk</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>2 pclk</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>..</td><td>..</td><td>..</td><td>..</td><td>..</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>14</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>15 pclk</td></tr>
</table>
Note:
1. not each PBd supports Glitch Filter Function</td><td>RW</td></tr>
</table>

Note:

1. pclk is the clock period configure to APB bus.
2. This function only used in interrupt input mode.
3. Not every bit for each port is implement this function. please refer *1.1,* only bits marked with "*13*" has this function.

21.4.1.28 PORTA VDDIO-SEL Register (PAVDDIO,0x0100)

PORTA generator pad vref/poc/hvps register.

	PAVDDIO																															0x0100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												Vddio_sel3	Vddio_sel2	Vddio_sel1	Vddio_sel0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
31:4	Reserved	Writing has no effect, Read as zero	R
3	vddio_sel[3]	control sel25 port of SPP_RE_SVR_182533V for generator I/O domain **voltage 1(PA23~PA31/PB/PC/PD)** VREFN/P ; 0: sel25 =0 ,I/O domain voltage 1 =1.8/2.8/3.0/3.3V; 1: sel25 =1 ,I/O domain voltage 1=2.5V;	RW
2	vddio_sel[2]	control sel25 port of SPP_RE_SVR_182533V for generator I/O domain **voltage 0(PA00~PA22)** VREFN/P ;	RW

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		0: sel25 =0 ,I/O domain **voltage 0** =1.8/2.8/3.0/3.3V; 1: sel25 =1 ,I/O domain **voltage 0** =2.5V;	
1	vddio_sel[1]	control sel18 port of SPP_SP_POC_1833V for generator I/O domain **voltage 1(PA23~PA31/PB/PC/PD)** POC_N/P ,HVPS_N/P ; 0: sel18 =0 ,I/O domain voltage 1 >=2.5V; 1: sel18 =1 ,I/O domain voltage 1<=1.8V;	RW
0	vddio_sel[0]	control sel18 port of SPP_SP_POC_1833V for generator I/O domain **voltage 0(PA00~PA22)** POC_N/P ,HVPS_N/P ; 0: sel18 =0 ,I/O domain **voltage 0** >=2.5V; 1: sel18 =1 ,I/O domain **voltage 0**<=1.8V;	RW

21.4.1.29 PORTA VDDIO-SEL Set Register (PAVDDIOS,0x0104)

PORTA GROUP generator pad vref/poc/hvps set register, WRITE-ONLY.

	PAVDDIOS																																0x0104
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												Vddio_sels3	Vddio_sels2	Vddio_sels1	Vddio_sels0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:4	Reserved	Writing has no effect, Read as zero	R
3:0	VDDIOS n	Writing 1 to VDDIOS n will set VDDIO n to 1 in register PAVDDIOn. Writing 0 to VDDIOS n will be ignored.	W

21.4.1.30 PORTA VDDIO-SEL Clear Register (PAVDDIOC,0x0108)

PORTA GROUP generator pad vref/poc/hvps clear register, WRITE-ONLY.

	PAVDDIOC																																0x0108
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												Vddio_selc3	Vddio_selc2	Vddio_selc1	Vddio_selc0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:4	Reserved	Writing has no effect, Read as zero	R
3:0	VDDIOC n	Writing 1 to VDDIOC n will set VDDIO n to 1 in register PAVDDIOn.	W

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		Writing 0 to VDDIOC n will be ignored.	

21.4.1.31 PORT Driver Disabled State Register0 (PxPEL,0x0110)

PORT x GROUP driver disabled state register0.

	PxPEL																															0x0110
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PEL15		PEL14		PEL13		PEL12		PEL11		PEL10		PEL09		PEL08		PEL07		PEL06		PEL05		PEL04		PEL03		PEL02		PEL01		PEL00	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PELn	Where n = 0 ~ 15 and PEL n[1:0] = PEL[2n+1 : 2n]. PEL[2n+1: 2n] is used to control state of the corresponding PxPEL[2n+1 : 2n],which it's output has been disabled. 00: Hi-Z 01: Pull-up 10: Pull-down 11: Repeater	RW

21.4.1.32 PORT Driver Disabled State Set Register0 (PxPELS,0x0114)

PORT x GROUP driver disabled state set register0, WRITE-ONLY.

	PxPELS																															0x0114
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PELS15		PELS14		PELS13		PELS12		PELS11		PELS10		PELS09		PELS08		PELS07		PELS06		PELS05		PELS04		PELS03		PELS02		PELS01		PELS00	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PELS n	Writing 1 to PELSn[0] will set PELn[0] to 1 in register PxPELS. Writing 1 to PELSn[1] will set PELn[1] to 1 in register PxPELS. Writing 0 to PELS n will be ignored.	W

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21.4.1.33 PORT Driver Disabled State Clear Register0 (PxPELC,0x0118)

PORT x GROUP driver disabled state clear register0, WRITE-ONLY.

	PxPELC																															0x0118
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PELC15		PELC14		PELC13		PELC12		PELC11		PELC10		PELC09		PELC08		PELC07		PELC06		PELC05		PELC04		PELC03		PELC02		PELC01		PELC00	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PELC n	Writing 1 to PELCn[0] will set PELn[0] to 0 in register PxPELC. Writing 1 to PELCn[1] will set PELn[1] to 0 in register PxPELC. Writing 0 to PELC n will be ignored.	W

21.4.1.34 PORT Driver Disabled State Register1 (PxPEH,0x0120)

PORT x GROUP driver disabled state register1.

	PxPEH																															0x0120
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PEH31		PEH30		PEH29		PEH28		PEH27		PEH26		PEH25		PEH24		PEH23		PEH22		PEH21		PEH20		PEH19		PEH18		PEH17		PEH16	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PEHn	Where n = 0 ~ 15 and PEH(n+16)[1:0] = PEH[2n+1 : 2n]. PEH[2n+1 : 2n] is used to control state of the corresponding PxPEH[2n+1 : 2n],which it's output has been disabled. 00: Hi-Z 01: Pull-up 10: Pull-down 11: Repeater	RW

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21.4.1.35 PORT Driver Disabled State Set Register1 (PxPEHS,0x0124)

PORT x GROUP driver disabled state set register1, WRITE-ONLY.

	PxPEHS																															0x0124
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PEHS31		PEHS30		PEHS29		PEHS28		PEHS27		PEHS26		PEHS25		PEHS24		PEHS23		PEHS22		PEHS21		PEHS20		PEHS19		PEHS18		PEHS17		PEHS16	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PEHS n	Writing 1 to PEHSn[0] will set PEHn[0] to 1 in register PxPEHS. Writing 1 to PEHSn[1] will set PEHn[1] to 1 in register PxPEHS. Writing 0 to PEHS n will be ignored.	W

21.4.1.36 PORT Driver Disabled State Clear Register1 (PxPEHC,0x0128)

PORT x GROUP driver disabled state clear register1, WRITE-ONLY.

	PxPEHC																															0x0128
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PEHC31		PEHC30		PEHC29		PEHC28		PEHC27		PEHC26		PEHC25		PEHC24		PEHC23		PEHC22		PEHC21		PEHC20		PEHC19		PEHC18		PEHC17		PELC16	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PEHC n	Writing 1 to PEHCn[0] will set PEHn[0] to 0 in register PxPEHC. Writing 1 to PEHCn[1] will set PEHn[1] to 0 in register PxPEHC. Writing 0 to PEHC n will be ignored.	W

21.4.1.37 PORT Drive Strength Register0 (PxDSL,0x0130)

PORT x GROUP Drive Strength register0.

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	PxDSL																															0x0130
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSL15		DSL14		DSL13		DSL12		DSL11		DSL10		DSL09		DSL08		DSL07		DSL06		DSL05		DSL04		DSL03		DSL02		DSL01		DSL00	
RST	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	DSLn	Where n = 0 ~ 15 and DSLn[1:0] = DSL[2n+1 : 2n]. DSL[2n+1 : 2n] is used to select drive strength of the corresponding PxDSL[2n+1 : 2n]. 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW

21.4.1.38 PORT Drive Strength Set Register0 (PxDSLS,0x0134)

PORT x GROUP Drive Strength set register0, WRITE-ONLY.

	PxDSLS																															0x0134
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSLS15		DSLS14		DSLS13		DSLS12		DSLS11		DSLS10		DSLS09		DSLS08		DSLS07		DSLS06		DSLS05		DSLS04		DSLS03		DSLS02		DSLS01		DSLS00	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DSLS n	Writing 1 to DSLSn[0] will set DSLn[0] to 1 in register PxDSLS. Writing 1 to DSLSn[1] will set DSLn[1] to 1 in register PxDSLS. Writing 0 to DSLS n will be ignored.	W

21.4.1.39 PORT Drive Strength Clear Register0 (PxDSLC,0x0138)

PORT x GROUP Drive Strength clear register0, WRITE-ONLY.

	PxDSLC																															0x0138
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	DSLC15		DSLC14		DSLC13		DSLC12		DSLC11		DSLC10		DSLC09		DSLC08		DSLC07		DSLC06		DSLC05		DSLC04		DSLC03		DSLC02		DSLC01		DSLC00	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DSLC n	Writing 1 to DSLCn[0] will set DSLn[0] to 0 in register PxDSLC. Writing 1 to DSLCn[1] will set DSLn[1] to 0 in register PxDSLC. Writing 0 to DSLC n will be ignored.	W

21.4.1.40 PORT Drive Strength Register1 (PxDSH,0x0140)

PORT x GROUP Drive Strength register1.

	PxDSH																															**0x0140**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSH31		DSH30		DSH29		DSH28		DSH27		DSH26		DSH25		DSH24		DSH23		DSH22		DSH21		DSH20		DSH19		DSH18		DSH17		DSH16	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	DSHn	Where n = 0 ~ 15 and DSH(n+16) = DSH[2n+1 : 2n]. DSH[2n+1 : 2n]is used to select drive strength of the corresponding PxDSH[2n+1 : 2n]. 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW

21.4.1.41 PORT Drive Strength Set Register1 (PxDSHS,0x0144)

PORT x GROUP Drive Strength set register1, WRITE-ONLY.

	PxDSHS																															**0x0144**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSHS31		DSHS30		DSHS29		DSHS28		DSHS27		DSHS26		DSHS25		DSHS24		DSHS23		DSHS22		DSHS21		DSHS20		DSHS19		DSHS18		DSHS17		DSHS16	

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RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DSHS n	Writing 1 to DSHSn[0] will set DSHn[0] to 1 in register PxDSHS. Writing 1 to DSHSn[1] will set DSHn[1] to 1 in register PxDSHS. Writing 0 to DSHS n will be ignored.	W

21.4.1.42 PORT Drive Strength Clear Register1 (PxDSHC,0x0148)

PORT x GROUP Drive Strength clear register1, WRITE-ONLY.

	PxDSHC																															**0x0148**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSHC31		DSHC30		DSHC29		DSHC28		DSHC27		DSHC26		DSHC25		DSHC24		DSHC23		DSHC22		DSHC21		DSHC20		DSHC19		DSHC18		DSHC17		DSHC16	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DSHC n	Writing 1 to DSHCn[0] will set DSHn[0] to 0 in register PxDSHC. Writing 1 to DSHSn[1] will set DSHn[1] to 1 in register PxDSHS. Writing 0 to DSHCn will be ignored.	W

21.4.1.43 PORT Slew Rate Register (PxSR,0x0150)

PORT x GROUP slew rate register.

	PxSR																															**0x0150**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SR31	SR30	SR29	SR28	SR27	SR26	SR25	SR24	SR23	SR22	SR21	SR20	SR19	SR18	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10	SR09	SR08	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	SR n	Where n = 0 ~ 31 and SR n = SR0 ~ SR31.	RW

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		SR n is used to switch slew rate of the corresponding PxSRn. 0: slow(half frequency) 1: fast	

21.4.1.44 PORT Slew Rate Set Register (PxSRS,0x0154)

PORT x GROUP slew rate set register, WRITE-ONLY.

	PxSRS																															0x0154
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRS31	SRS30	SRS29	SRS28	SRS27	SRS26	SRS25	SRS24	SRS23	SRS22	SRS21	SRS20	SRS19	SRS18	SRS17	SRS16	SRS15	SRS14	SRS13	SRS12	SRS11	SRS10	SRS09	SRS08	SRS07	SRS06	SRS05	SRS04	SRS03	SRS02	SRS01	SRS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SRS n	Writing 1 to SRS n will set SR n to 1 in register PxSRS. Writing 0 to SRS n will be ignored.	W

21.4.1.45 PORT Slew Rate Clear Register (PxSRC,0x0158)

PORT x GROUP slew rate clear register, WRITE-ONLY.

	PxSRC																															0x0158
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRC31	SRC30	SRC29	SRC28	SRC27	SRC26	SRC25	SRC24	SRC23	SRC22	SRC21	SRC20	SRC19	SRC18	SRC17	SRC16	SRC15	SRC14	SRC13	SRC12	SRC11	SRC10	SRC09	SRC08	SRC07	SRC06	SRC05	SRC04	SRC03	SRC02	SRC01	SRC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SRC n	Writing 1 to SRC n will set SR n to 0 in register PxSRC. Writing 0 to SRC n will be ignored.	W

21.4.1.46 PORT Schmitt Trigger Register (PxSMT,0x0160)

PORT x GROUP schmitt trigger register.

	PxSMT																															0x0160
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	SMT31	SMT30	SMT29	SMT28	SMT27	SMT26	SMT25	SMT24	SMT23	SMT22	SMT21	SMT30	SMT19	SMT18	SMT17	SMT16	SMT15	SMT14	SMT13	SMT12	SMT11	SMT10	SMT09	SMT08	SMT07	SMT06	SMT05	SMT04	SMT03	SMT02	SMT01	SMT00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	SMT n	Where n = 0 ~ 31 and SMT n = SMT0 ~ SMT31. SMT n is used to enable schmitt trigger of the corresponding PxSMTn. 0: schmitt trigger disabled 1: schmitt trigger enabled	RW

21.4.1.47 PORT Schmitt Trigger Set Register (PxSMTS,0x0164)

PORT x GROUP schmitt trigger set register, WRITE-ONLY.

	PxSMTS																															**0x0164**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SMTS31	SMTS30	SMTS29	SMTS28	SMTS27	SMTS26	SMTS25	SMTS24	SMTS23	SMTS22	SMTS21	SMTS20	SMTS19	SMTS18	SMTS17	SMTS16	SMTS15	SMTS14	SMTS13	SMTS12	SMTS11	SMTS10	SMTS09	SMTS08	SMTS07	SMTS06	SMTS05	SMTS04	SMTS03	SMTS02	SMTS01	SMTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SMTS n	Writing 1 to SMTS n will set SMT n to 1 in register PxSMTS. Writing 0 to SMTS n will be ignored.	W

21.4.1.48 PORT Schmitt Trigger Clear Register (PxSMTC,0x0168)

PORT x GROUP schmitt trigger clear register, WRITE-ONLY.

	PxSMTC																															**0x0168**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SMTC31	SMTC30	SMTC29	SMTC28	SMTC27	SMTC26	SMTC25	SMTC24	SMTC23	SMTC22	SMTC21	SMTC20	SMTC19	SMTC18	SMTC17	SMTC16	SMTC15	SMTC14	SMTC13	SMTC12	SMTC11	SMTC10	SMTC09	SMTC08	SMTC07	SMTC06	SMTC05	SMTC04	SMTC03	SMTC02	SMTC01	SMTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W

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31:0	SMTC n	Writing 1 to SMTC n will set SMT n to 0 in register PxSMTC. Writing 0 to SMTC n will be ignored.	W

21.4.1.49 PORT Receiver Enable State Register (PxIE,0x0180)

PORT x GROUP receiver enable register.

	PxIE																															0x0180
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IE31	IE30	IE29	IE28	IE27	IE26	IE25	IE24	IE23	IE22	IE21	IE30	IE19	IE18	IE17	IE16	IE15	IE14	IE13	IE12	IE11	IE10	IE09	IE08	IE07	IE06	IE05	IE04	IE03	IE02	IE01	IE00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	IE n	Where n = 0 ~ 31 and IE n = IE0 ~ IE31. IE n is used to enable receiver enable of the corresponding PxIEn. 0: receiver enable disabled 1: receiver enable enabled	RW

21.4.1.50 PORT Receiver Enable State Set Register (PxIES,0x0184)

PORT x GROUP receiver enable set register, WRITE-ONLY.

	PxIES																															0x0184
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IES31	IES30	IES29	IES28	IES27	IES26	IES25	IES24	IES23	IES22	IES21	IES20	IES19	IES18	IES17	IES16	IES15	IES14	IES13	IES12	IES11	IES10	IES09	IES08	IES07	IES06	IES05	IES04	IES03	IES02	IES01	IES00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	IES n	Writing 1 to IES n will set IE n to 1 in register PxIES. Writing 0 to IES n will be ignored.	W

21.4.1.51 PORT Receiver Enable State Clear Register (PxIEC,0x0188)

PORT x GROUP receiver enable clear register, WRITE-ONLY.

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	PxIEC																															0x0188
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC09	IEC08	IEC07	IEC06	IEC05	IEC04	IEC03	IEC02	IEC01	IEC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	IEC n	Writing 1 to IEC n will set IE n to 0 in register PxIEC. Writing 0 to IEC n will be ignored.	W

21.4.1.52 PORT Z Shadow Register Group

PORT Z group only have eight registers, PZINTS,PZINTC,PZMSKS,PZMSKC,PZPAT1S,PZPAT1C, PZPAT0S,PZPAT0C. those registers shadow as same as other group registers function which the offset address equal.

	PZINTS																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTS31	INTS30	INTS29	INTS28	INTS27	INTS26	INTS25	INTS24	INTS23	INTS22	INTS21	INTS20	INTS19	INTS18	INTS17	INTS16	INTS15	INTS14	INTS13	INTS12	INTS11	INTS10	INTS09	INTS08	INTS07	INTS06	INTS05	INTS04	INTS03	INTS02	INTS01	INTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZINTC																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC31	INTC30	INTC29	INTC28	INTC27	INTC26	INTC25	INTC24	INTC23	INTC22	INTC21	INTC20	INTC19	INTC18	INTC17	INTC16	INTC15	INTC14	INTC13	INTC12	INTC11	INTC10	INTC09	INTC08	INTC07	INTC06	INTC05	INTC04	INTC03	INTC02	INTC01	INTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZMSKS																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKS31	MSKS30	MSKS29	MSKS28	MSKS27	MSKS26	MSKS25	MSKS24	MSKS23	MSKS22	MSKS21	MSKS20	MSKS19	MSKS18	MSKS17	MSKS16	MSKS15	MSKS14	MSKS13	MSKS12	MSKS11	MSKS10	MSKS09	MSKS08	MSKS07	MSKS06	MSKS05	MSKS04	MSKS03	MSKS02	MSKS01	MSKS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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	PZMSKC																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKC31	MSKC30	MSKC29	MSKC28	MSKC27	MSKC26	MSKC25	MSKC24	MSKC23	MSKC22	MSKC21	MSKC20	MSKC19	MSKC18	MSKC17	MSKC16	MSKC15	MSKC14	MSKC13	MSKC12	MSKC11	MSKC10	MSKC09	MSKC08	MSKC07	MSKC06	MSKC05	MSKC04	MSKC03	MSKC02	MSKC01	MSKC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT1S																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1S31	PAT1S30	PAT1S29	PAT1S28	PAT1S27	PAT1S26	PAT1S25	PAT1S24	PAT1S23	PAT1S22	PAT1S21	PAT1S20	PAT1S19	PAT1S18	PAT1S17	PAT1S16	PAT1S15	PAT1S14	PAT1S13	PAT1S12	PAT1S11	PAT1S10	PAT1S09	PAT1S08	PAT1S07	PAT1S06	PAT1S05	PAT1S04	PAT1S03	PAT1S02	PAT1S01	PAT1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT1S																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1C31	PAT1C30	PAT1C29	PAT1C28	PAT1C27	PAT1C26	PAT1C25	PAT1C24	PAT1C23	PAT1C22	PAT1C21	PAT1C20	PAT1C19	PAT1C18	PAT1C17	PAT1C16	PAT1C15	PAT1C14	PAT1C13	PAT1C12	PAT1C11	PAT1C10	PAT1C09	PAT1C08	PAT1C07	PAT1C06	PAT1C05	PAT1C04	PAT1C03	PAT1C02	PAT1C01	PAT1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT0S																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0S31	PAT0S30	PAT0S29	PAT0S28	PAT0S27	PAT0S26	PAT0S25	PAT0S24	PAT0S23	PAT0S22	PAT0S21	PAT0S20	PAT0S19	PAT0S18	PAT0S17	PAT0S16	PAT0S15	PAT0S14	PAT0S13	PAT0S12	PAT0S11	PAT0S10	PAT0S09	PAT0S08	PAT0S07	PAT0S06	PAT0S05	PAT0S04	PAT0S03	PAT0S02	PAT0S01	PAT0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT0C																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	PAT0C31	PAT0C30	PAT0C29	PAT0C28	PAT0C27	PAT0C26	PAT0C25	PAT0C24	PAT0C23	PAT0C22	PAT0C21	PAT0C20	PAT0C19	PAT0C18	PAT0C17	PAT0C16	PAT0C15	PAT0C14	PAT0C13	PAT0C12	PAT0C11	PAT0C10	PAT0C09	PAT0C08	PAT0C07	PAT0C06	PAT0C05	PAT0C04	PAT0C03	PAT0C02	PAT0C01	PAT0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

21.4.1.53 GPIOZ Group ID to Load Register (PzGID2LD,0x00F0)

This register controls which Port Group to be load from GPIOZ.

	PzGID2LD																															**Base + 0x00F0**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													GPID		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOZ Group can shadow four register groups for GPIO Group A to D, when set or clear A to D register groups below four types, it will through shadow register to implement. the GPIOZ ID used for controls which Group to be manipulate.

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, Read as zero	R
2:0	GPID	GPIO Port ID load control register, according the values of GPID to load Shadow register group to the same offset address of group ID meet the GPID. GPID: Shadow register load to work groups 0: Load to GPIO Port A 1: Load to GPIO Port B 2: Load to GPIO Port C 3: Load to GPIO Port D 4: Undefine 5: Undefine	W

6) summarized all memory-mapped registers, which can be programmed to operate GPIO port and alternate function port sharing configuration.
7) All registers are in 32-bits width. Usually, 1 bit in the register affects a corresponding GPIO port and every GPIO port can be operated independently.
8) Gray bits in the register description indicates that this feature in the GPIO group who did not use, program can be ignored.

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21.4.2 Register Memory Map

Table 21-6 Registers Memory Map-Address Base

Name	Base	Description
PA	0x10010000	Address base of GPIO Port A
PB	0x10011000	Address base of GPIO Port B
PC	0x10012000	Address base of GPIO Port C
PD	0x10013000	Address base of GPIO Port D
PZ	0x10017000	Address base of GPIO Group Z (Shadow group)

Table 21-7 GPIO Registers Group Map

Name	RW	Description	Reset Value	Address Offset	Access Size
GPIO PORT A					
PAPINL	R	PORTA PIN Level Register	0x????_????	0x0000	32
PAINT	RW	PORTA Interrupt Register	0x0000_0000	0x0010	32
PAINTS	W	PORTA Interrupt Set Register	0x0000_0000	0x0014	32
PAINTC	W	PORTA Interrupt Clear Register	0x0000_0000	0x0018	32
PAMSK	RW	PORTA Interrupt Mask Register	0x1FDF_FFFF	0x0020	32
PAMSKS	W	PORTA Interrupt Mask Set Register	0x0000_0000	0x0024	32
PAMSKC	W	PORTA Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PAPAT1	RW	PORTA Pattern 1 Register	0x1FDF_FFFF	0x0030	32
PAPAT1S	W	PORTA Pattern 1 Set Register	0x0000_0000	0x0034	32
PAPAT1C	W	PORTA Pattern 1 Clear Register	0x0000_0000	0x0038	32
PAPAT0	RW	PORTA Pattern 0 Register	0x0000_0000	0x0040	32
PAPAT0S	W	PORTA Pattern 0 Set Register	0x0000_0000	0x0044	32
PAPAT0C	W	PORTA Pattern 0 Clear Register	0x0000_0000	0x0048	32
PAFLG	R	PORTA FLAG Register	0x0000_0000	0x0050	32
PAFLGC	RC	PORTA FLAG Clear Register	0x0000_0000	0x0058	32
PAGFCFG0	RW	PORTA Glitch Filter Configure 0	0x0000_0000	0x0070	32
PAGFCFG0S	W	PORTA Glitch Filter Configure 0 Set	0x0000_0000	0x0074	32
PAGFCFG0C	W	PORTA Glitch Filter Configure 0 Clear	0x0000_0000	0x0078	32
PAGFCFG1	RW	PORTA Glitch Filter Configure 1	0x0000_0000	0x0080	32
PAGFCFG1S	W	PORTA Glitch Filter Configure 1 Set	0x0000_0000	0x0084	32
PAGFCFG1C	W	PORTA Glitch Filter Configure 1 Clear	0x0000_0000	0x0088	32
PAGFCFG2	RW	PORTA Glitch Filter Configure 2	0x0000_0000	0x0090	32
PAGFCFG2S	W	PORTA Glitch Filter Configure 2 Set	0x0000_0000	0x0094	32
PAGFCFG2C	W	PORTA Glitch Filter Configure 2 Clear	0x0000_0000	0x0098	32
PAGFCFG3	RW	PORTA Glitch Filter Configure 3	0x0000_0000	0x00A0	32
PAGFCFG3S	W	PORTA Glitch Filter Configure 3 Set	0x0000_0000	0x00A4	32

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PAGFCFG3C	W	PORTA Glitch Filter Configure 3 Clear	0x0000_0000	0x00A8	32
PAVDDIO	RW	PORTA VDDIO-SEL Register	0x0000_0001	0x0100	32
PAVDDIOS	W	PORT A VDDIO-SEL Set Register	0x0000_0000	0x0104	32
PAVDDIOC	W	PORTA VDDIO-SEL Clear Register	0x0000_0000	0x0108	32
PAPEL	RW	PORTA Driver Disabled State Register0	0x0540_0000	0x0110	32
PAPELS	W	PORTA Driver Disabled State Set Register0	0x0000_0000	0x0114	32
PAPELC	W	PORTA Driver Disabled State Clear Register0	0x0000_0000	0x0118	32
PAPEH	RW	PORTA Driver Disabled State Register1	0x0155_5000	0x0120	32
PAPEHS	W	PORTA Driver Disabled State Set Register1	0x0000_0000	0x0124	32
PAPEHC	W	PORTA Driver Disabled State Clear Register1	0x0000_0000	0x0128	32
PADSL	RW	PORTA Drive Strength Register0	0xAAAA_AAAA	0x0130	32
PADSLS	W	PORTA Drive Strength Set Register0	0x0000_0000	0x0134	32
PADSLC	W	PORTA Drive Strength Clear Register0	0x0000_0000	0x0138	32
PADSH	RW	PORTA Drive Strength Register1	0x02AA_A2AA	0x0140	32
PADSHS	W	PORTA Drive Strength Set Register1	0x0000_0000	0x0144	32
PADSHC	W	PORTA Drive Strength Clear Register1	0x0000_0000	0x0148	32
PASR	RW	PORTA Slew Rate Register	0x1FDF_FFFF	0x0150	32
PASRS	W	PORTA Slew Rate Set Register	0x0000_0000	0x0154	32
PASRC	W	PORTA Slew Rate Clear Register	0x0000_0000	0x0158	32
PASMT	RW	PORTA Schmitt Trigger Register	0x0058_0000	0x0160	32
PASMTS	W	PORTA Schmitt Trigger Set Register	0x0000_0000	0x0164	32
PASMTC	W	PORTA Schmitt Trigger Clear Register	0x0000_0000	0x0168	32
PAIE	RW	PORTA Receiver enable state Register	0x1FDF_FFFF	0x0180	32
PAIES	W	PORTA Receiver enable state Set Register	0x0000_0000	0x0184	32
PAIEC	W	PORTA Receiver enable state Clear Register	0x0000_0000	0x0188	32
GPIO PORT B					
PBPINL	R	PORTB PIN Level Register	0x????_????	0x0000	32
PBINT	RW	PORTB Interrupt Register	0x0000_0000	0x0010	32
PBINTS	W	PORTB Interrupt Set Register	0x0000_0000	0x0014	32
PBINTC	W	PORTB Interrupt Clear Register	0x0000_0000	0x0018	32
PBMSK	RW	PORTB Interrupt Mask Register	0xFE37_EFFF	0x0020	32
PBMSKS	W	PORTB Interrupt Mask Set Register	0x0000_0000	0x0024	32
PBMSKC	W	PORTB Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PBPAT1	RW	PORTB Pattern 1 Register	0xFE37_EFFF	0x0030	32
PBPAT1S	W	PORTB Pattern 1 Set Register	0x0000_0000	0x0034	32
PBPAT1C	W	PORTB Pattern 1 Clear Register	0x0000_0000	0x0038	32

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PBPAT0	RW	PORTB Pattern 0 Register	0x01C8_0000	0x0040	32
PBPAT0S	W	PORTB Pattern 0 Set Register	0x0000_0000	0x0044	32
PBPAT0C	W	PORTB Pattern 0 Clear Register	0x0000_0000	0x0048	32
PBFLG	R	PORTB FLAG Register	0x0000_0000	0x0050	32
PBFLGC	RC	PORTB FLAG Clear Register	0x0000_0000	0x0058	32
PBGFCFG0	RW	PORTB Glitch Filter Configure 0	0x0000_0000	0x0070	32
PBGFCFG0S	W	PORTB Glitch Filter Configure 0 Set	0x0000_0000	0x0074	32
PBGFCFG0C	W	PORTB Glitch Filter Configure 0 Clear	0x0000_0000	0x0078	32
PBGFCFG1	RW	PORTB Glitch Filter Configure 1	0x0000_0000	0x0080	32
PBGFCFG1S	W	PORTB Glitch Filter Configure 1 Set	0x0000_0000	0x0084	32
PBGFCFG1C	W	PORTB Glitch Filter Configure 1 Clear	0x0000_0000	0x0088	32
PBGFCFG2	RW	PORTB Glitch Filter Configure 2	0x0000_0000	0x0090	32
PBGFCFG2S	W	PORTB Glitch Filter Configure 2 Set	0x0000_0000	0x0094	32
PBGFCFG2C	W	PORTB Glitch Filter Configure 2 Clear	0x0000_0000	0x0098	32
PBGFCFG3	RW	PORTB Glitch Filter Configure 3	0x0000_0000	0x00A0	32
PBGFCFG3S	W	PORTB Glitch Filter Configure 3 Set	0x0000_0000	0x00A4	32
PBGFCFG3C	W	PORTB Glitch Filter Configure 3 Clear	0x0000_0000	0x00A8	32
PBPEL	RW	PORTB Driver Disabled State Register0	0x0060_0000	0x0110	32
PBPELS	W	PORTB Driver Disabled State Set Register0	0x0000_0000	0x0114	32
PBPELC	W	PORTB Driver Disabled State Clear Register0	0x0000_0000	0x0118	32
PBPEH	RW	PORTB Driver Disabled State Register1	0x8015_0068	0x0120	32
PBPEHS	W	PORTB Driver Disabled State Set Register1	0x0000_0000	0x0124	32
PBPEHC	W	PORTB Driver Disabled State Clear Register1	0x0000_0000	0x0128	32
PBDSL	RW	PORTB Drive Strength Register0	0xA8AA_AAAA	0x0130	32
PBDSLS	W	PORTB Drive Strength Set Register0	0x0000_0000	0x0134	32
PBDSLC	W	PORTB Drive Strength Clear Register0	0x0000_0000	0x0138	32
PBDSH	RW	PORTB Drive Strength Register1	0xAAAA_AAAA	0x0140	32
PBDSHS	W	PORTB Drive Strength Set Register1	0x0000_0000	0x0144	32
PBDSHC	W	PORTB Drive Strength Clear Register1	0x0000_0000	0x0148	32
PBSR	RW	PORTB Slew Rate Register	0xFFFF_EFFF	0x0150	32
PBSRS	W	PORTB Slew Rate Set Register	0x0000_0000	0x0154	32
PBSRC	W	PORTB Slew Rate Clear Register	0x0000_0000	0x0158	32
PBSMT	RW	PORTB Schmitt Trigger Register	0x7800_0000	0x0160	32
PBSMTS	W	PORTB Schmitt Trigger Set Register	0x0000_0000	0x0164	32
PBSMTC	W	PORTB Schmitt Trigger Clear Register	0x0000_0000	0x0168	32
PBIE	RW	PORTB Receiver enable state Register	0xFFFF_EFFF	0x0180	32
PBIES	W	PORTB Receiver enable state Set Register	0x0000_0000	0x0184	32

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PBIEC	W	PORTB Receiver enable state Clear Register	0x0000_0000	0x0188	32
GPIO PORT C					
PCPINL	R	PORTC PIN Level Register	0x????_????	0x0000	32
PCINT	RW	PORTC Interrupt Register	0x0000_0000	0x0010	32
PCINTS	W	PORTC Interrupt Set Register	0x0000_0000	0x0014	32
PCINTC	W	PORTC Interrupt Clear Register	0x0000_0000	0x0018	32
PCMSK	RW	PORTC Interrupt Mask Register	0x01FF_FBFF	0x0020	32
PCMSKS	W	PORTC Interrupt Mask Set Register	0x0000_0000	0x0024	32
PCMSKC	W	PORTC Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PCPAT1	RW	PORTC Pattern 1 Register	0x01FF_FBFF	0x0030	32
PCPAT1S	W	PORTC Pattern 1 Set Register	0x0000_0000	0x0034	32
PCPAT1C	W	PORTC Pattern 1 Clear Register	0x0000_0000	0x0038	32
PCPAT0	RW	PORTC Pattern 0 Register	0x0000_0000	0x0040	32
PCPAT0S	W	PORTC Pattern 0 Set Register	0x0000_0000	0x0044	32
PCPAT0C	W	PORTC Pattern 0 Clear Register	0x0000_0000	0x0048	32
PCFLG	R	PORTC FLAG Register	0x0000_0000	0x0050	32
PCFLGC	RC	PORTC FLAG Clear Register	0x0000_0000	0x0058	32
PCGFCFG0	RW	PORTC Glitch Filter Configure 0	0x0000_0000	0x0070	32
PCGFCFG0S	W	PORTC Glitch Filter Configure 0 Set	0x0000_0000	0x0074	32
PCGFCFG0C	W	PORTC Glitch Filter Configure 0 Clear	0x0000_0000	0x0078	32
PCGFCFG1	RW	PORTC Glitch Filter Configure 1	0x0000_0000	0x0080	32
PCGFCFG1S	W	PORTC Glitch Filter Configure 1 Set	0x0000_0000	0x0084	32
PCGFCFG1C	W	PORTC Glitch Filter Configure 1 Clear	0x0000_0000	0x0088	32
PCGFCFG2	RW	PORTC Glitch Filter Configure 2	0x0000_0000	0x0090	32
PCGFCFG2S	W	PORTC Glitch Filter Configure 2 Set	0x0000_0000	0x0094	32
PCGFCFG2C	W	PORTC Glitch Filter Configure 2 Clear	0x0000_0000	0x0098	32
PCGFCFG3	RW	PORTC Glitch Filter Configure 3	0x0000_0000	0x00A0	32
PCGFCFG3S	W	PORTC Glitch Filter Configure 3 Set	0x0000_0000	0x00A4	32
PCGFCFG3C	W	PORTC Glitch Filter Configure 3 Clear	0x0000_0000	0x00A8	32
PCPEL	RW	PORTC Driver Disabled State Register0	0x000A_0009	0x0110	32
PCPELS	W	PORTC Driver Disabled State Set Register0	0x0000_0000	0x0114	32
PCPELC	W	PORTC Driver Disabled State Clear Register0	0x0000_0000	0x0118	32
PCPEH	RW	PORTC Driver Disabled State Register1	0x02A9_0001	0x0120	32
PCPEHS	W	PORTC Driver Disabled State Set Register1	0x0000_0000	0x0124	32
PCPEHC	W	PORTC Driver Disabled State Clear Register1	0x0000_0000	0x0128	32
PCDSL	RW	PORTC Drive Strength Register0	0xAA8A_AAAA	0x0130	32
PCDSLS	W	PORTC Drive Strength Set Register0	0x0000_0000	0x0134	32

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PCDSLC	W	PORTC Drive Strength Clear Register0	0x0000_0000	0x0138	32
PCDSH	RW	PORTC Drive Strength Register1	0x02AA_AAAA	0x0140	32
PCDSHS	W	PORTC Drive Strength Set Register1	0x0000_0000	0x0144	32
PCDSHC	W	PORTC Drive Strength Clear Register1	0x0000_0000	0x0148	32
PCSR	RW	PORTC Slew Rate Register	0x1FFF_FBFF	0x0150	32
PCSRS	W	PORTC Slew Rate Set Register	0x0000_0000	0x0154	32
PCSRC	W	PORTC Slew Rate Clear Register	0x0000_0000	0x0158	32
PCSMT	RW	PORTC Schmitt Trigger Register	0x0106_0300	0x0160	32
PCSMTS	W	PORTC Schmitt Trigger Set Register	0x0000_0000	0x0164	32
PCSMTC	W	PORTC Schmitt Trigger Clear Register	0x0000_0000	0x0168	32
PCIE	RW	PORTC Receiver enable state Register	0x1FFF_FBFF	0x0180	32
PCIES	W	PORTC Receiver enable state Set Register	0x0000_0000	0x0184	32
PCIEC	W	PORTC Receiver enable state Clear Register	0x0000_0000	0x0188	32
GPIO PORT D					
PDPINL	R	PORTD PIN Level Register	0x????_????	0x0000	32
PDINT	RW	PORTD Interrupt Register	0x0000_0000	0x0010	32
PDINTS	W	PORTD Interrupt Set Register	0x0000_0000	0x0014	32
PDINTC	W	PORTD Interrupt Clear Register	0x0000_0000	0x0018	32
PDMSK	RW	PORTD Interrupt Mask Register	0x0FCF_F3FC	0x0020	32
PDMSKS	W	PORTD Interrupt Mask Set Register	0x0000_0000	0x0024	32
PDMSKC	W	PORTD Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PDPAT1	RW	PORTD Pattern 1 Register	0x0FCF_F3FC	0x0030	32
PDPAT1S	W	PORTD Pattern 1 Set Register	0x0000_0000	0x0034	32
PDPAT1C	W	PORTD Pattern 1 Clear Register	0x0000_0000	0x0038	32
PDPAT0	RW	PORTD Pattern 0 Register	0x0000_0000	0x0040	32
PDPAT0S	W	PORTD Pattern 0 Set Register	0x0000_0000	0x0044	32
PDPAT0C	W	PORTD Pattern 0 Clear Register	0x0000_0000	0x0048	32
PDFLG	R	PORTD FLAG Register	0x0000_0000	0x0050	32
PDFLGC	RC	PORTD FLAG Clear Register	0x0000_0000	0x0058	32
PDGFCFG0	RW	PORTD Glitch Filter Configure 0	0x0000_0000	0x0070	32
PDGFCFG0S	W	PORTD Glitch Filter Configure 0 Set	0x0000_0000	0x0074	32
PDGFCFG0C	W	PORTD Glitch Filter Configure 0 Clear	0x0000_0000	0x0078	32
PDGFCFG1	RW	PORTD Glitch Filter Configure 1	0x0000_0000	0x0080	32
PDGFCFG1S	W	PORTD Glitch Filter Configure 1 Set	0x0000_0000	0x0084	32
PDGFCFG1C	W	PORTD Glitch Filter Configure 1 Clear	0x0000_0000	0x0088	32
PDGFCFG2	RW	PORTD Glitch Filter Configure 2	0x0000_0000	0x0090	32
PDGFCFG2S	W	PORTD Glitch Filter Configure 2 Set	0x0000_0000	0x0094	32
PDGFCFG2C	W	PORTD Glitch Filter Configure 2 Clear	0x0000_0000	0x0098	32
PDGFCFG3	RW	PORTD Glitch Filter Configure 3	0x0000_0000	0x00A0	32
PDGFCFG3S	W	PORTD Glitch Filter Configure 3 Set	0x0000_0000	0x00A4	32

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PDGFCFG3C	W	PORTD Glitch Filter Configure 3 Clear	0x0000_0000	0x00A8	32
PDPEL	RW	PORTD Driver Disabled State Register0	0x0000_4000	0x0110	32
PDPELS	W	PORTD Driver Disabled State Set Register0	0x0000_0000	0x0114	32
PDPELC	W	PORTD Driver Disabled State Clear Register0	0x0000_0000	0x0118	32
PDPEH	RW	PORTD Driver Disabled State Register1	0x0000_0010	0x0120	32
PDPEHS	W	PORTD Driver Disabled State Set Register1	0x0000_0000	0x0124	32
PDPEHC	W	PORTD Driver Disabled State Clear Register1	0x0000_0000	0x0128	32
PDDSL	RW	PORTD Drive Strength Register0	0xAA0A_AAA0	0x0130	32
PDDSLS	W	PORTD Drive Strength Set Register0	0x0000_0000	0x0134	32
PDDSLC	W	PORTD Drive Strength Clear Register0	0x0000_0000	0x0138	32
PDDSH	RW	PORTD Drive Strength Register1	0x00AA_A0AA	0x0140	32
PDDSHS	W	PORTD Drive Strength Set Register1	0x0000_0000	0x0144	32
PDDSHC	W	PORTD Drive Strength Clear Register1	0x0000_0000	0x0148	32
PDSR	RW	PORTD Slew Rate Register	0x0FCF_F3FC	0x0150	32
PDSRS	W	PORTD Slew Rate Set Register	0x0000_0000	0x0154	32
PDSRC	W	PORTD Slew Rate Clear Register	0x0000_0000	0x0158	32
PDSMT	RW	PORTD Schmitt Trigger Register	0x0000_0000	0x0160	32
PDSMTS	W	PORTD Schmitt Trigger Set Register	0x0000_0000	0x0164	32
PDSMTC	W	PORTD Schmitt Trigger Clear Register	0x0000_0000	0x0168	32
PDIE	RW	PORTD Receiver enable state Register	0x0FCF_F3FC	0x0180	32
PDIES	W	PORTD Receiver enable state Set Register	0x0000_0000	0x0184	32
PDIEC	W	PORTD Receiver enable state Clear Register	0x0000_0000	0x0188	32
Shadow Register Group PZ					
PzINTS	W	Shadow Interrupt Set Register	0x0000_0000	0x0014	32
PzINTC	W	Shadow Interrupt Clear Register	0x0000_0000	0x0018	32
PzMSKS	W	Shadow Interrupt Mask Set Register	0x0000_0000	0x0024	32
PzMSKC	W	Shadow Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PzPAT1S	W	Shadow Interrupt Pattern 1 Set Register	0x0000_0000	0x0034	32
PzPAT1C	W	Shadow Interrupt Pattern 1 Clear Register	0x0000_0000	0x0038	32
PzPAT0S	W	Shadow Interrupt Pattern 0 Set Register	0x0000_0000	0x0044	32
PzPAT0C	W	Shadow Interrupt Pattern 0 Clear Register	0x0000_0000	0x0048	32
PzGID2LD	W	PORT Group ID to be load from PZ Register	0x0000_0000	0x00F0	32

Note: 1. Pz**** in the description of register is use for shadow operation for other groups, more details will description as follow chapters.

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21.4.2.1 PORT PIN Level Registers (PxPINL,0x0000)

PAPINL,PBPINL,PCPINL and PDPINL are four 32-bit PORT PIN level registers. They are read-only registers.

	PxPINL																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PINL31	PINL30	PINL29	PINL28	PINL27	PINL26	PINL25	PINL24	PINL23	PINL22	PINL21	PINL20	PINL19	PINL18	PINL17	PINL16	PINL15	PINL14	PINL13	PINL12	PINL11	PINL10	PINL09	PINL08	PINL07	PINL06	PINL05	PINL04	PINL03	PINL02	PINL01	PINL00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PINL n	Where n = 0 ~ 31 and PBPINL n = PBPINL0 ~ PBPINL31. The PORTB PIN level can be read by reading PINL n bit in register PBPINL.	R

Note:

1. In the table, "x" represents the group A,B,C and D behind the description of similar.

21.4.2.2 PORT Interrupt Registers (PxINT,0x0010)

PAINT,PBINT,PCINT and PDINT are four 32-bit PORT interrupt registers.

	PxINT																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT31	INT30	INT29	INT28	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT30	INT19	INT18	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10	INT09	INT08	INT07	INT06	INT05	INT04	INT03	INT02	INT01	INT00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INT n	Where n = 0 ~ 31 and INT n = INT31 ~ INT00. Interrupt enable. 0: Corresponding pin is used as device functions or normal gpio 1: Corresponding pin is used as interrupt	RW

21.4.2.3 PORT Interrupt Set Registers (PxINTS,0x0014)

PAINTS,PBINTS,PCINTS and PDINTS are four 32-bit PORT interrupt set registers.

	PxINTS																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	INTS31	INTS30	INTS29	INTS28	INTS27	INTS26	INTS25	INTS24	INTS23	INTS22	INTS21	INTS20	INTS19	INTS18	INTS17	INTS16	INTS15	INTS14	INTS13	INTS12	INTS11	INTS10	INTS09	INTS08	INTS07	INTS06	INTS05	INTS04	INTS03	INTS02	INTS01	INTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INTS n	Writing 1 to INTS n will set INT n to 1 in register PBINT. Writing 0 to INTS n will no use.	W

21.4.2.4 PORT Interrupt Clear Registers (PxINTC,0x0018)

PAINTC,PBINTC,PCINTC and PDINTC are four 32-bit PORT interrupt clear registers.

	PxINTC																															**Base + 0x0018**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC31	INTC30	INTC29	INTC28	INTC27	INTC26	INTC25	INTC24	INTC23	INTC22	INTC21	INTC20	INTC19	INTC18	INTC17	INTC16	INTC15	INTC14	INTC13	INTC12	INTC11	INTC10	INTC09	INTC08	INTC07	INTC06	INTC05	INTC04	INTC03	INTC02	INTC01	INTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INTC n	Writing 1 to INTC n will set INT n to 0 in register PxINT. Writing 0 to INTC n will no use.	W

21.4.2.5 PORT Mask Registers (PxMSK,0x0020)

PAMSK,PBMSK,PCMSK and PDMSK are four 32-bit PORT mask registers.

	PxMSK																															**Base + 0x0020**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSK31	MSK30	MSK29	MSK28	MSK27	MSK26	MSK25	MSK24	MSK23	MSK22	MSK21	MSK20	MSK19	MSK18	MSK17	MSK16	MSK15	MSK14	MSK13	MSK12	MSK11	MSK10	MSK09	MSK08	MSK07	MSK06	MSK05	MSK04	MSK03	MSK02	MSK01	MSK00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W

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31:0	MSK n	Where n = 0 ~ 31 and MSK n = MSK31 ~ MSK0. When INT n = 1: 0: Enable the pin as an interrupt source 1: Disable the pin as an interrupt source When INT n = 0: 0: Corresponding pin will be used as device function 1: Corresponding pin will be used as gpio	RW

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.2.6 PORT Mask Set Registers (PxMSKS,0x0024)

PAMSKS,PBMSKS,PCMSKS and PDMSKS are four 32-bit PORT mask set registers.

	PxMSKS																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKS31	MSKS30	MSKS29	MSKS28	MSKS27	MSKS26	MSKS25	MSKS24	MSKS23	MSKS22	MSKS21	MSKS20	MSKS19	MSKS18	MSKS17	MSKS16	MSKS15	MSKS14	MSKS13	MSKS12	MSKS11	MSKS10	MSKS09	MSKS08	MSKS07	MSKS06	MSKS05	MSKS04	MSKS03	MSKS02	MSKS01	MSKS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	MSKS n	Writing 1 to MSKS n will set MSK n to 1 in register PBMSK. Writing 0 to MSKS n will no use.	W

21.4.2.7 PORT Mask Clear Registers (PxMSKC,0x0028)

PAMSKC,PBMSKC,PCMSKC and PDMSKC are four 32-bit PORT mask clear registers.

	PxMSKC																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKC31	MSKC30	MSKC29	MSKC28	MSKC27	MSKC26	MSKC25	MSKC24	MSKC23	MSKC22	MSKC21	MSKC20	MSKC19	MSKC18	MSKC17	MSKC16	MSKC15	MSKC14	MSKC13	MSKC12	MSKC11	MSKC10	MSKC09	MSKC08	MSKC07	MSKC06	MSKC05	MSKC04	MSKC03	MSKC02	MSKC01	MSKC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	MSKC n	Writing 1 to MSKC n will set MSK n to 0 in register PBMSK. Writing 0 to MSKC n will no use.	W

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21.4.2.8 PORT PAT1/Direction Registers (PxPAT1,0x0030)

PAPAT1,PBPAT1,PCPAT1 and PDPAT1 are four 32-bit PORT PAttern1/direction registers.

	PxPAT1																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT131	PAT130	PAT129	PAT128	PAT127	PAT126	PAT125	PAT124	PAT123	PAT122	PAT121	PAT120	PAT119	PAT118	PAT117	PAT116	PAT115	PAT114	PAT113	PAT112	PAT111	PAT110	PAT109	PAT108	PAT107	PAT106	PAT105	PAT104	PAT103	PAT102	PAT101	PAT100
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PAT1 n	Where n = 0 ~ 31 and PBPAT1 n = PAT131 ~ PAT10. When INT n = 1 (Interrupt function): 0: Level trigger interrupt 1: Edge trigger interrupt When INT n = 0 and MSK = 0 (Device function): 0: Corresponding pin is used as device 0 or device 1 function 1: Corresponding pin is used as device 2 or device 3 function When INT n = 0 and MSK = 0 (GPIO function): 0: Corresponding pin is used as gpio output 1: Corresponding pin is used as gpio input	RW

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.2.9 PORT PAT1/Direction Set Registers (PxPAT1S,0x0034)

PAPAT1S,PBPAT1S, PCPAT1S and PDPAT1S are four 32-bit PORT PATtern1 or direction set registers.

	PxPAT1S																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1S31	PAT1S30	PAT1S29	PAT1S28	PAT1S27	PAT1S26	PAT1S25	PAT1S24	PAT1S23	PAT1S22	PAT1S21	PAT1S20	PAT1S19	PAT1S18	PAT1S17	PAT1S16	PAT1S15	PAT1S14	PAT1S13	PAT1S12	PAT1S11	PAT1S10	PAT1S09	PAT1S08	PAT1S07	PAT1S06	PAT1S05	PAT1S04	PAT1S03	PAT1S02	PAT1S01	PAT1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT1S n	Writing 1 to PAT1S n will set PAT1 n to 1 in register PBPAT1. Writing 0 to PAT1S n will no use.	W

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21.4.2.10 PORT PAT1/Direction Clear Registers (PxPAT1C,0x0038)

PAPAT1C,PBPAT1C,PCPAT1C,PDPAT1C are four 32-bit PORT PATtern1 or direction clear registers.

	PxPAT1S,																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1C31	PAT1C30	PAT1C29	PAT1C28	PAT1C27	PAT1C26	PAT1C25	PAT1C24	PAT1C23	PAT1C22	PAT1C21	PAT1C20	PAT1C19	PAT1C18	PAT1C17	PAT1C16	PAT1C15	PAT1C14	PAT1C13	PAT1C12	PAT1C11	PAT1C10	PAT1C09	PAT1C08	PAT1C07	PAT1C06	PAT1C05	PAT1C04	PAT1C03	PAT1C02	PAT1C01	PAT1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT1C n	Writing 1 to PAT1C n will set PAT1 n to 0 in register PBPAT1. Writing 0 to PAT1C n will no use.	W

21.4.2.11 PORT PAT0/Data Registers (PxPAT0,0x0040)

PAPAT0,PBPAT0,PCPAT0 and PDPAT0 are four 32-bit PORT PATtern0 or data registers.

	PxPAT0,																															Base + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT031	PAT030	PAT029	PAT028	PAT027	PAT026	PAT025	PAT024	PAT023	PAT022	PAT021	PAT020	PAT019	PAT018	PAT017	PAT016	PAT015	PAT014	PAT013	PAT012	PAT011	PAT010	PAT009	PAT008	PAT007	PAT006	PAT005	PAT004	PAT003	PAT002	PAT001	PAT000
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PAT0 n	Where n = 0 ~ 31 and PAT0 n = PAT00 ~ PAT031. When INTn = 1 and PAT1 = 0: 0: Port is low level triggered interrupt input 1: Port is low high triggered interrupt input When INTn = 1 and PAT1 = 1: 0: Port is falling edge triggered interrupt input 1: Port is rising edge triggered interrupt input When INTn = 0 and MSK = 0 and PAT1 = 0: 0: Port is pin of device 0 1: Port is pin of device 1 When INTn = 0 and MSK = 0 and PAT1 = 1: 0: Port is pin of device 2 1: Port is pin of device 3 When INTn = 0 and MSK = 1 and PAT1 = 0:	RW

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		0: Port is GPIO output 0 1: Port is GPIO output 1	

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.2.12 PORT PAT0/Data Set Registers (PxPAT0S,0x0044)

PAPAT0S,PBPAT0S,PCPAT0S and PDPAT0S are four 32-bit PORT PATtern0 or data set registers.

	PxPAT0S																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0S31	PAT0S30	PAT0S29	PAT0S28	PAT0S27	PAT0S26	PAT0S25	PAT0S24	PAT0S23	PAT0S22	PAT0S21	PAT0S20	PAT0S19	PAT0S18	PAT0S17	PAT0S16	PAT0S15	PAT0S14	PAT0S13	PAT0S12	PAT0S11	PAT0S10	PAT0S09	PAT0S08	PAT0S07	PAT0S06	PAT0S05	PAT0S04	PAT0S03	PAT0S02	PAT0S01	PAT0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT0S n	Writing 1 to PBPAT0S n will set PAT0 n to 1 in register PBPAT0. Writing 0 to PBPAT0S n will no use.	W

21.4.2.13 PORT PAT0/Data Clear Registers (PxPAT0C,0x0048)

PAPAT0C,PBPAT0C,PCPAT0C and PDPAT0C are four 32-bit PORT PATtern 0 or data clear registers.

	PxPAT0C																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0C31	PAT0C30	PAT0C29	PAT0C28	PAT0C27	PAT0C26	PAT0C25	PAT0C24	PAT0C23	PAT0C22	PAT0C21	PAT0C20	PAT0C19	PAT0C18	PAT0C17	PAT0C16	PAT0C15	PAT0C14	PAT0C13	PAT0C12	PAT0C11	PAT0C10	PAT0C09	PAT0C08	PAT0C07	PAT0C06	PAT0C05	PAT0C04	PAT0C03	PAT0C02	PAT0C01	PAT0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT0C n	Writing 1 to PAT0C n will set PAT0 n to 0 in register PBPAT0. Writing 0 to PAT0C n will no use.	W

21.4.2.14 PORT FLAG Registers (PxFLG,0x0050)

PAFLG,PBFLG,PCFLG and PDFLG are four 32-bit PORT flag registers. They are read-only registers.

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	PxFLG																															Base + 0x0050
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAG31	FLAG30	FLAG29	FLAG28	FLAG27	FLAG26	FLAG25	FLAG24	FLAG23	FLAG22	FLAG21	FLAG20	FLAG19	FLAG18	FLAG17	FLAG16	FLAG15	FLAG14	FLAG13	FLAG12	FLAG11	FLAG10	FLAG09	FLAG08	FLAG07	FLAG06	FLAG05	FLAG04	FLAG03	FLAG02	FLAG01	FLAG00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	FLAG n	Where n = 0 ~ 31 and FLAG n = FLAG00 ~ FLAG31. FLAG n is interrupt flag bit for checking the interrupt whether to happen. When GPIO is used as interrupt function and the interrupt happened, the FLAG n in PBFLG will be set to 1.	R

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.2.15 PORT FLAG Clear Registers (PxFLGC,0x0058)

PAFLGC,PBFLGC,PCFLGC and PDFLGC are four 32-bit PORT flag clear registers. They are read-only registers.

	PxFLGC																															Base + 0x0058
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAGC31	FLAGC30	FLAGC29	FLAGC28	FLAGC27	FLAGC26	FLAGC25	FLAGC24	FLAGC23	FLAGC22	FLAGC21	FLAGC20	FLAGC19	FLAGC18	FLAGC17	FLAGC16	FLAGC15	FLAGC14	FLAGC13	FLAGC12	FLAGC11	FLAGC10	FLAGC09	FLAGC08	FLAGC07	FLAGC06	FLAGC05	FLAGC04	FLAGC03	FLAGC02	FLAGC01	FLAGC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	FLAGC n	When GPIO is used as interrupt function and when write 1 to the bit, the bit FLAG n in PBFLG will be cleared.	RC

21.4.2.16 PORT GLITCH FILTER Configure Register 0 (PxGFCFG0,0x0070)

PAGFCFG0,PBGFCFG0,PCGFCFG0 and PDGFCFG0 are four 32-bit PORT glitch filter control bit 0 registers.

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	PxGFCFG0																															Base + 0x0070
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG031	GFCFG030	GFCFG029	GFCFG028	GFCFG027	GFCFG026	GFCFG025	GFCFG024	GFCFG023	GFCFG022	GFCFG021	GFCFG020	GFCFG019	GFCFG018	GFCFG017	GFCFG016	GFCFG015	GFCFG014	GFCFG013	GFCFG012	GFCFG011	GFCFG010	GFCFG009	GFCFG008	GFCFG007	GFCFG006	GFCFG005	GFCFG004	GFCFG003	GFCFG002	GFCFG001	GFCFG000
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG0 n	Where n = 0 ~ 31 and GFCFG0 n = GFCFG00 ~ GFCFG031. GFCFG0 n is used for suppress the glitch filter on port signal bit 0 value . 0: glitch filter control signal bit 0 value is 0 1: glitch filter control signal bit 0 value is 1	RW

Note:

1. Not every PBD support glitch filter control, please check out Function Overview chapter for details.

21.4.2.17 PORT GLITCH FILTER Configure Set Register 0 (PxGFCFG0S,0x0074)

PAGFCFG0S,PBGFCFG0S,PCGFCFG0S and PDGFCFG0S are four 32-bit PORT glitch filter control bit 0 set registers.

	PxGFCFG0S																															Base + 0x0074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG0S31	GFCFG0S30	GFCFG0S29	GFCFG0S28	GFCFG0S27	GFCFG0S26	GFCFG0S25	GFCFG0S24	GFCFG0S23	GFCFG0S22	GFCFG0S21	GFCFG0S20	GFCFG0S19	GFCFG0S18	GFCFG0S17	GFCFG0S16	GFCFG0S15	GFCFG0S14	GFCFG0S13	GFCFG0S12	GFCFG0S11	GFCFG0S10	GFCFG0S09	GFCFG0S08	GFCFG0S07	GFCFG0S06	GFCFG0S05	GFCFG0S04	GFCFG0S03	GFCFG0S02	GFCFG0S01	GFCFG0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG0 S n	Writing 1 to GFCFG0S n will set glitch filter control signal GFCFG0 n to 0 in register PBGFCFG0. Writing 0 to GFCFG0S n will no use.	W

21.4.2.18 PORT GLITCH FILTER Configure Clear Register 0 (PxGFCFG0C,0x0078)

PAGFCFG0C,PBGFCFG0C,PCGFCFG0C and PDGFCFG0C are four 32-bit PORT glitch filter control bit 0 clear registers.

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	PxGFCFG0C																															Base + 0x0078
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG0C31	GFCFG0C30	GFCFG0C29	GFCFG0C28	GFCFG0C27	GFCFG0C26	GFCFG0C25	GFCFG0C24	GFCFG0C23	GFCFG0C22	GFCFG0C21	GFCFG0C20	GFCFG0C19	GFCFG0C18	GFCFG0C17	GFCFG0C16	GFCFG0C15	GFCFG0C14	GFCFG0C13	GFCFG0C12	GFCFG0C11	GFCFG0C10	GFCFG0C09	GFCFG0C08	GFCFG0C07	GFCFG0C06	GFCFG0C05	GFCFG0C04	GFCFG0C03	GFCFG0C02	GFCFG0C01	GFCFG0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG0C n	Writing 1 to GFCFG0C n will clear glitch filter control signal GFCFG0 n to 0 in register PxGFCFG0. Writing 0 to GFCFG0C n will no use.	W

21.4.2.19 PORT GLITCH FILTER Configure Register 1 (PxGFCFG1,0x0080)

PAGFCFG1,PBGFCFG1,PCGFCFG1 and PDGFCFG1 are four 32-bit PORT glitch filter control bit 1 registers.

	PxGFCFG1																															Base + 0x0080
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG131	GFCFG130	GFCFG129	GFCFG128	GFCFG127	GFCFG126	GFCFG125	GFCFG124	GFCFG123	GFCFG122	GFCFG121	GFCFG120	GFCFG119	GFCFG118	GFCFG117	GFCFG116	GFCFG115	GFCFG114	GFCFG113	GFCFG112	GFCFG111	GFCFG110	GFCFG109	GFCFG108	GFCFG107	GFCFG106	GFCFG105	GFCFG104	GFCFG103	GFCFG102	GFCFG101	GFCFG100
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG1 n	Where n = 0 ~ 31 and GFCFG1 n = GFCFG10 ~ GFCFG131. GFCFG1 n is used for suppress the glitch filter on port signal bit 1 value . 0: glitch filter control signal bit 1 value is 0 1: glitch filter control signal bit 1 value is 1	RW

Note:

1. Not every PBD support glitch filter control, please check out Function Overview chapter for details.

21.4.2.20 PORT GLITCH FILTER Configure Register 1 (PxGFCFG1S,0x0084)

PAGFCFG1S,PBGFCFG1S,PCGFCFG1S and PDGFCFG1S are four 32-bit PORT glitch filter control bit 1 set registers.

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	PxGFCFG1S																															Base + 0x0084
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG1S31	GFCFG1S30	GFCFG1S29	GFCFG1S28	GFCFG1S27	GFCFG1S26	GFCFG1S25	GFCFG1S24	GFCFG1S23	GFCFG1S22	GFCFG1S21	GFCFG1S20	GFCFG1S19	GFCFG1S18	GFCFG1S17	GFCFG1S16	GFCFG1S15	GFCFG1S14	GFCFG1S13	GFCFG1S12	GFCFG1S11	GFCFG1S10	GFCFG1S09	GFCFG1S08	GFCFG1S07	GFCFG1S06	GFCFG1S05	GFCFG1S04	GFCFG1S03	GFCFG1S02	GFCFG1S01	GFCFG1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG1S n	Writing 1 to GFCFG1S n will set glitch filter control signal GFCFG1 n to 0 in register PBGFCFG1. Writing 0 to GFCFG1S n will no use.	W

21.4.2.21 PORT GLITCH FILTER Configure Register 1 (PxGFCFG1C,0x0088)

PAGFCFG1C,PBGFCFG1C,PCGFCFG1C and PDGFCFG1C are four 32-bit PORT glitch filter control bit 1 clear registers.

	PxGFCFG1C																															Base + 0x0088
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG1C31	GFCFG1C30	GFCFG1C29	GFCFG1C28	GFCFG1C27	GFCFG1C26	GFCFG1C25	GFCFG1C24	GFCFG1C23	GFCFG1C22	GFCFG1C21	GFCFG1C20	GFCFG1C19	GFCFG1C18	GFCFG1C17	GFCFG1C16	GFCFG1C15	GFCFG1C14	GFCFG1C13	GFCFG1C12	GFCFG1C11	GFCFG1C10	GFCFG1C09	GFCFG1C08	GFCFG1C07	GFCFG1C06	GFCFG1C05	GFCFG1C04	GFCFG1C03	GFCFG1C02	GFCFG1C01	GFCFG1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG1C n	Writing 1 to GFCFG1C n will clear glitch filter control signal GFCFG1 n to 0 in register PBGFCFG1. Writing 0 to GFCFG1C n will no use.	W

21.4.2.22 PORT GLITCH FILTER Configure Register 2 (PxGFCFG2,0x0090)

PAGFCFG2,PBGFCFG2,PCGFCFG2 and PDGFCFG2 are four 32-bit PORT glitch filter control bit 2 registers.

	PxGFCFG2																															Base + 0x0090
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	GFCFG231	GFCFG230	GFCFG229	GFCFG228	GFCFG227	GFCFG226	GFCFG225	GFCFG224	GFCFG223	GFCFG222	GFCFG221	GFCFG220	GFCFG219	GFCFG218	GFCFG217	GFCFG216	GFCFG215	GFCFG214	GFCFG213	GFCFG212	GFCFG211	GFCFG210	GFCFG209	GFCFG208	GFCFG207	GFCFG206	GFCFG205	GFCFG204	GFCFG203	GFCFG202	GFCFG201	GFCFG200
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG2 n	Where n = 0 ~ 31 and GFCFG2 n = GFCFG20 ~ GFCFG231. GFCFG2 n is used for suppress the glitch filter on port signal bit 2 value . 0: glitch filter control signal bit 2 value is 0 1: glitch filter control signal bit 2 value is 1	RW

Note:

1. Not every PBD support Schmitt Trigger Control, please check out Function Overview chapter for details.

21.4.2.23 PORT GLITCH FILTER Configure Set Register 2 (PxGFCFG2S,0x0094)

PAGFCFG2S,PBGFCFG2S,PCGFCFG2S and PDGFCFG2S are four 32-bit PORT glitch filter control bit 2 set registers.

	PxGFCFG2S																															**Base + 0x0094**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG2S31	GFCFG2S30	GFCFG2S29	GFCFG2S28	GFCFG2S27	GFCFG2S26	GFCFG2S25	GFCFG2S24	GFCFG2S23	GFCFG2S22	GFCFG2S21	GFCFG2S20	GFCFG2S19	GFCFG2S18	GFCFG2S17	GFCFG2S16	GFCFG2S15	GFCFG2S14	GFCFG2S13	GFCFG2S12	GFCFG2S11	GFCFG2S10	GFCFG2S09	GFCFG2S08	GFCFG2S07	GFCFG2S06	GFCFG2S05	GFCFG2S04	GFCFG2S03	GFCFG2S02	GFCFG2S01	GFCFG2S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG2 S n	Writing 1 to GFCFG2S n will set glitch filter control signal GFCFG2 n to 0 in register PBGFCFG2. Writing 0 to GFCFG2S n will no use.	W

21.4.2.24 PORT GLITCH FILTER Configure Clear Register 2 (PxGFCFG2C,0x0098)

PAGFCFG2C,PBGFCFG2C,PCGFCFG2C and PDGFCFG2C are four 32-bit PORT glitch filter control bit 2 clear registers.

	PxGFCFG2C																															**Base + 0x0098**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	GFCFG2C31	GFCFG2C30	GFCFG2C29	GFCFG2C28	GFCFG2C27	GFCFG2C26	GFCFG2C25	GFCFG2C24	GFCFG2C23	GFCFG2C22	GFCFG2C21	GFCFG2C20	GFCFG2C19	GFCFG2C18	GFCFG2C17	GFCFG2C16	GFCFG2C15	GFCFG2C14	GFCFG2C13	GFCFG2C12	GFCFG2C11	GFCFG2C10	GFCFG2C09	GFCFG2C08	GFCFG2C07	GFCFG2C06	GFCFG2C05	GFCFG2C04	GFCFG2C03	GFCFG2C02	GFCFG2C01	GFCFG2C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG2C n	Writing 1 to GFCFG2C n will clear glitch filter control signal GFCFG2 n to 0 in register PBGFCFG2. Writing 0 to GFCFG2C n will no use.	W

21.4.2.25 PORT GLITCH FILTER Configure Register 3 (PxGFCFG3,0x00A0)

PAGFCFG3,PBGFCFG3,PCGFCFG3 and PDGFCFG3 are four 32-bit PORT glitch filter control bit 3 registers.

	PxGFCFG3																															**Base + 0x00A0**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG331	GFCFG330	GFCFG329	GFCFG328	GFCFG327	GFCFG326	GFCFG325	GFCFG324	GFCFG323	GFCFG322	GFCFG321	GFCFG320	GFCFG319	GFCFG318	GFCFG317	GFCFG316	GFCFG315	GFCFG314	GFCFG313	GFCFG312	GFCFG311	GFCFG310	GFCFG309	GFCFG308	GFCFG307	GFCFG306	GFCFG305	GFCFG304	GFCFG303	GFCFG302	GFCFG301	GFCFG300
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG3 n	Where n = 0 ~ 31 and GFCFG3 n = GFCFG30 ~ GFCFG331. GFCFG3 n is used for suppress the glitch filter on port signal bit 3 value . 0: glitch filter control signal bit 3 value is 0 1: glitch filter control signal bit 3 value is 1	RW

Note:

1. Not every PBD support glitch filter control, please check out Function Overview chapter for details.

21.4.2.26 PORT GLITCH FILTER Configure Set Register 3 (PxGFCFG3S,0x00A4)

PAGFCFG3S,PBGFCFG3S,PCGFCFG3S and PDGFCFG3S are four 32-bit PORT glitch filter control bit 3 set registers.

	PxGFCFG3S																															**Base + 0x00A4**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	GFCFG3S31	GFCFG3S30	GFCFG3S29	GFCFG3S28	GFCFG3S27	GFCFG3S26	GFCFG3S25	GFCFG3S24	GFCFG3S23	GFCFG3S22	GFCFG3S21	GFCFG3S20	GFCFG3S19	GFCFG3S18	GFCFG3S17	GFCFG3S16	GFCFG3S15	GFCFG3S14	GFCFG3S13	GFCFG3S12	GFCFG3S11	GFCFG3S10	GFCFG3S09	GFCFG3S08	GFCFG3S07	GFCFG3S06	GFCFG3S05	GFCFG3S04	GFCFG3S03	GFCFG3S02	GFCFG3S01	GFCFG3S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG3 S n	Writing 1 to GFCFG3S n will set glitch filter control signal GFCFG3 n to 0 in register PBGFCFG3. Writing 0 to GFCFG3S n will no use.	W

21.4.2.27 PORT GLITCH FILTER Configure Clear Register 3 (PxGFCFG3C,0x00A8)

PAGFCFG3C,PBGFCFG3C,PCGFCFG3C and PDGFCFG3C are four 32-bit PORT glitch filter control bit 3 clear registers.

	PxGFCFG3C																															**Base + 0x00A8**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFCFG3S31	GFCFG3S30	GFCFG3S29	GFCFG3S28	GFCFG3S27	GFCFG3S26	GFCFG3S25	GFCFG3S24	GFCFG3S23	GFCFG3S22	GFCFG3S21	GFCFG3S20	GFCFG3S19	GFCFG3S18	GFCFG3S17	GFCFG3S16	GFCFG3S15	GFCFG3S14	GFCFG3S13	GFCFG3S12	GFCFG3S11	GFCFG3S10	GFCFG3S09	GFCFG3S08	GFCFG3S07	GFCFG3S06	GFCFG3S05	GFCFG3S04	GFCFG3S03	GFCFG3S02	GFCFG3S01	GFCFG3S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	GFCFG3 C n	Writing 1 to GFCFG3C n will clear glitch filter control signal GFCFG3 n to 0 in register PBGFCFG3. Writing 0 to GFCFG3C n will no use.	W

These four registers used for suppress the glitch on port signal. The range of glitch width is:
1 x pclk ~ 15 x pclk

Bits	Name	Description	R/W
4	GFCFGn	Glitch Filter Configure Register for each PBD, digital filter which mask upto 15 pclk cycle's unstable input signal	RW

GFCFG3	GFCFG2	GFCFG1	GFCFG0	Drive Strength Level
0	0	0	0	(disable)
0	0	0	1	1 pclk
0	0	1	0	2 pclk
0	0	1	1	3

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..	..	..	..	..		
1	1	1	0	14		
1	1	1	1	15 pclk		

Note:

1. not each PBd supports Glitch Filter Function

Note:

1. pclk is the clock period configure to APB bus.
2. This function only used in interrupt input mode.
3. Not every bit for each port is implement this function. please refer *1.1*, only bits marked with "*13*" has this function.

21.4.2.28 PORTA VDDIO-SEL Register (PAVDDIO,0x0100)

PORTA generator pad vref/poc/hvps register.

	PAVDDIO																															0x0100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												Vddio_sel3	Vddio_sel2	Vddio_sel1	Vddio_sel0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
31:4	Reserved	Writing has no effect, Read as zero	R
3	vddio_sel[3]	control sel25 port of SPP_RE_SVR_182533V for generator I/O domain **voltage 1(PA23~PA31/PB/PC/PD)** VREFN/P ; 0: sel25 =0 ,I/O domain voltage 1 =1.8/2.8/3.0/3.3V; 1: sel25 =1 ,I/O domain voltage 1=2.5V;	RW
2	vddio_sel[2]	control sel25 port of SPP_RE_SVR_182533V for generator I/O domain **voltage 0(PA00~PA22)** VREFN/P ; 0: sel25 =0 ,I/O domain **voltage 0** =1.8/2.8/3.0/3.3V; 1: sel25 =1 ,I/O domain **voltage 0** =2.5V;	RW
1	vddio_sel[1]	control sel18 port of SPP_SP_POC_1833V for generator I/O domain **voltage 1(PA23~PA31/PB/PC/PD)** POC_N/P ,HVPS_N/P ; 0: sel18 =0 ,I/O domain voltage 1 >=2.5V; 1: sel18 =1 ,I/O domain voltage 1<=1.8V;	RW
0	vddio_sel[0]	control sel18 port of SPP_SP_POC_1833V for generator I/O domain **voltage 0(PA00~PA22)** POC_N/P ,HVPS_N/P ; 0: sel18 =0 ,I/O domain **voltage 0** >=2.5V; 1: sel18 =1 ,I/O domain **voltage 0**<=1.8V;	RW

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21.4.2.29 PORTA VDDIO-SEL Set Register (PAVDDIOS,0x0104)

PORTA GROUP generator pad vref/poc/hvps set register, WRITE-ONLY.

	PAVDDIOS																															0x0104
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												Vddio_sels3	Vddio_sels2	Vddio_sels1	Vddio_sels0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:4	Reserved	Writing has no effect, Read as zero	R
3:0	VDDIOS n	Writing 1 to VDDIOS n will set VDDIO n to 1 in register PAVDDIOn. Writing 0 to VDDIOS n will be ignored.	W

21.4.2.30 PORTA VDDIO-SEL Clear Register (PAVDDIOC,0x0108)

PORTA GROUP generator pad vref/poc/hvps clear register, WRITE-ONLY.

	PAVDDIOC																															0x0108
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												Vddio_selc3	Vddio_selc2	Vddio_selc1	Vddio_selc0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:4	Reserved	Writing has no effect, Read as zero	R
3:0	VDDIOC n	Writing 1 to VDDIOC n will set VDDIO n to 1 in register PAVDDIOn. Writing 0 to VDDIOC n will be ignored.	W

21.4.2.31 PORT Driver Disabled State Register0 (PxPEL,0x0110)

PORT x GROUP driver disabled state register0.

	PxPEL																															0x0110
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	PEL15		PEL14		PEL13		PEL12		PEL11		PEL10		PEL09		PEL08		PEL07		PEL06		PEL05		PEL04		PEL03		PEL02		PEL01		PEL00	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PELn	Where n = 0 ~ 15 and PEL n[1:0] = PEL[2n+1 : 2n]. PEL[2n+1: 2n] is used to control state of the corresponding PxPEL[2n+1 : 2n],which it's output has been disabled. 00: Hi-Z 01: Pull-up 10: Pull-down 11: Repeater	RW

21.4.2.32 PORT Driver Disabled State Set Register0 (PxPELS,0x0114)

PORT x GROUP driver disabled state set register0, WRITE-ONLY.

	PxPELS																															0x0114
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PELS15		PELS14		PELS13		PELS12		PELS11		PELS10		PELS09		PELS08		PELS07		PELS06		PELS05		PELS04		PELS03		PELS02		PELS01		PELS00	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PELS n	Writing 1 to PELSn[0] will set PELn[0] to 1 in register PxPELS. Writing 1 to PELSn[1] will set PELn[1] to 1 in register PxPELS. Writing 0 to PELS n will be ignored.	W

21.4.2.33 PORT Driver Disabled State Clear Register0 (PxPELC,0x0118)

PORT x GROUP driver disabled state clear register0, WRITE-ONLY.

	PxPELC																															0x0118
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	PELC15		PELC14		PELC13		PELC12		PELC11		PELC10		PELC09		PELC08		PELC07		PELC06		PELC05		PELC04		PELC03		PELC02		PELC01		PELC00	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PELC n	Writing 1 to PELCn[0] will set PELn[0] to 0 in register PxPELC. Writing 1 to PELCn[1] will set PELn[1] to 0 in register PxPELC. Writing 0 to PELC n will be ignored.	W

21.4.2.34 PORT Driver Disabled State Register1 (PxPEH,0x0120)

PORT x GROUP driver disabled state register1.

	PxPEH																															**0x0120**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PEH31		PEH30		PEH29		PEH28		PEH27		PEH26		PEH25		PEH24		PEH23		PEH22		PEH21		PEH20		PEH19		PEH18		PEH17		PEH16	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PEHn	Where n = 0 ~ 15 and PEH(n+16)[1:0] = PEH[2n+1 : 2n]. PEH[2n+1 : 2n] is used to control state of the corresponding PxPEH[2n+1 : 2n],which it's output has been disabled. 00: Hi-Z 01: Pull-up 10: Pull-down 11: Repeater	RW

21.4.2.35 PORT Driver Disabled State Set Register1 (PxPEHS,0x0124)

PORT x GROUP driver disabled state set register1, WRITE-ONLY.

	PxPEHS																															**0x0124**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	PEHS31		PEHS30		PEHS29		PEHS28		PEHS27		PEHS26		PEHS25		PEHS24		PEHS23		PEHS22		PEHS21		PEHS20		PEHS19		PEHS18		PEHS17		PEHS16	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PEHS n	Writing 1 to PEHSn[0] will set PEHn[0] to 1 in register PxPEHS. Writing 1 to PEHSn[1] will set PEHn[1] to 1 in register PxPEHS. Writing 0 to PEHS n will be ignored.	W

21.4.2.36 PORT Driver Disabled State Clear Register1 (PxPEHC,0x0128)

PORT x GROUP driver disabled state clear register1, WRITE-ONLY.

	PxPEHC																															**0x0128**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PEHC31		PEHC30		PEHC29		PEHC28		PEHC27		PEHC26		PEHC25		PEHC24		PEHC23		PEHC22		PEHC21		PEHC20		PEHC19		PEHC18		PEHC17		PELC16	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PEHC n	Writing 1 to PEHCn[0] will set PEHn[0] to 0 in register PxPEHC. Writing 1 to PEHCn[1] will set PEHn[1] to 0 in register PxPEHC. Writing 0 to PEHC n will be ignored.	W

21.4.2.37 PORT Drive Strength Register0 (PxDSL,0x0130)

PORT x GROUP Drive Strength register0.

	PxDSL																															**0x0130**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	DSL15		DSL14		DSL13		DSL12		DSL11		DSL10		DSL09		DSL08		DSL07		DSL06		DSL05		DSL04		DSL03		DSL02		DSL01		DSL00	
RST	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	DSLn	Where n = 0 ~ 15 and DSLn[1:0] = DSL[2n+1 : 2n]. DSL[2n+1 : 2n] is used to select drive strength of the corresponding PxDSL[2n+1 : 2n]. 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW

21.4.2.38 PORT Drive Strength Set Register0 (PxDSLS,0x0134)

PORT x GROUP Drive Strength set register0, WRITE-ONLY.

	PxDSLS																															**0x0134**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSLS15		DSLS14		DSLS13		DSLS12		DSLS11		DSLS10		DSLS09		DSLS08		DSLS07		DSLS06		DSLS05		DSLS04		DSLS03		DSLS02		DSLS01		DSLS00	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DSLS n	Writing 1 to DSLSn[0] will set DSLn[0] to 1 in register PxDSLS. Writing 1 to DSLSn[1] will set DSLn[1] to 1 in register PxDSLS. Writing 0 to DSLS n will be ignored.	W

21.4.2.39 PORT Drive Strength Clear Register0 (PxDSLC,0x0138)

PORT x GROUP Drive Strength clear register0, WRITE-ONLY.

	PxDSLC																															**0x0138**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	DSLC15		DSLC14		DSLC13		DSLC12		DSLC11		DSLC10		DSLC09		DSLC08		DSLC07		DSLC06		DSLC05		DSLC04		DSLC03		DSLC02		DSLC01		DSLC00	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DSLC n	Writing 1 to DSLCn[0] will set DSLn[0] to 0 in register PxDSLC. Writing 1 to DSLCn[1] will set DSLn[1] to 0 in register PxDSLC. Writing 0 to DSLC n will be ignored.	W

21.4.2.40 PORT Drive Strength Register1 (PxDSH,0x0140)

PORT x GROUP Drive Strength register1.

	PxDSH																															**0x0140**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSH31		DSH30		DSH29		DSH28		DSH27		DSH26		DSH25		DSH24		DSH23		DSH22		DSH21		DSH20		DSH19		DSH18		DSH17		DSH16	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	DSHn	Where n = 0 ~ 15 and DSH(n+16) = DSH[2n+1 : 2n]. DSH[2n+1 : 2n]is used to select drive strength of the corresponding PxDSH[2n+1 : 2n]. 00: 2mA 01: 4mA 10: 8mA 11: 12mA	RW

21.4.2.41 PORT Drive Strength Set Register1 (PxDSHS,0x0144)

PORT x GROUP Drive Strength set register1, WRITE-ONLY.

	PxDSHS																															**0x0144**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSHS31		DSHS30		DSHS29		DSHS28		DSHS27		DSHS26		DSHS25		DSHS24		DSHS23		DSHS22		DSHS21		DSHS20		DSHS19		DSHS18		DSHS17		DSHS16	

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RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DSHS n	Writing 1 to DSHSn[0] will set DSHn[0] to 1 in register PxDSHS. Writing 1 to DSHSn[1] will set DSHn[1] to 1 in register PxDSHS. Writing 0 to DSHS n will be ignored.	W

21.4.2.42 PORT Drive Strength Clear Register1 (PxDSHC,0x0148)

PORT x GROUP Drive Strength clear register1, WRITE-ONLY.

	PxDSHC																															**0x0148**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSHC31		DSHC30		DSHC29		DSHC28		DSHC27		DSHC26		DSHC25		DSHC24		DSHC23		DSHC22		DSHC21		DSHC20		DSHC19		DSHC18		DSHC17		DSHC16	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DSHC n	Writing 1 to DSHCn[0] will set DSHn[0] to 0 in register PxDSHC. Writing 1 to DSHSn[1] will set DSHn[1] to 1 in register PxDSHS. Writing 0 to DSHCn will be ignored.	W

21.4.2.43 PORT Slew Rate Register (PxSR,0x0150)

PORT x GROUP slew rate register.

	PxSR																															**0x0150**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SR31	SR30	SR29	SR28	SR27	SR26	SR25	SR24	SR23	SR22	SR21	SR20	SR19	SR18	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10	SR09	SR08	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	SR n	Where n = 0 ~ 31 and SR n = SR0 ~ SR31.	RW

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		SR n is used to switch slew rate of the corresponding PxSRn. 0: slow(half frequency) 1: fast	

21.4.2.44 PORT Slew Rate Set Register (PxSRS,0x0154)

PORT x GROUP slew rate set register, WRITE-ONLY.

	PxSRS																															0x0154
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRS31	SRS30	SRS29	SRS28	SRS27	SRS26	SRS25	SRS24	SRS23	SRS22	SRS21	SRS20	SRS19	SRS18	SRS17	SRS16	SRS15	SRS14	SRS13	SRS12	SRS11	SRS10	SRS09	SRS08	SRS07	SRS06	SRS05	SRS04	SRS03	SRS02	SRS01	SRS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SRS n	Writing 1 to SRS n will set SR n to 1 in register PxSRS. Writing 0 to SRS n will be ignored.	W

21.4.2.45 PORT Slew Rate Clear Register (PxSRC,0x0158)

PORT x GROUP slew rate clear register, WRITE-ONLY.

	PxSRC																															0x0158
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRC31	SRC30	SRC29	SRC28	SRC27	SRC26	SRC25	SRC24	SRC23	SRC22	SRC21	SRC20	SRC19	SRC18	SRC17	SRC16	SRC15	SRC14	SRC13	SRC12	SRC11	SRC10	SRC09	SRC08	SRC07	SRC06	SRC05	SRC04	SRC03	SRC02	SRC01	SRC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SRC n	Writing 1 to SRC n will set SR n to 0 in register PxSRC. Writing 0 to SRC n will be ignored.	W

21.4.2.46 PORT Schmitt Trigger Register (PxSMT,0x0160)

PORT x GROUP schmitt trigger register.

	PxSMT																															0x0160
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	SMT31	SMT30	SMT29	SMT28	SMT27	SMT26	SMT25	SMT24	SMT23	SMT22	SMT21	SMT30	SMT19	SMT18	SMT17	SMT16	SMT15	SMT14	SMT13	SMT12	SMT11	SMT10	SMT09	SMT08	SMT07	SMT06	SMT05	SMT04	SMT03	SMT02	SMT01	SMT00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	SMT n	Where n = 0 ~ 31 and SMT n = SMT0 ~ SMT31. SMT n is used to enable schmitt trigger of the corresponding PxSMTn. 0: schmitt trigger disabled 1: schmitt trigger enabled	RW

21.4.2.47 PORT Schmitt Trigger Set Register (PxSMTS,0x0164)

PORT x GROUP schmitt trigger set register, WRITE-ONLY.

	PxSMTS																															**0x0164**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SMTS31	SMTS30	SMTS29	SMTS28	SMTS27	SMTS26	SMTS25	SMTS24	SMTS23	SMTS22	SMTS21	SMTS20	SMTS19	SMTS18	SMTS17	SMTS16	SMTS15	SMTS14	SMTS13	SMTS12	SMTS11	SMTS10	SMTS09	SMTS08	SMTS07	SMTS06	SMTS05	SMTS04	SMTS03	SMTS02	SMTS01	SMTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SMTS n	Writing 1 to SMTS n will set SMT n to 1 in register PxSMTS. Writing 0 to SMTS n will be ignored.	W

21.4.2.48 PORT Schmitt Trigger Clear Register (PxSMTC,0x0168)

PORT x GROUP schmitt trigger clear register, WRITE-ONLY.

	PxSMTC																															**0x0168**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SMTC31	SMTC30	SMTC29	SMTC28	SMTC27	SMTC26	SMTC25	SMTC24	SMTC23	SMTC22	SMTC21	SMTC20	SMTC19	SMTC18	SMTC17	SMTC16	SMTC15	SMTC14	SMTC13	SMTC12	SMTC11	SMTC10	SMTC09	SMTC08	SMTC07	SMTC06	SMTC05	SMTC04	SMTC03	SMTC02	SMTC01	SMTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W

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31:0	SMTC n	Writing 1 to SMTC n will set SMT n to 0 in register PxSMTC. Writing 0 to SMTC n will be ignored.	W

21.4.2.49 PORT Receiver Enable State Register (PxIE,0x0180)

PORT x GROUP receiver enable register.

	PxIE																															0x0180
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IE31	IE30	IE29	IE28	IE27	IE26	IE25	IE24	IE23	IE22	IE21	IE30	IE19	IE18	IE17	IE16	IE15	IE14	IE13	IE12	IE11	IE10	IE09	IE08	IE07	IE06	IE05	IE04	IE03	IE02	IE01	IE00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	IE n	Where n = 0 ~ 31 and IE n = IE0 ~ IE31. IE n is used to enable receiver enable of the corresponding PxIEn. 0: receiver enable disabled 1: receiver enable enabled	RW

21.4.2.50 PORT Receiver Enable State Set Register (PxIES,0x0184)

PORT x GROUP receiver enable set register, WRITE-ONLY.

	PxIES																															0x0184
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IES31	IES30	IES29	IES28	IES27	IES26	IES25	IES24	IES23	IES22	IES21	IES20	IES19	IES18	IES17	IES16	IES15	IES14	IES13	IES12	IES11	IES10	IES09	IES08	IES07	IES06	IES05	IES04	IES03	IES02	IES01	IES00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	IES n	Writing 1 to IES n will set IE n to 1 in register PxIES. Writing 0 to IES n will be ignored.	W

21.4.2.51 PORT Receiver Enable State Clear Register (PxIEC,0x0188)

PORT x GROUP receiver enable clear register, WRITE-ONLY.

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	PxIEC																															0x0188
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC09	IEC08	IEC07	IEC06	IEC05	IEC04	IEC03	IEC02	IEC01	IEC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	IEC n	Writing 1 to IEC n will set IE n to 0 in register PxIEC. Writing 0 to IEC n will be ignored.	W

21.4.2.52 PORT Z Shadow Register Group

PORT Z group only have eight registers, PZINTS,PZINTC,PZMSKS,PZMSKC,PZPAT1S,PZPAT1C, PZPAT0S,PZPAT0C. those registers shadow as same as other group registers function which the offset address equal.

	PZINTS																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTS31	INTS30	INTS29	INTS28	INTS27	INTS26	INTS25	INTS24	INTS23	INTS22	INTS21	INTS20	INTS19	INTS18	INTS17	INTS16	INTS15	INTS14	INTS13	INTS12	INTS11	INTS10	INTS09	INTS08	INTS07	INTS06	INTS05	INTS04	INTS03	INTS02	INTS01	INTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZINTC																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC31	INTC30	INTC29	INTC28	INTC27	INTC26	INTC25	INTC24	INTC23	INTC22	INTC21	INTC20	INTC19	INTC18	INTC17	INTC16	INTC15	INTC14	INTC13	INTC12	INTC11	INTC10	INTC09	INTC08	INTC07	INTC06	INTC05	INTC04	INTC03	INTC02	INTC01	INTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZMSKS																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKS31	MSKS30	MSKS29	MSKS28	MSKS27	MSKS26	MSKS25	MSKS24	MSKS23	MSKS22	MSKS21	MSKS20	MSKS19	MSKS18	MSKS17	MSKS16	MSKS15	MSKS14	MSKS13	MSKS12	MSKS11	MSKS10	MSKS09	MSKS08	MSKS07	MSKS06	MSKS05	MSKS04	MSKS03	MSKS02	MSKS01	MSKS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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	PZMSKC																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKC31	MSKC30	MSKC29	MSKC28	MSKC27	MSKC26	MSKC25	MSKC24	MSKC23	MSKC22	MSKC21	MSKC20	MSKC19	MSKC18	MSKC17	MSKC16	MSKC15	MSKC14	MSKC13	MSKC12	MSKC11	MSKC10	MSKC09	MSKC08	MSKC07	MSKC06	MSKC05	MSKC04	MSKC03	MSKC02	MSKC01	MSKC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT1S																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1S31	PAT1S30	PAT1S29	PAT1S28	PAT1S27	PAT1S26	PAT1S25	PAT1S24	PAT1S23	PAT1S22	PAT1S21	PAT1S20	PAT1S19	PAT1S18	PAT1S17	PAT1S16	PAT1S15	PAT1S14	PAT1S13	PAT1S12	PAT1S11	PAT1S10	PAT1S09	PAT1S08	PAT1S07	PAT1S06	PAT1S05	PAT1S04	PAT1S03	PAT1S02	PAT1S01	PAT1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT1S																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1C31	PAT1C30	PAT1C29	PAT1C28	PAT1C27	PAT1C26	PAT1C25	PAT1C24	PAT1C23	PAT1C22	PAT1C21	PAT1C20	PAT1C19	PAT1C18	PAT1C17	PAT1C16	PAT1C15	PAT1C14	PAT1C13	PAT1C12	PAT1C11	PAT1C10	PAT1C09	PAT1C08	PAT1C07	PAT1C06	PAT1C05	PAT1C04	PAT1C03	PAT1C02	PAT1C01	PAT1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT0S																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0S31	PAT0S30	PAT0S29	PAT0S28	PAT0S27	PAT0S26	PAT0S25	PAT0S24	PAT0S23	PAT0S22	PAT0S21	PAT0S20	PAT0S19	PAT0S18	PAT0S17	PAT0S16	PAT0S15	PAT0S14	PAT0S13	PAT0S12	PAT0S11	PAT0S10	PAT0S09	PAT0S08	PAT0S07	PAT0S06	PAT0S05	PAT0S04	PAT0S03	PAT0S02	PAT0S01	PAT0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT0C																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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	PAT0C31	PAT0C30	PAT0C29	PAT0C28	PAT0C27	PAT0C26	PAT0C25	PAT0C24	PAT0C23	PAT0C22	PAT0C21	PAT0C20	PAT0C19	PAT0C18	PAT0C17	PAT0C16	PAT0C15	PAT0C14	PAT0C13	PAT0C12	PAT0C11	PAT0C10	PAT0C09	PAT0C08	PAT0C07	PAT0C06	PAT0C05	PAT0C04	PAT0C03	PAT0C02	PAT0C01	PAT0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

21.4.2.53 GPIOZ Group ID to Load Register (PzGID2LD,0x00F0)

This register controls which Port Group to be load from GPIOZ.

	PzGID2LD																															**Base + 0x00F0**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													GPID		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOZ Group can shadow four register groups for GPIO Group A to D, when set or clear A to D register groups below four types, it will through shadow register to implement. the GPIOZ ID used for controls which Group to be manipulate.

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, Read as zero	R
2:0	GPID	GPIO Port ID load control register, according the values of GPID to load Shadow register group to the same offset address of group ID meet the GPID. GPID: Shadow register load to work groups 0: Load to GPIO Port A 1: Load to GPIO Port B 2: Load to GPIO Port C 3: Load to GPIO Port D 4: Undefine 5: Undefine	W

21.5 Program Guide

21.5.1 Port Function Guide

INT	MASK	PAT1	PAT0	Port Description

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1	0	0	0	Port is low level triggered interrupt input.
1	0	0	1	Port is high level triggered interrupt input.
1	0	1	0	Port is fall edge triggered interrupt input.
1	0	1	1	Port is rise edge triggered interrupt input.
1	1	0	0	Port is low level triggered interrupt input. Interrupt is masked. Flag is recorded.
1	1	0	1	Port is high level triggered interrupt input. Interrupt is masked. Flag is recorded.
1	1	1	0	Port is fall edge triggered interrupt input. Interrupt is masked. Flag is recorded.
1	1	1	1	Port is rise edge triggered interrupt input. Interrupt is masked. Flag is recorded.
0	0	0	0	Port is pin of device 0.
0	0	0	1	Port is pin of device 1.
0	0	1	0	Port is pin of device 2.
0	0	1	1	Port is pin of device 3.
0	1	0	0	Port is GPIO output 0.
0	1	0	1	Port is GPIO output 1.
0	1	1	?	Port is GPIO input.

21.5.2 Configure without 3rd-unexpected state

Function switching between devices and gpio is controlled by combination of 4 registers: INT/MASK/PAT1/PAT0. As the four register is accessed by soft ware in serial sequence, which posing a risk that third states occur during configuration.

For example:

current state is:

INT = 0x0, MASK = 0x0, PAT0 = 0x0, PAT1 = 0x0;

target state is:

INT = 0x1, MASK = 0x1, PAT0 = 0x1, PAT1 = 0x1;

If the first step is to configure INT to 0x1, the 3rd state is:

INT = 0x1, MASK = 0x0, PAT0 = 0x0, PAT1 = 0x0;

This might triggers interrupt if port is low level.

To avoid the unexpected 3-state, the four registers must be updated in the same time.

There is an dummy group GPIOZ, which only used in this purpose. The working mechanism is the information of configure can be temporarily stored in the GPIOZ. When assert GPIOZ.LD, all the four registers will load their content into target group at the same time.

Example:

If the Port B current state is:

INT = 0x0, MASK = 0x0, PAT0 = 0x0, PAT1 = 0x0;

It needs to be configured to state:

INT = 0x1, MASK = 0x1, PAT0 = 0x1, PAT1 = 0x1;

There are two steps to finish:

Step1: put the configuration to temporary buffer: GPIOZ

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```
PzINTS = 0x1;
PzMSKS = 0x1;
PzPAT0S = 0x1;
PzPAT1S = 0x1;
```

alternatively, PzINT, PzMSK, PzPAT0, PzPAT1 are also can be configured straightly.

Step2: configure PzGID2LD to specify which port group to load

PzGID2LD = 0x1; (0x1 stands for GPIO Port B)

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22 SMB Controller

22.1 Overview

The SMB bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock (SCL). These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a “transmitter” or “receiver,” depending on the function of the device. Devices can also be considered as masters or slaves when performing data transfers. A master is the device that initializes/terminates a data transfer on the bus and generates clock signals to permit that transfer. During that time, any addressed device is considered as a slave. The SMB controller is software controlled. It behaves as a master or a slave. However, operating as a master and slave simultaneously is not supported.

22.2 Features

- Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
- Two speeds
  - Standard mode (100 Kb/s)
  - Fast mode (400 Kb/s)
- Device clock is identical with pclk(APB clock)
- Programmable SCL generator
- Master or slave SMB operation
- 7-bit addressing/10-bit addressing whether configure as Master or Slave
- Transmit General Call or START byte
- level transmit and receive 64 depth FIFOs
- Interrupt operation
- The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
- APB interface
- 3 independent SMB channels (SMB0, SMB1, SMB2)

22.3 Pin Description

Table 22-1 SMB Pin Description

Name	Width	GPIO	Description
SDA0	1-bit	PA12	SMB serial data
SCL0	1-bit	PA13	SMB serial clock
SDA1	1-bit	PB25	SMB serial data
SCL1	1-bit	PB26	SMB serial clock
SDA2	1-bit	PC27	SMB serial data
SCL2	1-bit	PC28	SMB serial clock

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Note:

1.Dedicate pull-up resistors must be introduced on board-level. The low-to-high (rise time) transition is highly dependent on RC time constant of the bus.

2.The two GPIOs refer to SMB must belong to the same GPIO group.

Totally speaking, for standard-mode SMB-bus system, the pull up resistor depends on following parameters:

- Supply voltage
- Bus capacitance
- Number of connected devices

For fast-mode SMB-bus system, switched pull-up circuit may be essential for strict speed and load requirement. (Please refer NXP Semiconductors, *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014)*')

22.4 Registers Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. The registers can be read and written by APB bus
3. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by write 1, write 0 has no effect

   RWS - read and write, set to 1 by write 1, write 0 has no effect

   RC - read only, and clear to 0 by read

   RS - read only, and set to 1 by read

   SPEC - special access method, relate to its description
4. Reset Value

   1 - reset to 1

   0 - reset to 0

   ? - value unknown after reset

22.4.1 Registers Memory Map

A read operation to an address location that contains unused bits results in a 0 value being returned on each of the unused bits.

Registers in SMB controller can be accessed by indicating 24-bit Address Base combined with 8-bit Address Offset.

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Table 22-2 Registers Memory Map Base Address

Name	Addr Base	Description
SMB0	0x10050000	Address base of SMB0
SMB1	0x10051000	Address base of SMB1
SMB2	0x10052000	Address base of SMB2

The SMB Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 22-3 SMB Registers Map

Name	RW	Reset Value	Address Offset	Access Size
SMB_CON	RW	0x007D	0x0000	16
SMB_TAR	RW	0x1055	0x0004	16
SMB_SAR	RW	0x0055	0x0008	16
SMB_DC	RW	0x0000	0x0010	16
SMB_SHCNT	RW	0x0190	0x0014	16
SMB_SLCNT	RW	0x01D6	0x0018	16
SMB_FHCNT	RW	0x003C	0x001C	16
SMB_FLCNT	RW	0x0082	0x0020	16
SMB_INTST	R	0x0000	0x002C	16
SMB_INTM	RW	0x08FF	0x0030	16
SMB_RAW_INTR_STAT	R	0x0000	0x0034	16
SMB_RXTL	RW	0x001F	0x0038	16
SMB_TXTL	RW	0x0020	0x003C	16
SMB_CINT	R	0x0000	0x0040	16
SMB_CRXUF	R	0x0000	0x0044	16
SMB_CRXOF	R	0x0000	0x0048	16
SMB_CTXOF	R	0x0000	0x004C	16
SMB_CRXREQ	R	0x0000	0x0050	16
SMB_CTXABT	R	0x0000	0x0054	16
SMB_CRXDN	R	0x0000	0x0058	16
SMB_CACT	R	0x0000	0x005C	16
SMB_CSTP	R	0x0000	0x0060	16
SMB_CSTT	R	0x0000	0x0064	16
SMB_CGC	R	0x0000	0x0068	16
SMB_ENABLE	RW	0x0000	0x006C	16
SMB_ST	R	0x0006	0x0070	16
SMB_TXFLR	R	0x0000	0x0074	16
SMB_RXFLR	R	0x0000	0X0078	16
SMB_SDAHD	RW	0x0055	0x007C	16
SMB_ABTSRC	R	0x0000	0x0080	16
SMB_DMACR	RW	0x0000	0x0088	16

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SMB_DMATDLR	RW	0x0000	0x008C	16
SMB_DMARDLR	RW	0x0000	0x0090	16
SMB_SDASU	RW	0x0064	0x0094	16
SMB_ACKGC	RW	0x0001	0x0098	16
SMB_ENBST	R	0x0000	0x009C	16
SMB_FLT	RW	0x0001	0x00A0	16

22.4.2 Registers and Fields Description

22.4.2.1 SMB Control Register(SMB_CON,0x0000)

This register can be written only when SMB is disabled, which corresponds to SMB_ENABLE[0] being set to 0. Writes at other time have on effect.

	SMB_CON																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									SLVDIS	RESTART	MATP	SATP	SPEED		MD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6	SLVDIS	This bit controls whether SMB has its slave disabled. 0: slave is enabled 1: slave is disabled **Note:** Software should ensure that if this bit is written with'0', then bit 0 should also be written with '0'.	RW
5	RESTART	Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions. 0: disable 1: enable	RW
4	MATP	This bit is a read-only copy of SMB_TAR.MATP. 0: 7-bit addressing 1: 10-bit addressing	R
3	SATP	When acting as a slave, this bit controls whether the SMB responds to 7-bit or 10-bit addresses. 0: 7-bit addressing 1: 10-bit addressing	RW

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2:1	SPEED	These bits control at which speed the SMB operates. 1: standard mode (100 kbps) 2: fast mode (400 kbps) **NOTE:** *when these two bits are set to 2'b00 or 2'b11, the speed mode will be automatically set to 2'b10 i.e. fast mode.*	RW
0	MD	This bit controls whether the SMB master is enabled. 0: master disabled 1: master enabled **Note:** Software should ensure that if this bit is written with'1', then bit 6 should also be written with '1'.	RW

22.4.2.2 SMB Target Address Register(SMB_TAR,0x0004)

	SMB_TAR																															
																																Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			MATP	SPECIAL	GC_OR_START	SMBTAR									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Name	Description	R/W
31:13	Reserved	Writing has no effect, read as zero.	R
12	MATP	This bit controls whether the SMB starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0: 7-bit addressing 1: 10-bit addressing **NOTE:** this bit is initially set to 0.	RW
11	SPECIAL	This bit indicates whether software performs a General Call or START BYTE command. 0: ignore the bit of GC_OR_START and use SMBTAR normally 1: perform special SMB command as specified in GC_OR_START bit **NOTE:** this bit is initially set to 0	RW
10	GC_OR_START	If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the SMB. 0: General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the SMB_INTST register. The SMB remains in General Call mode	RW

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		until the SPECIAL bit value (bit 11) is cleared 1: START BYTE	
9:0	SMBTAR	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the SMB_TAR and SMB_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself, but only to a slave.	RW

Note:

(1).It is not necessary to perform any write to this register if SMB is enabled as an SMB slave only.

(2).The meaning of "START byte" in bit 10 is different with the SMB "start condition".

"START byte" can only be applied when a device does not have such an interface, it must constantly monitor the bus via software. For more detail information, please refer *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014),* '3.1.15 START byte' section.

"start condition" means A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. please refer *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014),* '3.1.4 START and STOP' section for more information.

22.4.2.3 SMB Slave Address Register(SMB_SAR,0x08)

	SMB_SAR																															
																																Base + 0x08
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						SMBSAR									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Name	Description	R/W
31:10	Reserved	Writing has no effect. Read as zero.	R
9:0	SMBSAR	The SMBSAR holds the slave address when the SMB is operating as a slave. For 7-bit addressing, only SMBSAR[6:0] is used. This register can be written only when the SMB interface is disabled. Writes at other times have no effect.	RW

Note: It is not necessary to perform any write to this register if SMB is enabled as an SMB master only.

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22.4.2.4 SMB Rx/Tx Data Buffer and Command Register(SMB_DC,0x0010)

This is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO.

	SMB_DC																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					RESTART	STOP	CMD	DAT							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:11	Reserved	Writing has no effect. Read as zero.	R
10	RESTART	This bit controls whether a RESTART is issued before the byte is sent or received. 1: If SMB_CON.RESTART is 1, a RESTART is issued before the byte is sent or received, regardless of whether or not the transfer direction is changing from the previous command; if SMB_CON.RESTART is 0, a STOP followed by a START is issued instead. 0: If SMB_CON.RESTART is 1, a RESTERT is issued if the transfer direction is changing from the previous command, if SMB_CON.RESTART is 0, a STOP followed by a START is issued instead.	W
9	STOP	This bit controls whether a STOP is issued after the byte is sent or received. 1: STOP is issued after the byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0: STOP is not issued after the byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.	W
8	CMD	This bit controls whether a read or a write is performed. This bit does not control the direction when the SMB acts as a slave. It controls only the direction when it acts as a master. 1: Read 0: Write When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command	W

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		has been sent results in a *TX_ABRT* interrupt (bit 6 of the *SMB_RAW_INTR_STAT* register), unless bit 11 (*SPECIAL*) in the *SMB_TAR* register has been cleared. If a “1” is written to this bit after receiving a *RD_REQ* interrupt, then a *TX_ABRT* interrupt occurs.	
7:0	DAT	This register contains the data to be transmitted or received on the SMB bus. If you are writing to this register and want to perform a read, bits 7:0 (*DAT*) are ignored by the SMB module. However, when you read this register, these bits return the value of data received on the SMB interface.	RW

Note:

[1].this command only transfer 8-bit data combined with 1-bit CMD, extra bits on the bus will be eliminated. i.e. only 8-0 bits on the bus are accepted by SMB controller.

[2].For the detail information about what condition could generate START, STOP and RESTART, please refer "1.3.6 The condition could generate START, STOP and RESTART".

[3].The differences between SMB_ENABLE[5](RESTART) and SMB_DC[10](RESTART) is that SMB_ENABLE[5] determine whether or not SMB the capability of generating repeat start, but not transmit RESTART when this bit be setted. If this bit set "1", SMB_DC[10] controls whether a RESTART is issued, if set "0", SMB_DC[10] have no meaning.

22.4.2.5 SMB Standard Speed SCL High Count Register(SMB_SHCNT,0x0014)

	SMB_SHCNT																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SMBSHCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	SMBSHCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. The register sets the SCL clock high-period count for standard speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set.	RW

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22.4.2.6 SMB Standard Speed SCL Low Count Register(SMB_SLCNT,0x0018)

	SMB_SLCNT																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SMBSLCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	SMBSLCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set.	RW

22.4.2.7 SMB Fast Speed SCL High Count Register (SMB_FHCNT,0x001C)

	SMB_FHCNT																															Base + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SMBFHCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	SMBFHCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect.	RW

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		Minimum value allowed for the SMBSHCNT registers is 6. If the set value was less than 6, it will be automatically set to 6.	

22.4.2.8 SMB Fast Speed SCL Low Count Register (SMB_FLCNT,0x0020)

	SMB_FLCNT																															Base + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SMBFLCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	SMBFLCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect. Minimum value that can be programmed in the SMBSLCNT registers is 8. If the set value was less than 8, it will be automatically set to 8	RW

22.4.2.9 SMB Interrupt Status Register(SMB_INTST,0x002C)

Each bit in this register has a corresponding mask bit in the SMBINTM register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the *SMB_RAW_INTR_STAT* register

	SMB_INTST																															Base + 0x002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				IGC	ISTT	ISTP	IACT	RXDN	TXABT	RDREQ	TXEMP	TXOF	RXFL	RXOF	RXUF
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect,read as zero.	R

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11	IGC	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling SMB or when the CPU reads bit 0 of the *SMB_CGC* register. SMB stores the received data in the Rx buffer.	R
10	ISTT	Indicates whether a START or RESTART condition has occurred on the SMB interface regardless of whether SMB is operating in slave or master mode.	R
9	ISTP	Indicates whether a STOP condition has occurred on the SMB interface regardless of whether SMB is operating in slave or master mode.	R
8	IACT	This bit captures SMB activity and stays set until it is cleared. There are four ways to clear it: 1 Disabling the SMB 2 Reading the SMB_CACT register 3 Reading the SMB_CINT register 4 System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the SMB module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	R
7	RXDN	When the SMB is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	R
6	TXABT	This bit indicates if SMB, as an SMB transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an SMB master or an SMB slave, and is referred to as a “transmit abort”. When this bit is set to 1, the SMB_ABTSRC register indicates the reason why the transmit abort takes places. **Note:** *The SMB flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register SMB_CTXABT is read. Once this read is performed, the TX FIFO is then* *ready to accept more data bytes from the APB interface.*	R
5	RDREQ	This bit is set to 1 when SMB is acting as a slave and another SMB master is attempting to read data from SMB. The SMB holds the SMB bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the SMB_DC register. This bit is set to 0 just after the processor reads the SMB_CRREQ register.	R
4	TXEMP	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the SMB_TXTL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the SMB_ENB bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to	R

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		1, provided there is activity in the master or slave state machines. When there is no longer activity, then with SMB_ENB[0]=0.	
3	TXOF	Set during transmit if the transmit buffer is filled to SMB_TX_BUFFER_DEPTH and the processor attempts to issue another SMB command by writing to the SMB_DC register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when SMB_ENB[0]=0, this interrupt is cleared.	R
2	RXFL	Set when the receive buffer reaches or goes above the SMB_RXTL threshold in the SMB_RXTL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (SMB_ENB[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the SMB_ENB bit 0 is set to 0, regardless of the activity that continues.	R
1	RXOF	Set if the receive buffer is completely filled to 64 and an additional byte is received from an external SMB device. The SMB acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (SMB_ENB[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when SMB_ENB[0]=0, this interrupt is cleared.	R
0	RXUF	Set if the processor attempts to read the receive buffer when it is empty by reading from the SMB_DC register. If the module is disabled (SMB_ENB[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when SMB_ENB[0]=0, this interrupt is cleared.	R

Note: *22.5.5* summary all the condition could flush TX FIFO.

22.4.2.10 SMB Interrupt Mask Register(SMB_INTM,0x0030)

These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

	SMB_INTM																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				MIGC	MISTT	MISTP	MIACT	MRXDN	MTXABT	MRDREQ	MTXEMP	MTXOF	MRXFL	MRXOF	MRXUF
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R

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11	MIGC	These bits mask their corresponding interrupt status bits in the SMBINTST register.	RW
10	MISTT		RW
9	MISTP		RW
8	MIACT		RW
7	MRXDN		RW
6	MTXABT		RW
5	MRDREQ		RW
4	MTXEMP		RW
3	MTXOF		RW
2	MRXFL		RW
1	MRXOF		RW
0	MRXUF		RW

22.4.2.11 SMB Raw Interrupt Status Register(SMB_RAW_INTR_STAT,0x0034)

Address: **BASE + 0x0034**

Unlike the *SMB_INTST* register, these bits are not masked so they always show the true status of the SMB. See *SMB_INTST* for a detailed description of these bits. All bits are only read.

22.4.2.12 SMB Receive FIFO Threshold Register(SMB_RXTL,0x0038)

	SMB_RXTL																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RXTL					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect. Read as zero.	R
5:0	RXTL	Receive FIFO Threshold Level. Controls the level of entries that triggers the RxFIFO full interrupt. A value of n sets the threshold for (n+1) entries. For example, a value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.	RW

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22.4.2.13 SMB Transmit FIFO Threshold Register(SMB_TXTL,0x003C)

	SMB_TXTL																															Base + 0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										TXTL					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect. Read as zero.	R
5:0	TXTL	Transmit FIFO Threshold Level. Controls the level of entries that trigger the TxFIFO empty interrupt. A value of n sets the threshold for n entries. For example, A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.	RW

22.4.2.14 SMB Clear Combined and Individual Interrupt Register(SMB_CINT,0x0040)

	SMB_CINT																															Base + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CINT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CINT	Read this register to clear the combined interrupt, all individual interrupts, and the SMB_ABTSRC register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the SMB_ABTSRC register for an exception to clearing SMB_ABTSRC.	R

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22.4.2.15 SMB Clear RXUF Interrupt Register(SMB_CRXUF,0x0044)

	SMB_CRXUF																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CRXUF
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	CRXUF	Read this register to clear the RXUF interrupt (bit 0) of the SMB_INTST register.	R

22.4.2.16 SMB Clear RXOF Interrupt Register(SMB_CRXOF,0x0048)

	SMB_CRXOF																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CRXOF
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	CRXOF	Read this register to clear the RXOF interrupt (bit 1) of the SMBINTST register.	R

22.4.2.17 SMB Clear TX_OVER Interrupt Register(SMB_CTXOF,0x004C)

	SMB_CTXOF																															Base + 0x004C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CTXOF
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	CTXOF	Read this register to clear the TX_OVER interrupt (bit 3) of the SMBINTST register.	R

22.4.2.18 SMB Clear RDREQ Interrupt Register(SMB_CRXREQ,0x0050)

	SMB_CRXREQ																															Base + 0x0050
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CLRDREQ
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CLRDREQ	Read this register to clear the RDREQ interrupt (bit 5) of the SMBINTST register.	R

22.4.2.19 SMB Clear TX_ABRT Interrupt Register(SMB_CTXABT,0x0054)

	SMB_CTXABT																															Base + 0x0054
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CTXABT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	CTXABT	Read this register to clear the TX_ABRT interrupt (bit 6) of the SMB_INTST register, and the SMB_ABTSRC register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the SMB_ABTSRC register for an exception to clearing SMB_ABTSRC.	R

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22.4.2.20 SMB Clear RX_DONE Interrupt Register(SMB_CRXDN,0x0058)

	SMB_CRXDN																															Base + 0x0058
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CRXDN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CRXDN	Read this register to clear the RX_DONE interrupt (bit 7) of the SMB_INTST register.	R

22.4.2.21 SMB Clear ACTIVITY Interrupt Register(SMB_CACT,0x005C)

	SMB_CACT																															Base + 0x005C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CACT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CACT	Reading this register clears the ACTIVITY interrupt if the SMB is not active anymore. If the SMB module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the SMBINTST register.	R

22.4.2.22 SMB Clear STOP Interrupt Register(SMB_CSTP,0x0060)

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	SMB_CSTP																																Base + 0x0060
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CSTP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CSTP	Read this register to clear the STOP interrupt (bit 9) of the SMBINTST register.	R

22.4.2.23 SMB Clear START Interrupt Register(SMB_CSTT,0x0064)

	SMB_CSTT																																Base + 0x0064
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CSTT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	CSTT	Read this register to clear the START interrupt (bit 10) of the SMBINTST register.	R

22.4.2.24 SMB Clear GEN_CALL Interrupt Register(SMB_CGC,0x0068)

	SMB_CGC																																Base + 0x0068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CGC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	CGC	Read this register to clear the GEN_CALL interrupt (bit 11) of SMBINTST register.	R

22.4.2.25 SMB Enable Register(SMB_ENABLE,0x006C)

	SMBE_NABLE																															Base + 0x006C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														ABORT	SMBENB
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect Read as zero.	R
1	ABORT	When set, the controller initiates the transfer abort. 0: ABORT not initiated or ABORT done 1: ABORT operation in progress The software can abort the SMB transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.	RW
0	SMBENB	Controls whether the SMB is enabled. 0: Disables SMB (TX and RX FIFOs are held in an erased state) 1: Enables SMB Software can disable SMB while it is active. However, it is important that care be taken to ensure that SMB is disabled properly. When SMB is disabled, the following occurs: – The TX FIFO and RX FIFO get flushed. – Status bits in the SMB_INTST register are still active until SMB goes into IDLE state. If the module is transmitting, it stops as well as deletes the	RW

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		contents of the transmit buffer after the current transfer is complete. If the module is receiving, the SMB stops the current transfer at the end of the current byte and does not acknowledge the transfer.	

22.4.2.26 SMB Status Register(SMB_ST,0x0070)

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

When the SMB is disabled by writing 0 in bit 0 of the SMB_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machine goes to idle and SMB_ENABLE[0]=0:

- Bits 5 and 6 are set to 0

	SMB_ST																															Base + 0x0070
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									SLVACT	MSTACT	RFF	RFNE	TFE	TFNF	ACT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Name	Description	R/W
31:7	Reserved	Writing has no effect. Read as zero.	R
6	SLVACT	Slave FSM Activity Status. 0: Slave FSM is in IDLE state so the Slave part of SMB is not Active 1: Slave FSM is not in IDLE state so the Slave part of SMB is Active	R
5	MSTACT	Master FSM Activity Status. 0: Master FSM is in IDLE state so the Master part of SMB is not Active 1: Master FSM is not in IDLE state so the Master part of SMB is Active	R
4	RFF	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full	R
3	RFNE	Receive FIFO Not Empty.	R

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		This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty	
2	TFE	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty	R
1	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full	R
0	ACT	SMB Activity Status. The OR of SLVACT and MSTACT bits.	R

22.4.2.27 SMB Transmit FIFO Level Register(SMB_TXFLR,0x0074)

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The SMB is disabled
- There is a transmit abort—that is, TX_ABRT bit is set in the SMB_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

																																Base + 0x0074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										TXFLR					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect, read as zero.	R
5:0	TXFLR	Contains the number of valid data entries in the transmit FIFO	R

22.4.2.28 SMB Receive FIFO Level Register(SMB_RXFLR,0x0078)

This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever:

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– The SMB is disabled

– Whenever there is a transmit abort caused by any of the events tracked in SMB_ABTSRC

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

																																Base + 0x0078
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RXFLR					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect, read as zero.	R
5:0	RXFLR	Contains the number of valid data entries in the receive FIFO	R

22.4.2.29 SMB SDA Hold Time Register(SMB_SDAHD,0x007C)

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of APB clock period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented—one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when SMB_ENABLE[0]=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in APB clock cycles.

	SMB_SDAHD																															Base + 0x007C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SDAHD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	SDAHD	SMB Hold Time. Sets the required SDA hold time in units of APB clock period.	RW

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22.4.2.30 SMB Transmit Abort Source Register(SMB_ABTSRC,0x0080)

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the SMBCTXABT register or the SMBCINT register is read. To clear Bit 9, the source of the SBYTE_NORSTRT must be fixed first; RESTART must be enabled (SMB_CON[5]=1), the SPECIAL bit must be cleared (SMB_TAR[11]), or the GC_OR_START bit must be cleared (SMB_TAR[10]). Once the source of the SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

	SMB_ABTSRC																															Base + 0x0080
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TX_FLUSH_CNT								Reserved							USER_ABRT	SLVRD_INTX	SLV_ARBLOST	SLVFLUSH_TXFIFO	ARB_LOST	ABRT_MASTER_DIS	ABRT_10B_RD_NORSTRT	SBYTE_NORSTRT	ABRT_HS_NORSTRT	SBYTE_ACKDET	ABRT_HS_ACKDET	ABRT_GCALL_READ	ABRT_GCALL_NOCK	ABRT_TXDATA_NOACK	ABRT_10ADDR2_NOACK	ABRT_10ADDR1_NOACK	ABRT_7B_ADDR_NOACK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	TX_FLUSH_CNT	This field preserves the TXFLR value prior to the last TX_ABRT event. It is cleared whenever SMB is disabled.	R
23:17	Reserved	Read as zero.	R
16	USER_ABRT	This is a master-mode-only bit. Master has detected the transfer abort	R
15	SLVRD_INTX	1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of SMB_DC register.	R
14	SLV_ARBLOST	1: Slave lost the bus while transmitting data to a remote master. SMB_ABTSRC[12] is set at the same time. **Note:** *Even though the slave never "owns" the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then SMB no longer own the bus.* Reset value: 0x0.	R
13	SLVFLUSH_TXFIFO	1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.	R

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		Reset value: 0x0.	
12	ARB_LOST	1: Master has lost arbitration, or if SMB_ABTSRC[14] is also set, then the slave transmitter has lost arbitration. **Note:** *SMB can be both master and slave at the same time.* Reset value: 0x0.	R
11	ABRT_MASTER_DIS	1: User tries to initiate a Master operation with the Master mode disabled. Reset value: 0x0.	R
10	ABRT_10B_RD_NORSTRT	1: The restart is disabled (RESTART bit (SMB_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode. Reset value: 0x0.	R
9	SBYTE_NORSTRT	To clear Bit 9, the source of the SBYTE_NORSTRT must be fixed first; restart must be enabled (SMB_CON[5]=1), the SPECIAL bit must be cleared (SMB_TAR[11]), or the GC_OR_START bit must be cleared (SMB_TAR[10]). Once the source of the SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. 1: The restart is disabled (RESTART bit (SMB_CON[5]) = 0) and the user is trying to send a START Byte. Reset value: 0x0.	R
8	ABRT_HS_NORSTRT	1: The restart is disabled (RESTART bit (SMB_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode. Reset value: 0x0.	R
7	SBYTE_ACKDET	1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Reset value: 0x0.	R
6	ABRT_HS_ACKDET	1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Reset value: 0x0.	R
5	ABRT_GCALL_READ	1: SMB in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (SMBDC[9] is set to 1). Reset value: 0x0.	R
4	ABRT_GCALL_NOACK	1: SMB in master mode sent a General Call and no slave on the bus acknowledged the General Call.	R

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		Reset value: 0x0.	
3	ABRT_TXDATA_NOACK	1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledgement from the remote slave(s). Reset value: 0x0.	R
2	ABRT_10ADDR2_NOACK	1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. Reset value: 0x0.	R
1	ABRT_10ADDR1_NOACK	1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0.	R
0	ABRT_7B_ADDR_NOACK	1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Reset value: 0x0.	R

22.4.2.31 SMB DMA Control Register(SMB_DMACR,0x0088)

The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of SMB_ENABLE.

	SMB_DMACR																															Base + 0x0088	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														TDEN	RDEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect. Read as zero.	R
1	TDEN	**Transmit DMA Enable**. This bit enables/disables the transmit DMA channel. 0: Transmit DMA disabled 1: Transmit DMA enabled Reset value: 0x0.	RW
0	RDEN	**Receive DMA Enable**. This bit enables/disables the receive DMA channel. 0: Receive DMA disabled	RW

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		1: Receive DMA enabled Reset value: 0x0.	

22.4.2.32 SMB DMA Transmit Data Level Register(SMB_DMATDLR,0x008C)

	SMB_DMACR																															Base + 0x008C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										TDLR					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect, read as zero.	R
5:0	TDLR	**DMA Transmit Data Level**. This bit field controls the level at which a DMA request is made by the transmit logic. The dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value.	R W

22.4.2.33 SMB DMA Transmit Data Level Register(SMB_DMARDLR,0x0090)

	SMB_DMACR																															Base + 0x0090
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RDLR					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect. Read as zero.	R
5:0	RDLR	**DMA Receive Data Level**. This bit field controls the level at which a DMA request is made by the receive logic. The dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1.	RW

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22.4.2.34 SMB SDA Setup Register(SMB_SDASU,0x0094)

This register controls the amount of time delay (in terms of number of APB clock periods) introduced in the rising edge of SCL, relative to SDA changing, when SMB services a read request in a slave-transmitter operation. The relevant SMB requirement is $t_{SU:DAT}$(*Note 5*)as detailed in the I2C Bus Specification(Please Google "*UM10204 pdf*").

Note: The length of setup time is calculated using [(SMB_SDASU - 1) * (apb_clk_period)], so if the user requires 10 apb clock periods of setup time, they should program a value of 11. The SMB_SDA_SETUP register is only used by the SMB when operating as a slave transmitter

Note 5: A Fast-mode SMB-bus device can be used in a Standard-mode SMB-bus system, but the requirement $t_{SU;DAT}$ >= 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max}$ + $t_{SU;DAT}$ = 1000 +250 =1250 ns (according to the Standard-mode SMB-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time(Please refer NXP Semiconductors, *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014), Table 10, Fig 38*)

	SMB_SDASU																															Base + 0x0094
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SDASU							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Name	Description	R/W
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	SDASU	SDA Setup. It is recommended that if the required delay is 1000ns, then for an APB clock frequency of 10 MHz, SMBSDASU should be programmed to a value of 11.	RW

22.4.2.35 SMB ACK General Call Register(SMB_ACKGC,0x0098)

The register controls whether SMB responds with an ACK or NACK when it receives an SMB General Call address.

	SMB_ACKGC																															Base + 0x0098
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															ACKGC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	ACKGC	ACK General Call. When set to 1, SMB responds with an ACK when it receives a General Call. When set to 0, the SMB does not generate General Call interrupts.	RW

22.4.2.36 SMB Enable Status Register(SMB_ENBST,0x009C)

The register is used to report the SMB hardware status when the SMB_ENABLE[0] is set from 1 to 0; that is, when SMB is disabled.

If SMB_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.

If SMB_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'.

Note: When SMB_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the SMB depends on SMB bus activities.

	SMB_ENBST																															Base + 0x009C		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													SLVRDLST	SLVDISB	SMBEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:3	Reserved	Writing has no effect, read as zero.	R
2	SLVRDLST	Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an SMB transfer due to the setting of SMB_ENABLE[0] from 1 to 0. When read as 1, SMB is deemed to have been actively engaged in an aborted SMB transfer (with matching address) and the data phase of the SMB transfer has been entered, even though a data byte has been responded with a NACK. **Note:** *1. If the remote SMB master terminates the transfer with a STOP condition before the SMB has a chance to NACK a transfer, and SMB_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, SMB is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer.* *2. The CPU can safely read this bit when SMB_ENABLE[0] is read as 0.* Reset value: 0x0.	R
1	SLVDISB	Slave Disabled While Busy (Transmit, Receive). This bit indicates if a	R

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		potential or active Slave operation has been aborted due to the setting of the SMB_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the SMB_ENABLE register while: (a) SMB is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, SMB is deemed to have forced a NACK during any part of an SMB transfer, irrespective of whether the SMB address matches the slave address set in SMB (SMBSAR register) OR if the transfer is completed before SMBENB is set to 0 but has not taken effect. **Note:** *1. If the remote SMB master terminates the transfer with a STOP condition before the SMB has a chance to NACK a transfer, and SMBENB has been set to 0, then this bit will also be set to 1. When read as 0, SMB is deemed to have been disabled when there is master activity, or when the SMB bus is idle.* *2. The CPU can safely read this bit when SMB_ENABLE[0] is read as 0.* Reset value: 0x0.	
0	SMBEN	When read as 1, SMB is deemed to be in an enabled state. When read as 0, SMB is deemed completely inactive.	R

22.4.2.37 SMB Filter Register(SMB_FLT,0x00A0)

This register is used to store the duration, measured in APB clock cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. This register must be programmed with a minimum value of 1.

	SMB_FLT																															Base + 0x00A0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								FLTCNT							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	FLTCNT	This register sets the duration, measured in SMB device clock cycles, of the longest value in the SCL or SDA lines that are filtered out by the spike suppression logic.	RW

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		This register can be written only when the SMB interface is disabled. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.	

22.5 Operating Flow

This section provides information on the following topics:

- "Slave Mode Operation"
- "Master Mode Operation"
- "Disabling SMB"

Note: It is important to note that the SMB should only be set to operate as an SMB Master, or SMB Slave, but not both simultaneously. This is achieved by ensuring that bit 6 (SMBSLAVE_DISABLE) and 0 (SMBMASTER_MODE) of the SMBCON register are never set to 0 and 1, respectively.

22.5.1 SMB Behavior

The SMB can be controlled via software to be either:

- An SMB master only, communicating with other SMB slaves.

OR

- An SMB slave only, communicating with one more SMB masters.

The master is responsible for generating the clock and controlling the transfer of data. The slave is responsible for either transmitting or receiving data to/from the master. The device that is receiving data, which can be either a master or a slave, sends the acknowledgement of data. As mentioned previously, the SMB protocol also allows multiple masters to reside on the SMB bus and uses an arbitration procedure to determine bus ownership.

Each slave has a unique address that is determined by the system designer. When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W) to determine if the master wants to transmit data or receive data from the slave. The slave then sends an acknowledgement (ACK) pulse after the address.

If the master (master-transmitter) is writing to the slave (slave-receiver), the receiver gets one byte of data. This transaction continues until the master terminates the transmission with a STOP condition. If the master is reading from a slave (master-receiver), the slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse. This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition.

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22.5.2 Master Mode Operation

This section includes the following topics:

- "Initial Configuration"
- "Dynamic SMBTAR or SMB10BITADDR_MASTER Update"
- "Master Transmit and Master Receive"

22.5.2.1 Configuration

To use the SMB as a master perform the following steps:

1. Disable the SMB by writing 0 to the SMBENB register. And wait for the SMBENBST.SMBEN = 0.
2. Write to the SMB_CON register to set the speed mode supported (bits 2:1). Please note that the MATP (bit4) is NOT writable. The addressing mode is controlled by Register SMB_TAR.
3. Set the expected SCL frequency. SMB_CON.SPEED = 2'b01, only SMB_SHCNT and SMBSLCNT are needed to be configured; SMB_CON.SPEED = 2'b10, only SMB_FHCNT and SMB_FLCNT are needed to be configured.

   Supposed:

   T_{scl} : SMB SCL period

   T_{SMB_clk} : SMB device clock period

   $T_{min_scl_l}$: Protocol minimum SCL low time

   $T_{min_scl_h}$: Protocol minimum SCL high time

   Then can get the equation:

   $T_{scl} = T_{SMB_clk} * ((SMB*HCNT + 8) + (SMB*LCNT + 1))$

   And the following conditions should be met:

   $(SMB*HCNT + 8) * T_{SMB_clk} >= T_{min_scl_h}$

   $(SMB*LCNT + 1) * T_{SMB_clk} >= T_{min_scl_l}$

   SMB*HCNT >= 6

   SMB*LCNT >= 8
4. Write to the SMB_TAR register the address of the SMB device to be addressed. It also indicates whether a General Call or a START BYTE command is going to be performed by SMB. The addressing mode that master starts, either 7-bit or 10-bit addressing, is controlled by the SMB10BITADDR_MASTER bit field (bit 12).
5. Enable the SMB by writing a 1 into SMB_ENABLE register. And wait for the SMB_ENBST.SMBEN = 1.
6. Now write the transfer direction and data to be sent to the SMB_DC register (This can be done

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by DMA). If the SMB_DC register is written before the SMB is enabled, the data and commands are lost as the buffers are kept cleared when SMB is not enabled.

Note: *For multiple SMB transfers, perform additional writes to the TX FIFO such that the TX FIFO does not become empty during the SMB transaction. If the TX FIFO is completely emptied at any stage and SMB_CON.STPHLD is 0, then further writes to the TX FIFO results in an independent SMB transaction.*

22.5.2.2 Dynamic SMBTAR or SMB10BITADDR_MASTER Update

The SMB supports dynamic updating of the SMBTAR (bits 9:0) and SMB10BITADDR_MASTER (bit 12) bit fields of the SMBTAR register. You can dynamically write to the SMBTAR register provided the following conditions are met:

1 SMB is not enabled (SMBENB=0);

OR

2 SMB is enabled (SMBENB=1);

AND

SMB is NOT engaged in any Master (tx, rx) operation (SMBST[5]=0);

AND

SMB is enabled to operate in Master mode (SMBCON[0]=1);

AND

there are NO entries in the TX FIFO (SMBST[2]=0).

22.5.2.3 Master Transmit and Master Receive

The SMB supports switching back and forth between reading and writing dynamically. To transmit data, write the data to be transferred to lower byte of the SMB Rx/Tx Data Buffer and Command Register (SMB_DC). The *CMD* bit (SMB_DC[8]) should be written to 0 for SMB write operations.

Subsequently, a read command may be issued by writing “don’t cares” to the lower byte of the SMBDC register, and a 1 should be written to the *CMD* bit.

22.5.3 Slave Mode Operation

This section includes the following procedures:

- “Initial Configuration”
- “Slave-Transmitter Operation for a Single Byte”
- “Slave-Receiver Operation for a Single Byte”
- “Slave-Transfer Operation For Bulk Transfers”

22.5.3.1 Initial Configuration

To use the SMB as a slave, perform the following steps:

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1 Disable the SMB by writing a ‘0’ to bit 0 of the SMBENB register.
2 Write to the SMB_SAR register (bits 9:0) to set the slave address. This is the address to which the SMB responds.
3 Write to the SMB_CON register to specify which type of addressing is supported (7- or 10-bit by setting bit 3). Enable the SMB in slave-only mode by writing a ‘0’ into bit 6 (SMBSLAVE_DISABLE) and a ‘0’ to bit 0 (MASTER_MODE).

Note: *Slaves and masters do not have to be programmed with the same type of addressing 7- or 10-bit address. For instance, a slave can be programmed with 7-bit addressing and a master with 10-bit addressing, and vice versa.*

4 Enable the SMB by writing a ‘1’ in bit 0 of the SMB_ENB register.

Note: *Depending on the reset values chosen, steps 2 and 3 may not be necessary because the reset values can be configured. For instance, if the device is only going to be a master, there would be no need to set the slave address because you can configure SMB to have the slave disabled after reset and to enable the master after reset. The values stored are static and do not need to be reprogrammed if the SMB is disabled.*

22.5.3.2 Slave-Transmitter Operation for a Single Byte

When another SMB master device on the bus addresses the SMB and requests data, the SMB acts as a slave-transmitter and the following steps occur:

1 The other SMB master device initiates an SMB transfer with an address that matches the slave address in the SMB_SAR register of the SMB.
2 The SMB acknowledges the sent address and recognizes the direction of the transfer to indicate that it is acting as a slave-transmitter.
3 The SMB asserts the RDREQ interrupt (bit 5 of the SMBINTST register) and holds the SCL line low. It is in a wait state until software responds.
   If the RDREQ interrupt has been masked, due to SMB_INTM[5] register (MRDREQ bit field) being set to 0, then it is recommended that a hardware and/or software timing routine be used to instruct the CPU to perform periodic reads of the SMB_INTST register.
   a Reads that indicate SMB_INTST[5] (RDREQ bit field) being set to 1 must be treated as the equivalent of the RDREQ interrupt being asserted.
   b Software must then act to satisfy the SMB transfer.
   c The timing interval used should be in the order of 10 times the fastest SCL clock period the SMB can handle. For example, for 400 kb/s, the timing interval is 25us.

Note: *The value of 10 is recommended here because this is approximately the amount of time required for a single byte of data transferred on the SMB bus.*

4 If there is any data remaining in the TX FIFO before receiving the read request, then the SMB asserts a TX_ABRT interrupt (bit 6 of the SMBINTST register) to flush the old data from

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the TX FIFO.

Note: *Because the SMB's TX FIFO is forced into a flushed/reset state whenever a TX_ABRT event occurs, it is necessary for software to release the SMB from this state by reading the SMB_CTXABT register before attempting to write into the TX FIFO. See register SMB_INTST for more details. If the TX_ABRT interrupt has been masked, due to of SMB_INTM[6] register (MTX_ABRT bit field) being set to 0, then it is recommended that re-using the timing routine (described in the previous step), or a similar one, be used to read the SMBINTST register.*

a Reads that indicate bit 6 (TXABT) being set to 1 must be treated as the equivalent of the TX_ABRT interrupt being asserted.
b There is no further action required from software.
c The timing interval used should be similar to that described in the previous step for the SMBINTST[5] register.

5 Software writes to the SMB_DC register with the data to be written (by writing a '0' in bit 8).
6 Software must clear the RDREQ and TX_ABRT interrupts (bits 5 and 6, respectively) of the SMBINTST register before proceeding.
If the RDREQ and/or TX_ABRT interrupts have been masked, then clearing of the SMB_INTST register will have already been performed when either the RDREQ or TXABT bit has been read as 1.
7 The SMB releases the SCL and transmits the byte.
8 The master may hold the SMB bus by issuing a RESTART condition or release the bus by issuing a STOP condition.

22.5.3.3 Slave-Receiver Operation for a Single Byte

When another SMB master device on the bus addresses the SMB and is sending data, the SMB acts as a slave-receiver and the following steps occur:

1 The other SMB master device initiates an SMB transfer with an address that matches the SMB's slave address in the SMBSAR register.
2 The SMB acknowledges the sent address and recognizes the direction of the transfer to indicate that the SMB is acting as a slave-receiver.
3 SMB receives the transmitted byte and places it in the receive buffer.

Note: *If the RX FIFO is completely filled with data when a byte is pushed, then an overflow occurs and the SMB continues with subsequent SMB transfers. Because a NACK is not generated, software must recognize the overflow when indicated by the SMB (by the RXOF bit in the SMBINTST register) and take appropriate actions to recover from lost data. Hence, there is a real time constraint on software to service the RX FIFO before the latter overflow as there is no way to re-apply pressure to the remote transmitting master. You must select a deep enough RX FIFO depth to satisfy the interrupt service interval of their system.*

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4 SMB asserts the RX_FULL interrupt (SMBINTST[2] register).

If the RX_FULL interrupt has been masked, due to setting SMB_INTM[2] register to 0 or setting SMB_TX_TL to a value larger than 0, then it is recommended that a timing routine be implemented for periodic reads of the “SMBST”. Reads of the SMB_ST register, with bit 3 (RFNE) set at 1, must then be treated by software as the equivalent of the RX_FULL interrupt being asserted.

5 Software may read the byte from the SMB_DC register (bits 7:0).

6 The other master device may hold the SMB bus by issuing a RESTART condition or release the bus by issuing a STOP condition.

22.5.3.4 Slave-Transfer Operation For Bulk Transfers

In the standard SMB protocol, all transactions are single byte transactions and the programmer responds to a remote master read request by writing one byte into the slave’s TX FIFO.

When a slave (slave-transmitter) is issued with a read request (RDREQ) from the remote master (master-receiver), at a minimum there should be at least one entry placed into the slave-transmitter’s TX FIFO.

SMB is designed to handle more data in the TX FIFO so that subsequent read requests can take that data without raising an interrupt to get more data. Ultimately, this eliminates the possibility of significant latencies being incurred between raising the interrupt for data each time had there been a restriction of having only one entry placed in the TX FIFO.

This mode only occurs when SMB is acting as a slave-transmitter. If the remote master acknowledges the data sent by the slave-transmitter and there is no data in the slave’s TX FIFO, the SMB holds the SMB SCL line low while it raises the read request interrupt (RDREQ) and waits for data to be written into the TX FIFO before it can be sent to the remote master.

If the RDREQ interrupt is masked, due to bit 5 (MRDREQ) of the SMB_INTST register being set to 0, then it is recommended that a timing routine be used to activate periodic reads of the SMB_INTST register. Reads of SMB_INTST that return bit 5 (RDREQ) set to 1 must be treated as the equivalent of the RDREQ interrupt referred to in this section.

The RDREQ interrupt is raised upon a read request, and like interrupts, must be cleared when exiting the interrupt service handling routine (ISR). The ISR allows you to either write 1 byte or more than 1 byte into the TX FIFO. During the transmission of these bytes to the master, if the master acknowledges the last byte. Then the slave must raise the RDREQ again because the master is requesting for more data.

22.5.4 Disabling SMB

The register SMB_ENBST is added to allow software to unambiguously determine when the hardware

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has completely shutdown in response to the SMB_ENABLE register being set from 1 to 0.

22.5.4.1 Procedure

1 Define a timer interval (tSMB_poll) equal to the 10 times the signaling period for the highest SMB transfer speed used in the system and supported by SMB. For example, if the highest SMB transfer mode is 400 kb/s, then this tSMB_poll is 25us.

2 Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.

3 Execute a blocking thread/process/function that prevents any further SMB master transactions to be started by software, but allows any pending transfers to be completed.

Note: *This step can be ignored if SMB is programmed to operate as an SMB slave only.*

4 The variable POLL_COUNT is initialized to zero.

5 Set SMBENB to 0.

6 Read the SMB_ENBST register and test the SMB_ENABLE[0]. Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.

7 If SMB_ENBST[0] is 1, then sleep for tSMB_poll and proceed to the previous step. Otherwise, exit with a relevant success code.

22.5.5 Summary the condition could flush TX FIFO

1. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset.
2. TX_ABRT event occurs. The TX FIFO remains in this flushed state until the register SMB_CTXABT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.
3. When act as a slave, the slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.

22.5.6 The condition could generate START, STOP and RESTART

A STOP condition is generated only when the user specifically requests it by setting bit 9 (Stop bit) of the command written to SMB_DC register. Naturally, if the last byte send out does not set bit 9 (Stop bit), the component does not generate a STOP if the Tx FIFO becomes empty; in this situation the component holds the SCL line low, stalling the bus until a new entry is available in the Tx FIFO

Figure 22-1 illustrates the behavior of the SMB when the Tx FIFO becomes empty while operating as a master transmitter, as well as showing the generation of a STOP condition.

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Figure 22-1 Master Transmitter — Tx FIFO Empties/STOP Generation

Figure 22-2 illustrates the behavior of the SMB when the Tx FIFO becomes empty while operating as a master receiver, as well as showing the generation of a STOP condition.

Figure 22-2 Master Receiver — Tx FIFO Empties/STOP Generation

Figure 22-3 and Figure 22-4 illustrate configurations where the user can control the generation of RESTART conditions on the SMB bus. If bit 10 (Restart) of the SMB_DC register is set and the restart capability is enabled (IC_RESTART_EN=1), a RESTART is generated before the data byte is written to or read from the slave. If the restart capability is not enabled a STOP followed by a START is generated in place of the RESTART. Figure 22-3 illustrates this situation during operation as a master transmitter.

Figure 22-3 Master Transmitter — Restart bit of SMB_DC is set

Figure 22-4 illustrates the same situation, but during operation as a master receiver.

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Figure 22-4 Master Receiver — Restart bit of SMB_DC is set

Figure 22-5 illustrates operation as a master transmitter where the Stop bit of the SMB_DC register is set and the Tx FIFO is not empty

Figure 22-5 Master Transmitter — Stop Bit of SMB_DC Set/Tx FIFO Not Empty

Figure 22-6 illustrates operation as a master transmitter where the first byte loaded into the Tx FIFO is allowed to go empty with the Restart bit set.

Figure 22-6 Master Transmitter — First Byte Loaded Into Tx FIFO Allowed to Empty, Restart Bit Set

Figure 22-7 illustrates operation as a master receiver where the Stop bit of the SMB_DC register is set and the Tx FIFO is not empty

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Figure 22-7 Master Receiver — Stop Bit of IC_DATA_CMD Set/Tx FIFO Not Empty

Figure 22-8 illustrates operation as a master receiver where the first command loaded after the Tx FIFO is allowed to empty and the Restart bit is set

Figure 22-8 Master Receiver — First Command Loaded After Tx FIFO Allowed to Empty/Restart Bit Set

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23 Synchronous Serial Interface(SSI)

23.1 Overview

The SSI is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom CODECS, and other devices that use serial protocols for transferring data. The SSI supports National's Microwire, Texas Instruments Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The SSI operates in master mode (the attached peripheral functions as a slave) and supports serial bit rates from 7.2 KHz to 50 MHz. Serial data formats may range from 2 to 32 bits in length. The SSI provides 128 entries deep x 32 bits wide transmit and receive data FIFOs.

The FIFOs may be loaded or emptied by the Central Processor Unit (CPU) using programmed I/O, or DMA transfers while receiving or transmitting.

23.2 Features

- 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
- Full-duplex or transmit-only or receive-only operation
- Programmable transfer order: MSB first or LSB first
- 128 entries deep x 32 bits wide transmit and receive data FIFOs
- Configurable normal transfer mode or Interval transfer mode
- Programmable clock phase and polarity for Motorola's SPI format
- Two slave select signal supporting up to 2 slave devices
- Back-to-back character transmission/reception mode
- Loop back mode for testing

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23.3 Block Diagram

Figure 23-1 SSI Block Diagram

The APB Interface is a slave interface. It is used for register configuration and data transfer.
The FIFO block is bidirectional. There are two 128x32 memory in this block, one used as transmission data buffer, and the other used for data reception.
The Clk_gen module generate the sub-clocks for the Transfer Control module.
The Transfer Control act as the handler of SPI timing generation.

23.4 Functional Description

Serial data is transferred between the processor and external peripheral through FIFO buffers in the SSI. Data transfers to system memory are handled by either the CPU (using programmed I/O) or by DMA. Operation is full duplex-separate buffers and serial data paths permit simultaneous transfers to and from the external peripheral.

Programmed I/O transmits and receives data directly between the CPU and the transmit/receive FIFO's. The DMA controller transfers data during transmit and receive operations between memory and the FIFO's.

Transmit data is written by the CPU or DMA to the SSI's transmit FIFO. The SSI then takes the data from the FIFO, serializes it, and transmits it via the SSI_DO signal to the peripheral. Data from the peripheral is received via the SSI_DIsignal, converted to parallel words and is stored in the Receive FIFO. Read operations automatically target the receive FIFO, while write operations write data to the transmit FIFO. Both the transmit and receive FIFO buffers are 128 entries deep by 17 bits wide. As the

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received data fills the receive FIFO, a programmable threshold triggers an interrupt to the Interrupt Controller. If enabled, an interrupt service routine responds by identifying the source of the interrupt and then performs one or several read operations from the inbound (receive) FIFO buffer.

23.5 Pin Description

Table 23-1 SSI Controller Pins Description

Name	I/O	GPIO	Description
SSI_CLK	Output	PC15/PC23/PD16	Serial bit-rate clock
SSI_FRM1	Output	PC16/PC24/PD17	First slave select enable
SSI_DO	Output	PC11/PC19/PD12	Transmit data
SSI_DI	Input	PC12/PC20/PD13	Receive data
SSI_CE2	Output	PC14/PC22/PD15	Second slave select enable
SSI_GPC	Output	PC13/PC21/PD14	General purpose control signal to external chip

SSI_CLK is the bit-rate clock driven from the SSI to the peripheral. SSI_CLK is toggled only when data is actively being transmitted and received.

SSI_FRM1 or SSI_CE2 are the frame signal, indicating the begin and the end of a serialized data word.

SSI_DO and SSI_DI are the Transmit and Receive serial data lines in standard SPI, SSP and NM protocol.

SSI_GPC is general-purpose control signal, synchronized with SSI_CLK, can be used for LCD control.

23.6 Data Formats

Four signals are used to transfer data between the processor and external peripheral. The SSI supports three formats: Motorola SPI, Texas Instruments SSP, and National Microwire. Although they have the same basic structure the three formats have significant differences, as described below:

1 SSI_FRM1/SSI_CE2 varies for each protocol as follows:
   - For SPI and Microwire formats, SSI_FRM1/SSI_CE2 functions as a chip select to enable the external device (target of the transfer), and is held active-low during the data transfer.
   - For SSP format, this signal is pulsed high for one serial bit-clock period at the start of each frame.

2 SSI_CLK varies for each protocol as follows:
   - For Microwire, both transmit and receive data sources switch data on the falling edge of SSI_CLK, and sample incoming data on the rising edge.
   - For SSP, transmit and receive data sources switch data on the rising edge of SSI_CLK, and sample incoming data on the falling edge.
   - For SPI, the user has the choice of which edge of SSI_CLK to use for switching outgoing

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data, and for sampling incoming data. In addition, the user can move the phase of SSI_CLK, shifting its active state one-half period earlier or later at the start and end of a frame.

While SSP and standard SPI are full-duplex protocols, Microwire use a half-duplex master-slave messaging protocol. At the start of a frame, a 1 or 2-byte control message is transmitted from the controller to the peripheral. The peripheral does not send any data. The peripheral interprets the message and, if it is a READ request, responds with requested data, one clock after the last bit of the requesting message.

The serial clock (SSI_CLK) only toggles during an active frame. At other times it is held in an inactive or idle state, as defined by its specified protocol.

23.6.1 Motorola's SPI Format Details

23.6.1.1 General Single Transfer Formats

The figures below show the timing of general single transfer format.

Figure 23-2 Standard SPI Single Character Transfer Format (PHA = 0)

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Figure 23-3 Standard SPI Single Character Transfer Format (PHA = 1)

For SSICR1.PHA = 0, when SSICR1.TFVCK = B'00, hardware ensures the first clock edge appears one SSI_CLK period after SSI_FRM1/SSI_CE2 goes valid; when SSICR1.TCKFI = B'00, hardware ensures the SSI_FRM1/SSI_CE2negated half SSI_CLK period after last clock change edge; when SSICR1.TFVCK ≠ B'00 or SSICR1.TCKFI ≠ B'00, 1/2/3 more clock cycles are inserted.

For SSICR1.PHA = 1, when SSICR1.TFVCK = B'00, hardware ensures the first clock edge appears half SSI_CLK period after SSI_FRM1/SSI_CE2 goes valid; when SSICR1.TCKFI = B'00, hardware ensures the SSI_FRM1/SSI_CE2 negated one SSI_CLK period after last clock change edge; when SSICR1.TFVCK ≠ B'00 or SSICR1.TCKFI ≠ B'00, 1/2/3 more clock cycles are inserted.
Data is sampled from SSI_DI_IO1 at every rising edge (when PHA = 0, POL = 0 or PHA = 1, POL = 1) or at every falling edge (when PHA = 0, POL = 1 or PHA = 1, POL = 0). According to Standard SPI protocol, input data should be stable at every sample clock edge.

Drive data onto output line at every rising edge (when PHA = 0, POL = 1 or PHA = 1, POL = 0) or at every falling edge (when PHA = 0, POL = 0 or PHA = 1, POL = 1).

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23.6.1.2 Back-to-Back Transfer Formats

Figure 23-4 Standard SPI Back-to-Back Transfer Format

For Motorola's SPI format transfers those continuous characters are exchanged during SSI_FRM1/SSI_CE2being valid, the timing is illustrated in the figure (SSICR1.ITFRM = 0).

Back-to-back transfer is performed as transmit-only/full-duplex operation when transmit-FIFO is not empty before the completion of the last character's transfer or performed as receive-only operation.

23.6.1.3 Frame Interval Mode Transfer Format

When in interval mode (SSIITR. IVLTM ≠ '0'), SSI always wait for an interval time (SSIITR.IVLTM), transfer fixed number of characters (SSIICR), then repeats the operation.

When SSICR0.RFINE = 1, if transmit-FIFO is still empty after the interval time, receive-only transfer will occur.

During interval-wait time, SSI stops SSI_CLK, and when SSICR1.ITFRM = 0 it negates the SSI_FRM1/SSI_CE2, when SSICR1.ITFRM = 1 it keeps asserting the SSI_FRM1/SSI_CE2.

For transfers finished with transmit-FIFO empty, if the SSI transmit-FIFO is empty before fixed number of characters being loaded to transfer (SSICR1.UNFIN must be 1), then the SSI will set SSISR.UNDR = 1; if enabled, it'll send out a SSI under-run interrupt. At the same time, SSI will hold the SSI_FRM1/SSI_CE2 and SSI_CLK signals at current status and wait for the transmit-FIFO filling. The SSI will continue transfer after transmit-FIFO being filled. The SSI always stops after completion of fixed number of characters' transfer (SSICR1.UNFIN must be 0) with transmit-FIFO empty.

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For transfers finished by SSICR0.RFINC being valid set, the SSI will stop after finished current character transfer and needn't wait for a whole completion of fixed number of characters' transfer.

Two Interval transfer mode are illustrated in the following figures. In these timing diagram, SSICR1.PHA = 0, SSICR1.POL = 0 and SSIICR = 0.

Figure 23-5 Standard SPI Frame Interval Mode Transfer Format (ITFRM = 0, ITFRM= 0)

Figure 23-6 Standard SPI Frame Interval Mode Transfer Format (ITFRM = 1, ITFRM = 1)

23.6.2 TI's SSP Format Details

In this format, each transfer begins with SSI_FRM1 pulsed high for one SSI_CLK period. Then both master and slave drive data at SSI_CLK's rising edge and sample data at the falling edge. Data are transferred with MSB first or LSB first. At the end of the transfer, SSI_DO retains the value of the last bit sent through the next idle period.

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Figure 23-7 TI's SSP Single Transfer Format

Figure 23-8 TI's SSP Back-to-back Transfer Format

23.6.3 National Microwire Format Details

It supports format 1 and format 2.

Format		Drive Edge	Sample Edge
NM1	Master	↓	↑
	Slave	↓	↑
NM2	Master	↓	↓
	Slave	↑	↑

If format 1 is selected, both master and slave drive data at SSI_CLK falling edge and sample data at the rising edge.

If format 2 is selected, master drive and sample data at SSI_CLK falling edge, slave drive and sample data at SSI_CLK rising edge.

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SSI_CLK goes high midway through the command's MSB (or LSB) and continues to toggle at the bit rate. One bit clock (format 1) or half bit clock (format 2) period after the last command bit, the external slave must return the serial data requested, with MSB first (or LSB first) on SSI_DI.

SSI_FRM1/SSI_CE2 de-asserts high half clock (SSI_CLK) period (and 1/2/3 additional clock periods) later.

Format 1 support back-to-back transfer, the start and end of back-to-back transfers are similar to those of a single transfer. However, SSI_FRM1/SSI_CE2 remains asserted throughout the transfer. The end of a character data on SSI_DI is immediately followed by the start of the next command byte on SSI_DO.

Figure 23-9 National Microwire Format 1 Single Transfer

Figure 23-10 National Microwire Format 1 Back-to-back Transfer

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Figure 23-11 National Microwire Format 2 Read Timing

Figure 23-12 National Microwire Format 2 Write Timing

23.7 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

5. Register Address = Base + Address offset
6. The registers can be read and written by APB bus
7. Register read/write attribute

R - Read only

W - Write only

RW - read and write

RCW - read and write, but clear to 0 by read

RSW - read and write, but set to 1 by read

RWC - read and write, clear to 0 by write 1, write 0 has no effect

RWS - read and write, set to 1 by write 1, write 0 has no effect

RC - read only, and clear to 0 by read

RS - read only, and set to 1 by read

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SPEC - special access method, relate to its description

8. Reset Value

1 - reset to 1

0 - reset to 0

? - value unknown after reset

23.7.1 Registers Mapping

Table 23-2 Registers Memory Map Base Address

Name	Base	Description
SSI0	0x10043000	Address base of SSI0
SSI1	0x10044000	Address base of SSI1

The SSI is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 23-3 SSI Serial Port Registers Map

Name	RW	Reset Value	Address Offset	Access Size
SSIDR	RW	0x????_????	0x0000	32
SSICR0	RW	0x0000_0000	0x0004	32
SSICR1	RW	0x0008_7830	0x0008	32
SSISR	RW	0x0000_0098	0x000C	32
SSIITR	RW	0x????_0000	0x0010	16
SSIICR	RW	0x????_????	0x0014	8
SSIGR	RW	0x????_??00	0x0018	16
SSIRCNT	RW	0x0000_0000	0x001C	32

23.7.2 Register and Fields Description

23.7.2.1 SSI Data Register(SSIDR,0x0000)

	SSIDR																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D31-D17															GPC/D16	D15-10															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	D31-D17	D31-D17 to be written to/read from Transmit/Receive FIFO.	RW

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16	GPC/D16	This bit can be used as normal data bus bit 16 or GPC bit alternatively. When it is used as normal data bus bit, it's readable / writable; when SSI_GPC is used, it is GPC bit for SSI_GPC pin output and it's write-only.	RW
15:0	D15-D0	D15-D0 to be written to/read from Transmit/Receive FIFO. When the transfer frame length is less than 17-bit, received data is automatically right justified in the receive-FIFO and the upper unused bits are filled with '0'. For transmission, the upper unused bits of the data written into SSIDR is ignored by the transmit logic. **Note:** "upper unused bits" does not include the SSIDR.GPC bit. National Microwire format includes format 1 and format2, when national Microwire format 2 is selected, Bit 16 of SSIDR is defined as read/write operation judge bit, if it is 0, bit 15~0 represent one read command; if it is 1, bit 15~0 represent one write command and following is the written data. So the maximum length of one command (is defined in MCOM) is 16, the maximum length of one written or read data (is defined in FLEN) can be 17. Transmit-FIFO only contain one read operation command once, or one write operation command and its data once, after transmit-FIFO is empty, next command can be filled in transmit-FIFO.	RW

23.7.2.2 SSI Control Register0(SSICR0,0x0004)

	SSICR0																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												TENDIAN		RENDIAN		SSIE	TIE	RIE	TEIE	REIE	LOOP	RFINE	RFINC	EACLRUN	FSEL	Reserved	VRCNT	TFMODE	TFLUSH	RFLUSH	DISREV
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as '0'.	R
19:18	TENDIAN	Transfer endian 0: Most significant byte in a word first, most significant bit in a byte first. 1: Most significant byte in a word first, least significant bit in a byte first. 2: Least significant byte in a word first, least significant bit in a byte first. 3: Least significant byte in a word first, most significant bit in a byte	RW

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		first.	
17:16	RENDIAN	Receive endian 0: Most significant byte in a word first, most significant bit in a byte first. 1: Most significant byte in a word first, least significant bit in a byte first. 2: Least significant byte in a word first, least significant bit in a byte first. 3: Least significant byte in a word first, most significant bit in a byte first	RW
15	SSIE	This bit is used to enable/disable SSI module. 0: disable; 1: enable. Clearing SSIE will not reset SSI FIFO, SSICR0, SSICR1, SSIGR, SSIITR and SSIICR automatically. Software should ensure the FIFOs/registers are properly configured and be flush/reset manually when necessary before enabling SSI.	RW
14	TIE	This bit enables/disables the transmit-FIFO half-empty interrupt TXI and the tdreq signal to PDMA. 0: disable; 1: enable for the TXI interrupt 1: disable; 0: enable for the tdreq signal to PDMA. Note: the TXI interrupt and tdreq signal to PDMA can't work at the same time.	RW
13	RIE	This bit enables/disables the receive-FIFO half-full interrupt RXI and the rdreq signal to PDMA. 0: disable; 1: enable.for the RXI interrupt 1: disable; 0: enable for the rdreq signal to PDMA. Note: the RXI interrupt and rdreq signal to PDMA can't work at the same time.	RW
12	TEIE	This bit enables/disables the transmit-error interrupt TEI. 0: disable; 1: enable.	RW
11	REIE	This bit enables/disables the receive-error interrupt REI. 0: disable; 1: enable.	RW
10	LOOP	Used for test purpose. In loop mode, the output of SSI transmit shift register is connected to input of SSI receive shift register internally. The data received should be the same as the data transmitted. And do not output any valid signals on the pins. 0: normal SSI mode; 1: LOOP mode.	RW

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<table>
<tr><td>9</td><td>RFINE</td><td>Receive finish control enable.
0: disable; 1: enable.
For SSICR1.FMAT = B’010 (National Microwire format 1 is selected), SSICR0.RFINE must be 0.</td><td>The receive finish condition list below:
<table><tr><th>RFINE</th><th>RFINC</th><th>Receive Finish Condition</th></tr><tr><td>0</td><td>x</td><td>Same as transmit completion condition (transmit-fifo is empty and SSICR1.UNFIN = 0)</td></tr><tr><td>1</td><td>0</td><td>Receive continue</td></tr><tr><td>1</td><td>1</td><td>Receive finish</td></tr></table></td><td>RW</td></tr>
<tr><td>8</td><td>RFINC*</td><td>Receive finish control bit.
0: receive continue
1: receive finished</td><td></td><td>RW</td></tr>
<tr><td>7</td><td>EACLRUN</td><td colspan="2">0: don’t auto clear under flag, software clear under
1: software auto clear under flag when tfifo don’t empty</td><td>RW</td></tr>
<tr><td>6</td><td>FSEL</td><td colspan="2">This bit sets the frame signal to be used for slave select. The unselected frame signal always output invalid level.
0: SSI_FRM1 is selected
1: SSI_CE2_IO2 is selected</td><td>RW</td></tr>
<tr><td>5</td><td>Reserved</td><td colspan="2">Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>4</td><td>VRCNT</td><td colspan="2">Receive counter (RCNT) valid flag.
0: SSIRCNT.RCNT will be ignored.
1: SSIRCNT.RCNT will be used.</td><td>RW</td></tr>
<tr><td>3</td><td>TFMODE</td><td colspan="2">0: new tfifo empty mode(with Grey code convert, recommended)
1: old tfifo empty mode(not recommended)</td><td>RW</td></tr>
<tr><td>2</td><td>TFLUSH</td><td colspan="2">Flush the transmit FIFO when set to 1.
Always return 0 after one cycle of pclk.</td><td>RW</td></tr>
<tr><td>1</td><td>RFLUSH</td><td colspan="2">Flush the receive FIFO when set to 1.
Always return 0 after one cycle of pclk</td><td>RW</td></tr>
<tr><td>0</td><td>DISREV</td><td colspan="2">Receive function enable.
0: enable.
1: disable.</td><td>RW</td></tr>
</table>

Note:

***:** When transmitting finished or for receive-only operation, transmit function can be disabled and this bit is used to control receiving completion, and the SSI will consume less power.

When the finish condition is set, the receiving will complete after present character is completely shifted in, then the SSI will stop the SSI_CLK and negate the SSI_FRM1 / SSI_CE2_IO2 if necessary. To make sure present transfer is completed, user must read and get SSISR.END = 1 (or SSISR.BUSY = 0).

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23.7.2.3 SSI Control Register1(SSICR1,0x0008)

	SSICR1																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRMHL		TFVCK		TCKFI		GPCMD	ITFRM	UNFIN	FMAT			TTRG				MCOM				RTRG				FLEN					GPCHL	PHA	POL
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	1	1	0	0	0	0

Bits	Name	Description	RW
31:30	FRMHL	Frame valid level select, FRMHL [1: 0] correspond to SSI_CE2_IO2 and SSI_FRM1 respectively. **FRMHL[1:0]** / **Description** 00 — SSI_FRM1 is low level valid and SSI_CE2_IO2 is low level valid — Initial value 01 — SSI_FRM1 is high level valid and SSI_CE2_IO2 is low level valid 10 — SSI_FRM1 is low level valid and SSI_CE2_IO2 is high level valid 11 — SSI_FRM1 is high level valid and SSI_CE2_IO2 is high level valid	RW
29:28	TFVCK	Time from frame valid to clock start. When TFVCK = B'00, the time is fixed half or one SSI_CLK cycle according to SSICR1.POL and SSICR1.PHA configuration. For SSICR1.FMAT = B'001, SSICR1.TFVCK is ignored. **TFVCK[1:0]** / **Description** 00 — half or one SSI_CLK cycle delay time — Initial value 01 — 1 more SSI_CLK cycle delay is added 10 — 2 more SSI_CLK cycle delay is added 11 — 3 more SSI_CLK cycle delay is added	RW
27:26	TCKFI	Time from clock stop to frame invalid. When TCKFI = B'00, the time is fixed one SSI_CLK or half SSI_CLK cycle according to SSICR1.POL and SSICR1.PHA configuration. For SSICR1.FMAT = B'001, SSICR1.TFVCK is ignored. **TCKFI[1:0]** / **Description** 00 — half or one SSI_CLK cycle delay — Initial value 01 — 1 more SSI_CLK cycle delay is added 10 — 2 more SSI_CLK cycle delay is added 11 — 3 more SSI_CLK cycle delay is added	RW
25	GPCMD	SSI_GPC in normal mode or special mode, 0:normal; 1:special In normal mode, SSI_GPC level is related to SSIDR;	RW

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<table>
<tr><td></td><td></td><td>In special mode, SSI_GPC can be configured, and its level is GPCHL.</td><td></td></tr>
<tr><td>24</td><td>ITFRM</td><td>Frame during interval, selects if the Frame (SSI_FRM1 /SSI_CE2_IO2) signal is negated or not during interval time at Interval Mode (SSICR1.FMAT = B’000(quad and dual spi?) and SSIITR.IVLTM ≠ H’0000). It’s ignored at Normal Mode.
0: SSI_FRM1 /SSI_CE2_IO2 de-asserts during interval time at Interval Mode
1: SSI_FRM1 /SSI_CE2_IO2 keeps asserted during interval time at Interval Mode</td><td>RW</td></tr>
<tr><td>23</td><td>UNFIN</td><td>This bit controls whether the SSI finishes transmission or wait for data filling (underrun happen) after all data in transmit-FIFO are sent out during transfer. This bit must be cleared to 0 when SSICR1.FMAT = B’001. (TI’s SSP format)
0: TxFIFO empty means end of transmission
1: Transmission didn’t finish when transmit-FIFO is empty, SSI underrun error would occur and SSI waits for data filling; SSI_CLK and SSI_FRM1 /SSI_CE2_IO2 keeps asserted, SSI_CLK stop at the current level
Note: For TxFIFO empty before any transfer after SSI enabled, if SSICR1.UNFIN = 1 or SSICR0.RFINE = 0, SSI will wait till TxFIFO isn’t empty then start to transfer and no underrun error will occur; if SSICR1.UNFIN = 0 and SSICR0.RFINE = 1, after transmit-FIFO become empty, SSI will start a receive-only transfer.</td><td>RW</td></tr>
<tr><td>22:20</td><td>FMAT</td><td>These bits set the operating transfer format.
<table>
<tr><th>FMAT</th><th>Description</th><th></th></tr>
<tr><td>000</td><td>Motorola’s SPI format(standard)</td><td>Initial value</td></tr>
<tr><td>001</td><td>TI’s SSP format</td><td></td></tr>
<tr><td>010</td><td>National Microwire 1 format</td><td></td></tr>
<tr><td>011</td><td>National Microwire 2 format</td><td></td></tr>
</table></td><td>RW</td></tr>
<tr><td>19:16</td><td>TTRG</td><td>These bits define the transmit-FIFO half-empty threshold value, which when equal or less characters left in transmit-FIFO, the SSISR.TFHE will be set to ‘1’.
0000: less than or equal to 1
n: less than or equal to nx8
Note: 0000 is not recommended</td><td>RW</td></tr>
<tr><td>15:12</td><td>MCOM</td><td>Defines the length of command.
Only used when SSICR1.FMAT = b’010 or b’011 (National Microwire format 1 or 2 is selected).
The command length is (MCOM + 1).
Initial value is b’0111.</td><td>RW</td></tr>
<tr><td>11:8</td><td>RTRG</td><td>These bits define the receive-FIFO half-full threshold value, which when equal or more characters received in receive-FIFO, the SSISR.RFHF</td><td>RW</td></tr>
</table>

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		will be set to '1'. 0000: more than or equal to 1 n: more than or equal to nx8	
7:3	FLEN	These bits set the bit length of every character to be transmitted/received. The maximum data length can be configured is 32 bits. For data length longer than 17 bits (multiples of the SSICR1.FLEN configured length), the software should ensure properly processing. When SSI_GPC pin is used, the FLEN shouldn't be configured as B'01111 (17-bit data). When TI SSP mode is selected (FMAT = 2'b001), 2-bit data length (FLEN = 0) isn't supported. The bit length of one data = FLEN + 2 **Note:** In Dual SPI/Quad SPI, the bit length should be multiple of 2/4. If it is not proper, the BLI interrupt will be generated.	RW
2	GPCHL	SSI_GPC level. This bit is valid when GPCMD is high 0:low; 1:high	RW
1	PHA	This bit sets the phase of the SSI_CLK from the beginning of a data frame for SPI format (SSICR1.FMAT = B'000 or B'100 or B'101). 0: The leading edge of SSI_CLK is used to sample data from SSI_DI_IO1 after the SSI_FRM1 /SSI_CE2_IO2 goes valid, it is initial value 1: The leading edge of SSI_CLK is used to drive data onto SSI_DO_IO0 after the SSI_FRM1 /SSI_CE2_IO2 goes valid	RW
0	POL	SSI_CLK polarity for SPI format during idle state. (SSICR1.FMAT = B'000 or B'100 or B'101). 0: SSI_CLK keeps low level when idle 1: SSI_CLK keeps high level when idle	RW

23.7.2.4 SSI Status Register(SSISR,0x000C)

	SSISR																															Base + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TFIFO-NUM								RFIFO-NUM								END	BUSY	TFF	RFE	TFHE	RFHF	TUNDR	ROVER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	TFIFO-NUM	These bits indicate the Characters Number in Transmit-FIFO.	R

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15:8	RFIFO-NUM	These bits indicate the Characters Number in Receive-FIFO.	R
7	END	This bit indicates transfer end status. It is the inverse of SSISR.BUSY when transfer is in process, but it'll keep cleared at interval time before transfer is completed. It'll be set when transfer finished. When SSICR0.FIE is set, It will generate the XFI interrupt. This interrupt will be auto cleared to '0' after reading SSISR.	R
6	BUSY	This bit indicates SSI's working status. 0: SSI is idle or at interval time 1: Transmission and/or reception is in process	R
5	TFF	This bit denotes transmit-FIFO is full or not. 0: Transmit-FIFO is not full 1: Transmit-FIFO is full	R
4	RFE	This bit denotes receive-FIFO is empty or not. 0: Receive-FIFO is not empty 1: Receive-FIFO is empty	R
3	TFHE	This bit denotes whether the characters number in transmit-FIFO being less or equal to SSICR1.TTRG. 0: The data in transmit-FIFO is more than the condition set by SSICR1.TTRG 1: The data in transmit-FIFO meets the condition set by SSICR1.TTRG When SSICR0.TIE is set , it will generate the TXI interrupt	R
2	RFHF	This bit denotes whether the characters number in receive-FIFO being more or equal to the number set by SSICR1.RTRG. 0: The data in receive-FIFO is less than the condition set by SSICR1.RTRG 1: The data in receive-FIFO meets the condition set by SSICR1.RTRG When SSICR0.RIE is set, it will generate the RXI interrupt	R
1	TUNDR	Transmit-FIFO underrun status. When underrun happens, SSI set this bit and keeps the current status of SSI_CLK and SSI_FRM1/SSI_CE2_IO2, waiting for transmit-FIFO filling. 0: Transmit-FIFO underrun has not occurred 1: Transmit-FIFO underrun was occurred When SSICR0.TEIE is set, it will generate the TEI interrupt. Write '0' to clear this bit, writing '1' has no effect	RW
0	ROVER	Receive-FIFO overrun status, new received data will lose. 0: Receive-FIFO overrun has not occurred 1: Receive-FIFO overrun was occurred; When SSICR0.REIE is set, it will generate the REI interrupt. Write '0' to clear this bit, writing '1' has no effect	RW

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23.7.2.5 SSI Interval Time Control Register(SSIITR,0x0010)

	SSIITR																																Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CNTCLK	IVLTM														
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as indeterminate figure.	R
15	CNTCLK	Counting clock source select. 0: Use SSI bit clock (SSI_CLK) as the interval counter clock source 1: Use 32K clock as the interval counter clock source	RW
14:0	IVLTM	Interval time set, set the cycle number of counting clock source for desired interval time. When SSIITR.IVLTM = 0x0000, normal mode is selected, and SSIITR.CNTCLK and SSIICR are ignored. When SSIITR.IVLTM ≠ 0x0000, interval mode(not supported by Dual and Quad mode) is selected. The interval time is calculated as follows: *Interval time ≈ [CNTCLK clock period] *[Value of IVLTM]* The actual interval time is as follow: When SSIITR.CNTCLK = 0: *Interval time = [CNTCLK clock period] * [Value of IVLTM] + 3 * dev_clk period* When SSIITR.CNTCLK = 1: *Interval time ≥ [CNTCLK clock period] * [Value of IVLTM + 1] + 1 * dev_clk period;* *Interval time ≤ [CNTCLK clock period] * [Value of IVLTM + 2] + 2 * dev_clk period*	RW

23.7.2.6 SSI Interval Character-per-frame Control Register(SSIICR,0x0014)

	SSIICR																																Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													ICC		
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0

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Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as indeterminate figure.	R
2:0	ICC	Sets the fixed number of characters to be transmitted / received each time during SSI_CLK changing (and SSI_FRM1 /SSI_CE2_IO2 asserting) in interval mode for SSICR1.FMAT = B'000 (Motorola's standard SPI format is selected). SSIICR is ignored for SSICR1.FMAT ≠ B'000. The desired transfer number of characters-per-frame is (SSIICR set value + 1).	RW

23.7.2.7 SSI Clock Generator Register(SSIGR,0x0018)

	SSIGR																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								CGV							
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as indeterminate figure.	R
7:0	CGV	Sets the frequency of serial bit clock (SSI_CLK). The serial bit clock (SSI_CLK) is generated by dividing device-clock as follows: F_{SSI_CLK} = [Frequency of device clock] / (2 * (CGV + 1)) Device clock is generated in CPM module. The value in SSIGR can be set from 0 to 255, and initialized to 0x0000 on power-on reset.	RW

23.7.2.8 SSI Receive Counter Register(SSIRCNT,0x001C)

	SSIRCNT																															Base + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	RCNT	Number of data to be received. If SSICR1.UNFIN = 0 and SSICR0.RFINE = 1, after transmit-FIFO become empty, SSI will start a receive-only transfer. If SSICR0.VRCNT = 1, a special internal counter will be increased automatically. When the value of the internal counter equals to the RCNT, the receiving operation will be stopped automatically.	RW

23.8 Software Guideline

23.8.1 Common flow

The initial steps are:

1) set GPIO
2) disable interrupt (or not) by setting SSICR0
3) clear SSISR (write 0x0, clear interrupt, FIFO state and working condition)
4) flush FIFO (write SSICR0.xFLUSH once for each FIFO)
5) select the counting clock by configuring SSIITR
6) configure SSIGR (set the frequency of serial bit clock)
7) configure SSICR1 (set valid level of CE signals, set head and end delay of the transfer, set state of CE signals in interval time, select protocols, set threshold of FIFO, set bit length, etc.)
8) configure SSIICR (set the fixed number of characters to be transmit/received each time during SSI_CLK changing in interval mode)
9) configure SSIRCNT (number of data to be received)
10) configure SSICR0 (the start trigger is in this register)

Note: the frequency of dev_clk should not be 4 times or more higher than PCLK

23.8.2 Interrupt Operation

In SSI, there are TXI, TEI, TFI, RXI, REI 4 interrupts, all these interrupts are combined together to make one SSI interrupt, which can be masked by writing ‘1’ into corresponding mask bit in INTC interrupt mask register (IMR). See Table 23-4.

Table 23-4 SSI Interrupts

Operation	Condition	Flag Bit	Mask Bit	Interrupt	DMAC Activation
Transmit	T-FIFO is half-empty or less	SSISR.TFHE	SSICR0.TIE	**TXI**	Possible
	Transmit under-run error	SSISR.TUNDR	SSICR0.TEIE	**TEI**	Impossible

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Receive	R-FIFO is half-full or more	SSISR.RFHF	SSICR0.RIE	**RXI**	Possible
	Receive overrun error	SSISR.ROVER	SSICR0.REIE	**REI**	Impossible

Either SSISR.TFHE or SSISR.RFHF can activate DMA transferring when corresponding individual interrupt mask bit in SSICR0 is cleared (masked) and DMA is enabled and configured.

23.9 Index

Name	**Description**
APB	Advanced Microcontroller Bus Architecture
CPU	Central Processing Unit
Endian	The convention used to interpret the bytes making up a data word when those bytes are stored in computer memory. See Endianness at Wikipedia
FIFO	First In, First Out, a method for organizing and manipulating a data buffer
LSB	See Endian
MSB	See Endian
SPI	Serial Peripheral Interface
Standard SPI	See SPI

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24 Universal Asynchronous Receiver/Transmitter (UART)

24.1 Overview

This chapter describes the universal asynchronous receiver/transmitter (UART) serial ports. There are two UARTs: All UARTs use the same programming model. Each of the serial ports can operate in interrupt-based mode or DMA-based mode.

The Universal asynchronous receiver/transmitter (UART) is compatible with the 16550-industry standard and can be used as slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) serial infrared specification 1.1.

24.2 Features

- Full-duplex operation
- 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
- 64x8 bit transmit FIFO and 64x11bit receive FIFO
- Transmission, reception and line status Independently
- Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
- Separate DMA requests for transmit and receive data services in FIFO mode
- Supports modem flow control by software or hardware
- Slow infrared asynchronous interface that conforms to IrDA specification

24.3 Block Diagram

Figure 24-1 UART DATA Controller Block Diagram

As shown in UART DATA Controller Block Diagram，the two part includes receiving data and sending data in UART; From PIN to receive the data processing and put it on the APB bus. For the transmission direction, UART gets the data from the APB bus and sent to the PIN.

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24.4 Functional Description

24.4.1 Full-duplex operation

UART bidirectional communication，can realize full duplex transmission and reception.

24.4.2 The meaning of all bits

1.start : first sends a signal to a logic "0", to indicate the beginning of transmissiong or reception character.
2.data bit : after the start bit. data bits can be 5,6,7,8etc, constitute a character. Began to transfer from the lowest.
3.parity bit : it is optional and used to check the accuracy of data transmission and reception.
4.stop bit : it marks the end of a character data. can be high level 1,1.5,2. stop bit is not only the end of said transmission, and provides computer correction clock synchronization opportunity.
5.idle bit : In a logic "1" state, said the current line without data transfer.

24.4.3 RFIFO and TFIFO

TFIFO is 64*8bit transmission FIFO; RFIFO is 64*11bit receiving FIFO. they used to cache data.
The data in the UART registers(temporary memory block), and then through the FIFO transmitted to the serial device, without the FIFO, the information will become be, may not transfer to Modem.

24.4.4 Transmission, reception and line status Independently

Independently controlled transmit, receive (data ready or timeout), line status interrupts

24.4.5 Slow infrared asynchronous interface

UART also contains a IrDA serial infrared(SIR) encoder/decoder module. IrDA SIR module is used to convert between asynchronous UART data stream and a half duplex serial SIR interface. The SIR module's task is to give the UART to provide a digital output code and a decoding input . UART signal pin and a infrared transceiver connected to implement IrDA SIR physical layer connection.

24.5 Pins Description

Table 24-1 UART Pins Description

Name	Type	Description
RxD	Input	Receive data input
TxD	Output	Transmit data output
CTS_	Input	Clear to Send --- Modem Transmission enabled
RTS_	Output	Request to Send --- UART Transmission request

NOTE: UART0 support RxD, TxD, RTS_, CTS_; UART1 support RxD, TxD.

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24.6 Data Format Description

Figure 24-2 UART Frame Structure Diagram

As shown in UART Frame Structure Diagram, the frame data from left to right transmission. The start bit and parity bit are all 1bit; Data bits and stop bits can be changed, so data bits range is 5bit to 8bit; stop bits range is 1bit ,1.5bit and 2bit;

24.7 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   RC- Read only, and Clear to 0 by read
   RS- Read only, and Set to 1 by read
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

24.7.1 Register Memory Map

There are 2 UART controllers in chip, name UART0, UART1 respectively. The base address of UARTS(s) as follows:

Table 24-2 Registers Memory Map Base Address

Name	Base	Description
UART0	0x10030000	Address base of UART0
UART1	0x10031000	Address base of UART1

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The UART is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 24-3 UART Registers Map

Name	RW	Reset Value	Address Offset	Access Size
URBR	R	0x0000_00??	0x0000	32
UTHR	W	0x0000_00??	0x0000	32
UDLLR	RW	0x0000_0000	0x0000	32
UDLHR	RW	0x0000_0000	0x0004	32
UIER	RW	0x0000_0000	0x0004	32
UIIR	R	0x0000_0001	0x0008	32
UFCR	W	0x0000_0000	0x0008	32
ULCR	RW	0x0000_0000	0x000C	32
UMCR	RW	0x0000_0000	0x0010	32
ULSR	R	0x0000_0060	0x0014	32
UMSR	R	0x0000_0000	0x0018	32
USPR	RW	0x0000_0000	0x001C	32
ISR	RW	0x0000_0000	0x0020	32
UMR	RW	0x0000_0000	0x0024	32
UACR	RW	0x0000_0000	0x0028	32
URCR	R	0x0000_00??	0x0040	32
UTCR	R	0x0000_00??	0x0044	32

24.7.2 Register and Fields Description

24.7.2.1 UART Receive Buffer Register(URBR,0x0000)

The read-only URBR is corresponded to one level 11bit buffer in non-FIFO mode and a 32x11bit FIFO that holds the character(s) received by the UART. Bits in URBR are right justified when being configured to use fewer than eight bits, and the rest of most significant data bits are zeroed and the most significant three bits of each buffer are the status for the character in the buffer. If ULSR.DRY is 0, don't read URBR, otherwise wrong operation may occur.

	URBR																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								URBR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

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Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	URBR	8-bit UART receive read data.	R

NOTE:

The URBR register is valid when ULCR register's field DLAB = 0 and cpu to request read operation;

24.7.2.2 UART Transmit Hold Register(UTHR,0x0000)

The write-only UTHR is corresponded to one level 8 bit buffer in non-FIFO mode and a 32x8bit FIFO in FIFO mode that holds the data byte(s) to be transmitted next.

	UTHR																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								UTHR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	UTHR	8-bit UART transmit write hold data.	W

NOTE:

The UTHR register is valid when ULCR register's field DLAB = 0 and cpu to request writing operation;

24.7.2.3 UART Divisor Latch Low Register (UDLLR,0x000)

UART Divisor Latch registers, UDLLR/UDLHR together compose the divisor for the programmable baud rate generator that can take the UART device clock and divide it by 1 to (2^{16} – 1).

The UART device source clock is EXCLK or EXCLK/2 that is determined by CPCCR.ECS. UDLHR/UDLLR stores the high/low 8-bit of the divisor respectively. Load these divisor latches during initialization to ensure that the baud rate generator operates properly. If both Divisor Latch registers are 0, the 16X clock stops.

If you don't set UMR and UACR, UART will work at normal mode with the specified frequency. The relationship between baud rate and the value of Divisor is shown by the formula when UMR and UACR are not set:

Baud Rate = (UART device clock) / (16 * **Divisor**)

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	UDLLR																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								DLL_8bit							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	DLL_8bit	Low 8-bit divisor Latch	RW

NOTE:

The UDLLR register is valid when ULCR register's field DLAB = 1;

24.7.2.4 UART Divisor Latch High Register (UDLHR,0x0004)

The interpretation of the same with UDLLR.

	UDLHR																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								DLH_8bit							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	DLH_8bit	high 8-bit divisor Latch	RW

NOTE:

The UDLHR register is valid when ULCR register's field DLAB = 1;

24.7.2.5 UART Interrupt Enable Register (UIER,0x0004)

The UART Interrupt Enable Register (UIER) contains the interrupt enable bits for the five types of interrupts (receive data ready, timeout, line status, and transmit data request, and modem status) that set a value in UIIR.

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	UIER																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											RTOIE	MSIE	RLSIE	TDRIE	RDRIE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4	RTOIE	**Receive Timeout Interrupt Enable.** 0: Disable the receive timeout interrupt 1: Enable the receive timeout interrupt Timeout means the URDR (FIFO mode) is not empty but no character has received for a period of time T: T (bits) = 4 X Word length + 12.	RW
3	MSIE	**Modem Status Interrupt Enable.** 0: Disable the modem status interrupt 1: Enable the modem status interrupt	RW
2	RLSIE	**Receive Line Status Interrupt Enable.** 0: Disable receive line status interrupt 1: Enable receive line status interrupt	RW
1	TDRIE	**Transmit Data Request Interrupt Enable.** 0: Disable the transmit data request interrupt 1: Enable the transmit data request interrupt	RW
0	RDRIE	**Receive Data Ready Interrupt Enable.** 0: Disable the receive data ready interrupt 1: Enable the receive data ready interrupt	RW

NOTE:

The UIER register is valid when ULCR register's field DLAB = 0;

24.7.2.6 UART Interrupt Identification Register (UIIR,0x0008)

The read-only UART Interrupt Identification Register (UIIR) records the prioritized pending interrupt source information. Its initial value after power-on reset is 0x01.

	UIIR																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								FFMSEL		Reserved		INID			INPEND
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:8</td><td>Reserved</td><td>Writing has no effect.
Read as zero.</td><td>R</td></tr>
<tr><td>7:6</td><td>FFMSEL</td><td>FIFO Mode Select.
0b00: Non-FIFO mode
0b01: Reserved
0b10: Reserved
0b11: FIFO mode</td><td>R</td></tr>
<tr><td>5:4</td><td>Reserved</td><td>Writing has no effect.
Read as zero.</td><td>R</td></tr>
<tr><td>3:1</td><td>INID</td><td>Interrupt Identifier.
These bits identify the current highest priority pending interrupt.
<table>
<tr><td>INID</td><td>Description</td></tr>
<tr><td>0b000</td><td>Modem Status</td></tr>
<tr><td>0b001</td><td>Transmit Data Request</td></tr>
<tr><td>0b010</td><td>Receive Data Ready</td></tr>
<tr><td>0b011</td><td>Receive Line Status</td></tr>
<tr><td>0b100</td><td>Reserved</td></tr>
<tr><td>0b101</td><td>Reserved</td></tr>
<tr><td>0b110</td><td>Receive Time Out</td></tr>
<tr><td>0b111</td><td>Reserved</td></tr>
</table>
See Table 24-4 for details.</td><td>R</td></tr>
<tr><td>0</td><td>INPEND</td><td>Interrupt Pending.
0: interrupt is pending
1: No interrupt pending</td><td>R</td></tr>
</table>

Table 24-4 UART Interrupt Identification Register Description

UIIR.INID	Interrupt Set/Clear Cause			
	Priority	**Type**	**Source**	**Clear Condition**
0b0001	—	None	No pending interrupt	—
0b0110	1st Highest	Receive Line Status	Overrun, Parity, Frame Error, Break Interrupt, and FIFO Error (DMA mode only)	Reading ULSR or empty all the error characters in DMA mode
0b0100	2nd Highest	Receive Data Ready	FIFO mode: Trigger threshold was reached Non-FIFO mode: URBR full	FIFO mode: Reading URBR till below trigger threshold. Non-FIFO mode: Empty URBR

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0b1100	2nd Highest	Receive Timeout	FIFO mode only: URBR not empty but no data read in for a period of time	Reset receive buffer by setting UFCR.RFRT to 1 or Reading URBR
0b0010	3rd Highest	Transmit Data Request	FIFO mode: Empty location in UTHR equal to half or more than half Non-FIFO mode: UTHR empty	FIFO mode: Data number in UTHR more than half Non-FIFO mode: Writing UTHR
0b0000	4th Highest	Modem Status	Modem CTS_ pin status change	Reading UMSR

24.7.2.7 UART FIFO Control Register (UFCR,0x0008)

The write-only register UFCR contains the control bits for receive and transmit FIFO.

	UFCR																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								RDTR		Reserved	UME	DME	TFRT	RFRT	FME
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:6	RDTR	**Receive Buffer Data Number Trigger.** These bits are used to select the trigger level for the receive data ready interrupt in FIFO mode. 0b00: 1 0b01: 16 0b10: 32 0b11: 60	W
5	Reserved	Writing has no effect. Read as zero.	R
4	UME	**UART Module Enable.** 0: Disable UART 1: Enable UART	RW
3	DME	**DMA Mode Enable.** 0: Disable DMA mode 1: Enable DMA mode	W
2	TFRT	**Transmit Holding Register Reset.**	W

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		0: Not reset 1: Reset transmit FIFO	
1	RFRT	**Receive Buffer Reset.** 0: Not reset 1: Reset receive FIFO	W
0	FME	**FIFO Mode Enable.** Set this bit before the trigger levels. 0: non-FIFO mode 1: FIFO mode	W

24.7.2.8 UART Line Control Register (ULCR,0x000C)

The ULCR defines the format for UART data transmission.

	ULCR																															Base + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								DLAB	SBK	STPAR	PARM	PARE	SBLS	WLS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	DLAB	**Divisor Latch Access Bit.** 0: Enable to access URBR, UTHR or UIER 1: Enable to access UDLLR or UDLHR	RW
6	SBK	**Set Break.** Causes a break condition (at least one 0x00 data) to be transmitted to the receiving UART. Acts only on the TXD pin and has no effect on the transmit logic. 0: No effect on TXD output 1: Forces TXD output to 0	RW
5	STPAR	**Sticky Parity.** Setting this bit forces parity location to be opposite of PARM bit when PARE is 1 (it is ignored when PARE is 0). 0: Disable Sticky parity 1: Enable Sticky parity (opposite o f PARM bit)	RW
4	PARM	**Parity Odd/Even Mode Select.** If PARE = 0, PARM is ignored. 0: Odd parity	RW

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		1: Even parity	
3	PARE	**Parity Enable.** Enables a parity bit to be generated on transmission or checked on reception. 0: No parity 1: Parity	RW
2	SBLS	**Stop Bit Length Select.** Specifies the number of stop bits transmitted and received in each character. When receiving, the receiver checks only the first stop bit. 0: 1 stop bit 1: 2 stop bits, except for 5-bit character then 1-1/2 bits	RW
1:0	WLS	**Word Length Select.** 0b00: 5-bit character 0b01: 6-bit character 0b10: 7-bit character 0b11: 8-bit character	RW

24.7.2.9 UART Modem Control Register (UMCR,0x0010)

The UMCR uses the modem control pins RTS_ and CTS_ to control the interface with a modem or data set. UMCR also controls the loopback mode. Loopback mode must be enabled before the UART is enabled..

	UMCR																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								MDCE	FCM	Reserved	LOOP	Reserved		RTS	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	MDCE	**Modem Control Enable.** 0: Modem function is disabled 1: Modem function is enabled	RW
6	FCM	**Flow Control Mode.** 0: Flow control by software 1: Flow control by hardware	RW
5	Reserved	Writing has no effect. Read as zero.	R

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4	LOOP	**Loop Back.** This bit is used for diagnostic testing of the UART. When LOOP is 1, TXD output pin is set to a logic 1 state, RXD is disconnected from the pin, and the output of the transmitter shifter register is looped back into the receiver shift register input internally, similar to CTS_ and RTS_ pins and the RTS bit of the UMCR is connected to CTS bit of UMSR respectively. Loopback mode must be selected before the UART is enabled. 0: Normal operation mode 1: Loopback-mode UART operation	RW
3:2	Reserved	Writing has no effect. Read as zero.	R
1	RTS	**Request To Send.** This bit can control the RTS_ output state. 0: RTS_ force to high 1: RTS_ force to low	RW
0	Reserved	Writing has no effect. Read as zero.	R

24.7.2.10 UART Line Status Register (ULSR,0x0014)

The read-only ULSR indicates status information during the data transfer. Receive error information in ULSR[4:1] remains set until software reads ULSR and it must be read before the error character is read.

	ULSR																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								FIFOE	TEMP	TDRQ	BI	FMER	PARER	OVER	DRY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	FIFOE	**FIFO Error Status. (FIFO mode only)** FIFOE is set when there is at least one kind of receive error (parity, frame, overrun, break) for any of the characters in receive buffer. FIFOE is reset when all error characters are read out of the buffer.	R

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		During DMA transfer, the error interrupt generates when FIFOE is 1, and no receive DMA request generates even when data in receive buffer reaches the trigger threshold until all the error characters are read out. In non-DMA mode, FIFOE set does not generate error interrupt. 0: No error data in receive buffer or non-FIFO mode 1: One or more error character in receive buffer	
6	TEMP	**Transmit Holding Register Empty.** Set when both UTHR and shift register are empty. It is cleared when either the UTHR or the shift register contains a data character. 0: There is data in the transmit shifter and UTHR 1: All the data in the transmit shifter and UTHR has been shifted out	R
5	TDRQ	**Transmit Data Request.** Set when UTHR has half or more empty location (FIFO mode) or empty (non-FIFO mode). When both UIER.TDRIE and TDRQ are 1, transmit data request interrupt generates or during DMA transfer, DMA request to the DMA controller generates when UIER.TDRIE is 0 and TDRQ is 1. 0: There is one (non-FIFO mode) or more than half data (FIFO mode) in UTHR 1: None data (non-FIFO mode) or half or less than half data (FIFO mode) in UTHR	R
4	BI	**Break Interrupt.** BI is set when the received data input is held low for longer than a full-word transmission time (the total time of start bit + data bits + parity bit + stop bits). BI is cleared when the processor reads the ULSR. In FIFO mode, only one character equal to 0x00 is loaded into the FIFO regardless of the length of the break condition. BI shows the break condition for the character at the front of the FIFO, not the most recently received character. 0: No break signal has been received 1: Break signal received	R
3	FMER	**Framing Error.** Set when the bit following the last data bit or parity bit is detected to be 0. If the ULCR had been set for two or one and half stop bits, the other stop bits are not checked except the first one. In FIFO mode, FMER shows a framing error for the character at the front of the receive buffer, not for the most recently received character. Cleared when the processor reads the ULSR. 0: No framing error 1: Invalid stop bit has been detected	R
2	PARER	**Parity Error.**	R

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		Indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. PARER is set upon detection if a parity error and is cleared when the processor reads the ULSR. In FIFO mode, PARER shows a parity error for the character at the front of the FIFO, not the most recently received character. 0: No parity error 1: Parity error has occurred	
1	OVER	**Overrun Error.** Set when both receive buffer and shifter are full and new data is received which will be lost. Cleared when the processor reads the ULSR. 0: No data has been lost 1: Receive data has been lost	R
0	DRY	**Data Ready.** Set when a complete incoming character has been received into the Receive Buffer registers. DRY is cleared when the receive buffer is read (non-FIFO mode) or when the buffer is empty or when the buffer is reset by setting UFCR.RFRT to 1. 0: No data has been received 1: Data is available in URBR	R

24.7.2.11 UART Modem Status Register (UMSR,0x0018)

The read-only UMSR provides the current state of the control lines from the modem to the processor. They are cleared when the processor reads UMSR.

	UMSR																																Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CTS	Reserved			CCTS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4	CTS	**Status of Clear To Send.** When MDCE bit is 1, this bit is the complement of CTS_ input. If Loop bit of UMCR is 1, this bit is equivalent to RTS bit of UMCR. 0: CTS_ pin is 1 1: CTS_ pin is 0	R

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3:1	Reserved	Writing has no effect.Read as zero.	R
0	CCTS	**Change status of CTS_.** When MDCE bit is 1, this bit indicates the state change on CTS_ pin. 0: No state change on CTS_ pin since last read of UMSR 1: A change occurs on the state of CTS_ pin	R

24.7.2.12 UART Scratchpad Register(USPR,0x001C)

This Scratchpad register is used as a scratch register for the programmer and has no effect on the UART.

	USPR																															Base + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								STCH_D							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	STCH_D	Be scratched data	RW

24.7.2.13 Infrared Selection Register (ISR,0x0020)

The ISR is used to configure the slow-infrared (SIR) interface that is provided in each UART to support two-way wireless communication using infrared transmission that conforms to the IrDA serial infrared specification 1.1. The maximum frequency is up to 115.2kbps.

	ISR																															Base + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											RDPL	TDPL	XMODE	RCVEIR	XMITIR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	RDPL	**Receive Data Polarity.** 0: Slow-infrared (SIR) interface decoder takes positive pulses as zeros 1: SIR decoder takes negative pulses as zeros	RW

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3	TDPL	**Transmit Data Polarity.** 0: SIR encoder generates a positive pulse for a data bit of zero 1: SIR encoder generates a negative pulse for a data bit of zero	RW
2	XMODE	**Transmit Pulse Width Mode.** Set when the transmit encoder needs to generate 1.6us pulses (that are 3/16 of a bit-time at 115.2 kbps). Cleared when the transmit encoder needs to generate 3/16 of a bit-time wide according to current baud rate. 0: Transmit pulse width is 3/16 of a bit-time wide 1: Transmit pulse width is 1.6 us	RW
1	RCVEIR	**Receiver SIR Enable.** This bit is used to select the signal from the RXD pin is processed by the IrDA decoder before it is fed to the UART (RCVEIR = 1) or bypass IrDA decoder and is fed directly to the UART (RCVEIR = 0). 0: Receiver is in UART mode 1: Receiver is in SIR mode	RW
0	XMITIR	**Transmitter SIR Enable.** This bit is used to select TXD output pin is processed by the IrDA encoder before it is fed to the device pin (XMITIR = 1) or bypass IrDA encoder and is fed directly to the device pin (XMITIR = 0). **Note:** Disable infrared LED before XMITIR is set, otherwise a false start bit may occur. 0: Transmitter is in UART mode 1: Transmitter is in SIR mode	RW

24.7.2.14 UART M Register (UMR, 0x0024)

It will take UART at least M cycles to transmit or receive one bit.

It will take UART at most M+1 cycles to transmit or receive one bit.

	UMR																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											M				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4:0	M	The value of UMR register.	RW

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24.7.2.15 UART Add Cycle Register (UACR,0x0028)

It controls time that UART need to transmit or receive the nth bit of the data.

	UACR																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				AC											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect. Read as zero.	R
11:0	AC	If the nth bit of the register is： 1: it will take UART M+1 cycles to transmit or receive the bit of data; 0: it will take UART M cycles to transmit or receive the bit of data For except; 12'h0: it will take UART M cycles to transmit or receive one bit of data; 12'hFFF: it will take UART M+1 cycles to transmit or receive one bit of data;	RW

24.7.2.16 UART RXFIFO Counter Register (URCR,0x0040)

Indicates there are n data in RXFIFO.

	URCR																															Base + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									RCNT						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6:0	RCNT	RXFIFO Counter. Indicates there are n data in RXFIFO when this field is n.	R

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24.7.2.17 UART TXFIFO Counter Register (UTCR,0x0044)

Indicates there are n data in TXFIFO

	UTCR																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									TCNT						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect Read as zero.	R
6:0	TCNT	TXFIFO Counter. Indicates there are n data in TXFIFO when this field is n.	R

24.8 Operation Flow

The following sections describe the UART operations that include flow of configuration, data transmission, data reception, and Infrared mode.

24.8.1 UART Configuration

Before UART starts to transfer data or changing transfer format, configuration must be done to define the transfer format. The sample flow is as the following:

In FIFO mode, set FME bit of UFCR to 1, reset receive and transmit FIFO, then initialize the UART as described below:

1. Clear UFCR.UME to 0.
2. Set value in UDLL/UDHR to generate the baud rate clock.
3. Set data format in ULCR.
4. If it is in FIFO MODE, set FME bit and other FIFO control in UFCR, reset receive and transmit FIFO, otherwise skip item 4.
5. Set each interrupt enable bit in UIER in interrupt-based transfer or set UFCR.DME in DMA-based transfer (DMA transfer is FIFO mode only), then set UFCR.UME.

24.8.2 Data Transmission

After configuration, UART is ready for data transfer. For data transmission, refer to the following procedure:

1. Read ULSR.TDRQ (interrupt disable) or wait for transmit data request interrupt (interrupt

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enable), if TDRQ = 1 or transmit data request interrupt generates, that means there is enough empty location in UTHR for new data.

2 If ULSR.TDRQ is 1 or get the transmit data request interrupt, write transmit data to UTHR to start transmission.

3 Do item 1 and item 2 if there are more data waiting for transmit.

4 After all necessary data are written to UTHR, wait ULSR.TEMP = 1, that means all data completely transmitted.

5 If it is necessary to send break, set ULCR.SBK and at least wait for 1-bit interval time to send a valid break, then clear ULCR.SBK.

6 Clear UME bit to finish UART transmission.

24.8.3 Data Reception

After configuration, UART is ready for data transfer. For data reception, refer to the following sample procedure:

1 Read ULSR.DRY (interrupt disable) or wait for receive data request interrupt (interrupt enable), if ULSR.DRY =1 or receive data request interrupt generates, that means URBR has one data (non-FIFO mode) or data in URBR reaches the trigger value. (FIFO mode)

2 If ULSR.DRY = 1 or receive data request interrupt generates, then read ULSR.FIFOE or see if there is error interrupt, if FIFOE = 1, it means received data has receive error, then go to error handler, other wise go to item 3.

3 Read one received data in URBR (non-FIFO mode) or data equal to trigger value in URBR. (FIFO mode)

4 Check whether all data received: check whether ULSR.DRY = 0, in FIFO mode and interrupt is enabled, timeout interrupt may generate, when timeout interrupt generates, read URBR till ULSR.DRY = 0.

5 Clear UFCR.UME to end data reception when all data are received and ULSR.DRY = 0.

24.8.4 Receive Error Handling

A sample error handling flow is as the following:

1 If ULSR.FIFOE = 1, it means there is receive error in received data, then check what error it is.

2 If ULSR.OVER = 1, go to OVER error handling.

3 If ULSR.BI = 1, go to Break handling.

4 If ULSR.FMER = 1, go to Frame error handling.

5 If PARER = 1, go to PARER error handling.

24.8.5 Modem Transfer

When UMCR.MDCE = 1, modem control is enabled. Transfer flow can be stopped and restarted by software through RTS_ and CTS_ pin. When UART transmitter detects low level on CTS_ pin, it stops transmission and TxD pin goes to mark state after finishing transmitting the current character until it

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detects CTS_ pin goes back to high level. RTS_ pin is output to receiving UART and its state can be controlled by setting UMCR.RTS bit, that is, setting UMCR.RTS to 1, RTS_ pin is low level output that means UART is ready to receive data, on the contrary, it means UART currently can't receive more data.

24.8.6 DMA Transfer

UART can operate in DMA-based (UFCR.DME = 1, FIFO mode only), that is, dma request initiated by UART takes the place of interrupt request and transmission/reception is carried out using DMA instead of CPU. Be sure that software guarantee to disable transmit and receive interrupt except timeout and error interrupts.

During DMA transfer, if an interrupt occurs, software must first read the ULSR to see if an error interrupt exists, then check the UIIR for the source of the interrupt and if DMA channel is already halt because of the error indicator from UART, then disable DMA channel and read out all the error data from receive FIFO. Software re-set and re-enable DMA and data transfer by DMA will re-start.

24.8.7 Slow IrDA Asynchronous Interface

Each UART supports slow infra-red (SIR) transmission and reception by setting ISR.XMITIR and ISR.RCVEIR to 1 (make sure the two bits are not set to 1 at the same time because SIR can't operate full-duplex). According to the IrDA 1.1, data rate is limited at a maximum value of 115.2Kbps.

In SIR transmit mode, the transmit pulse comes out at a rate of 3/16 (when the transmit data bit is zero); in SIR receive mode, the receiver must detect the 3/16 pulsed period to recognize a zero value (an active high or low pulse is demodulation to 0, and no pulse is demodulation to 1).

Compared to normal UART, there are some limitations to SIR, that is, each character is fixed to 8-bit data width, no parity and 1 stop bit and modem function is ignored. The IrDA 1.1 specifies a minimum 10ms latency after an optical node ceases transmitting before its receiver recovers its receiving function and software must guarantee this delay.

In the IrDA 1.1 specification, communication must start up at the rate of 9600bps, but then allows the link to negotiate higher (or lower) data rates if supported by both ends. However, the communication rate will not automatically change. Change, if necessary, is performed by software.

24.8.8 For any frequency clock to use the UART

Note: if you don't set M register and UACR the UART work at normal mode with the specified frequencies. To use other frequency you should to set M register and UACR to right value.

1 The Improving

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Following changes are made:

a One bit is composed by M CLK_{BR} cycles, which can be 4~1024.

b Some extra CLK_{BR} cycles can be inserted in some bits in one frame, so that like M has fraction.

For instance:

$CLK_{BR} = CLK_{DEV} / N$ N = 1, 2, …

$CLK_{BR} = CLK_{DEV}$ = 4MHz

Band rate = 460800

In accurate

$M_a = 8.681$

We take

M = 8, with 8 extra cycles in every frame

A 12-bit register is used to indicate where to insert the extra cycles.

The first line is the time expected

The second line is the time actual

The third line is the time error

Time expected	0	2.17	4.34	4.34	6.51	8.68	10.85	13.02	15.19	17.36	19.53	21.70	23.87
Time actual	0	2.25	4.25	4.25	6.5	8.75	10.75	13	15.25	17.25	19.5	21.75	23.75
Time error	0	0.08	0.09	0.09	0.01	0.07	0.10	0.02	0.06	0.11	0.03	0.05	0.12

For transmission, in theory, the biggest error is half of CLK_{BR} cycle, which is 0.125us here.

2 To set UMR register

$CLK_{BR} = CLK_{DEV} / N$

$M_a = CLK_{BR}$/band rate

M is modem of M_a.

Write M to M register.

Considering the power and the robust quality, for M form 6 to 32 is you better select by set the UDLR.

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The max error

$$\frac{0.5/CLK_{BR}}{M_a/CLK_{BR}} = 0.5/M_a < 0.5/M$$

M	4	8	16	32	64
error/W_{bit}	12.5%	6.25%	3.125%	1.56%	0.78%

3 To set UACR value

For each bit of it means:

0: means not to add additional cycle to the bit that UART is prepare to transmit or receive, in another word, you will to use M cycles to transmit or receive the bit

1: means to add additional cycle to the bit that UART is prepare to transmit or receive, in another word, you will to use M+1 cycles to transmit or receive the bit

To set UACR value you must ensure that the max error of each bit should be less than $0.5P_{BR}$.

For example：M_a-M =0.15; M+1-M_a=0.85;

Write 8 to UMR,

Write 0x408 to UACR

cycle/bit	:	M，	M，	M，	M+1，	M，	M，	M，	M，	M，	M，	M+1，	M
UACR	:	0	0	0	1	0	0	0	0	0	0	1	0

24.9 Index

Table 24-5 Description of Proprietary Vocabulary

Name	Description
UART	universal asynchronous receiver/transmitter
SIR	Serial infrared

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25 MMC/SD CE-ATA Controller(MSC)

25.1 Overview

The Multi Media Card (MMC) is a universal low cost mass storage and communication media that is designed to cover a wide area of applications such as electronic toys, organizers, PDAs, smart phones, and so on.

The Secure Digital (SD) card is an evolution of MMC. It is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in newly emerging audio and video consumer electronic devices. The physical form factor, pin assignment, and data transfer protocol are forward compatible with the Multi Media Card with some additions. An SD card can be categorized as SD memory or SD I/O card, commonly known as SDIO. A memory card invokes a copyright protection mechanism that complies with the security of the SDMI standard and is faster and capable of higher memory capacity. The SDIO card provides high-speed data I/O with low-power consumption for mobile electronic devices.

For CE-ATA detail protocol , please referred to WWW.CE-ATA.ORG.

25.2 Features

- Fully compatible with the MMC System Specification version 4.2
- Support SD Specification 3.0
- Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
- Maximum data rate is 50MBps
- Support MMC data width 1bit ,4bit
- Built-in programmable frequency divider for MMC/SD bus
- Built-in Special Descriptor DMA
- Multi-SD function support including multiple I/O and combined I/O and memory
- IRQ supported enable card to interrupt MMC/SD controller
- Single or multi block access to the card including erase operation
- Stream access to the MMC card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
- Supports CE-ATA digital protocol commands
- Support Command Completion Signal and interrupt to CPU
- Command Completion Signal disable feature
- The maximum block length is 4096bytes

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25.3 Block Diagram

Figure 25-1 MMC/SD Controller Block Diagram

25.4 Functional Description

All communication between system and cards is controlled by the MSC. The MSC sends commands of two type: broadcast and addressed (point-to-point) commands.

Broadcast commands are intended for all cards, command like “Go_Idle_State”, “Send_Op_Cond”, “All_Send_CID” and “Set_Relative_Addr” are using way of broadcasting. During Broadcast mode, all cards are in open-drain mode, to avoid bus contention.

After Broadcast commands “Set_Relative_Addr” issue, cards are enter standby mode, and Addressed command will be used from now on, in this mode, CMD/DAT will return to push-pull mode, to have maximum driving for maximum operation frequency.

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The MMC and the SD are similar product. Besides the 4x bandwidth and the built-in encryption, they are being programmed similarly.

The MMC/SD controller (MSC) is the interface between the software and the MMC/SD bus. It is responsible for the timing and protocol between the software and the MMC/SD bus. It consists of control and status registers, a 16-bit response FIFO that is 8 entries deep, and one 32-bit receive/transmit data FIFOs that are 16 entries deep. The registers and FIFOs are accessible by the software.

MSC also enable minimal data latency by buffering data and generating and checking CRCs.

25.4.1 MSC Reset

The MMC/SD controller (MSC) can be reset by a hardware reset or software reset. All registers and FIFO controls are set to their default values after any reset.

25.4.2 Voltage Validation

All cards shall be able to establish communication with the host using any operation voltage in the maximal allowed voltage range specified in this standard. However, the support minimum and maximum values for Vdd are defined in Operation Conditions register (OCR) and many not cover the whole range. Cards that store the CID and CSD data in the payload memory would be able to communicate these information only under data transfer Vdd conditions. That means if host and card have non compatible Vdd ranges, the card will not be able to complete the identification cycle, nor to send CSD data.

Therefore, a special command Send_Op_Cont (CMD1 for MMC), SD_Send_Op_Cont (CMD41 for SD Memory) and IO_Send_Op_Cont (CMD5 for SDIO) are designed to provide a mechanism to identify and reject cards which do not match the Vdd range desired by the host. This is accomplished by the host sending the required Vdd voltage window as the operand of this command. Cards which can not perform data transfer in the specified range must discard themselves from further bus operations and go into Inactive State. By omitting the voltage range in the command, the host can query each card and determine the common voltage range before sending out-of-range cards into the Inactive State. This query should be used if the host is able to select a common voltage range or if a notification to the application of non usable cards in the stack is desired.

25.4.3 Card Registry

Card registry on MMC and SD card are different.

For SD card, Identification process start at clock rate Fod, while CMD line output drives are push-pull drivers instead of open-drain. After the bus is activated the host will request the cards to send their valid operation conditions. The response to ACMD41 is the operation condition register of the card.

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The same command shall be send to all of the new cards in the system. Incompatible cards are sent into Inactive State. The host then issue the command All_Send_CID (CMD2) to each card and get its unique card identification (CID) number. Card that is unidentified, that is, which is in Ready State, send its CID number as the response. After the CID was sent by the card it goes into Identification State. Thereafter, the host issues Send_Relative_Addr (CMD3) asks the card to publish a new relative card address (RCA), which is shorter that CID and which will be used to address the card in the future data transfer mode. Once the RCA is received the card state changes to the Stand-by State. At this point, if the host wants that the card will have another RCA number, it may ask the card to publish a new number by sending another Send_Relative_Addr command to the card. The last published RCA is the actual RCA of the card. The host repeats the identification process, that is, the cycles with CMD2 and CMD3 for each card in the system.

In MMC, the host starts the card identification process in open-drain mode with the identification clock rate Fod. The open drain driver stages on the CMD line allow parallel card operation during card identification. After the bus is active the host will request the cards to send their valid operation conditions (CMD1). The response to CMD1 is the 'wired or' operation on the condition restrictions of all cards in the system. Incompatible cards are sent into Inactive State. The host then issues the broadcast command All_Send_CID (CMD2), asking all cards for their unique card identification (CID) number. All unidentified cards, that is, those which are in Ready State, simultaneously start sending their CID numbers serially, while bit-wise monitoring their outgoing bit-stream. Those cards, whose outgoing CID bits do not match the corresponding bits on the command line in any one of the bit periods stop sending their CID immediately and must wait for the next identification cycle. Since CID is unique for each card, only one card can be successfully send its full CID to the host. This card then goes into Identification State. Thereafter, the host issues Set_Relative_Addr (CMD3) to assign to this card a relative card address (RCA). Once the RCA is received the card state changes to the Stand-by State, and the card does not react to further identification cycles, and its output switches from open-drain to push-pull. The host repeat the process, which is CM2 and CMD3, until the host receive time-out condition to recognize completion of the identification process.

25.4.4 Card Access

25.4.4.1 Block Access, Block Write and Block Read

During block write (CMD24-27) one or more blocks of data are transferred from the host to the card with a CRC appended to the end of each block by the host. A card supporting block write shall always be able to accept a block of data defined by WRITE_BL_LEN. If the CRC fails, the card shall indicate the failure on the DAT line; the transferred data will be discarded and not written, and all further transmitted blocks (in multiple block write mode) will be ignored.

Programming of the CID and CSD registers does not require a previous block length setting. The transferred data is also CRC protected. If a part of the CSD or CID register is stored in ROM, then this unchangeable part must match the corresponding part of the receive buffer. If this match fails, then the card will report an error and not change any register contents. Some cards may require long and

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unpredictable times to write a block of data. After receiving a block of data and completing the CRC check, the card will begin writing and hold the DAT line low if its write buffer is full and unable to accept new data from a new WRITE_BLOCK command. The host may poll the status of the card with a SEND_STATUS command (CMD13) at any time, and the card will respond with its status. The status bit READY_FOR_DATA indicates whether the card can accept new data or whether the write process is still in progress). The host may deselect the card by issuing CMD7 (to select a different card) which will displace the card into the Disconnect State and release the DAT line without interrupting the write operation. When reselecting the card, it will reactivate busy indication by pulling DAT to low if programming is still in progress and the write buffer is unavailable.

Block read is similar to stream read, except the basic unit of data transfer is a block whose maximizes is defined in the CSD (READ_BL_LEN). If READ_BL_PARTIAL is set, smaller blocks whose starting and ending address are entirely contained within one physical block (as defined by READ_BL_LEN) may also be transmitted. Unlike stream read, a CRC is appended to the end of each block ensuring data transfer integrity. CMD17 (READ_SINGLE_BLOCK) initiates a block read and after completing the transfer, the card returns to the Transfer state. CMD18 (READ_MULTIPLE_BLOCK) starts a transfer of several consecutive blocks. Blocks will be continuously transferred until a stop command is issued. If the host uses partial blocks whose accumulated length is not block aligned and block misalignment is not allowed, the card shall detect a block misalignment at the beginning of the first mis-aligned block, set the ADDRESS_ERROR error bit in the status register, abort transmission and wait in the Data State for a stop command.

25.4.4.2 Stream Access, Stream Write and Stream Read (MMC Only)

Stream write (CMD20) starts the data transfer from the host to the card beginning from the starting address until the host issues a stop command. Since the amount of data to be transferred is not determined in advance, CRC can not be used. If the end of the memory range is reached while sending data and no stop command has been sent by the host, all further transferred data is discarded.

There is a stream oriented data transfer controlled by READ_DAT_UNTIL_STOP (CMD11). This command instructs the card to send its payload, starting at a specified address, until the host sends a STOP_TRANSMISSION command (CMD12). The stop command has execution delay due to the serial command transmission. The data transfer stops after the end bit of the stop command. If the end of the memory range is reached while sending data and no stop command has been sent yet by the host, the contents of the further transferred payload is undefined.

25.4.4.3 Erase, Group Erase and Sector Erase (MMC Only)

It is desirable to erase many sectors simultaneously in order to enhance the data throughput. Identification of these sectors is accomplished with the TAG_* commands. Either an arbitrary set of sectors within a single erase group, or an arbitrary selection of erase groups may be erase at one time, but not both together. That is, the unit of measure for determining an erase is either a sector or an

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erase group. If a set of sectors must be erased, all selected sectors must lie within the same erase group. To facilitate selection, a first command with the starting address is followed by a second command with the final address, and all sectors (or groups) within this range will be selected for erase.

25.4.4.4 Wide Bus Selection/Deselection

Wide Bus (4 bit bus width) operation mode may be selected / deselected using ACMD6. The default bus width after power up or GO_IDLE (CMD0) is 1 bit bus width. ACMD6 command is valid in 'trans state' only. That means the bus width may be changed only after a card was selected (CMD7).

25.4.5 Protection Management

Three write protect methods are supported in the host for Cards, Card internal write protect (Card's responsibility), Mechanical write protect switch (Host responsibility only) and Password protection card lock operation.

25.4.5.1 Card Internal Write Protection

Card data may be protected against either erase or write. The entire card may be permanently write protected by the manufacturer or content provider by setting the permanent or temporary write protect bits in the CSD. For cards which support write protection of groups of sectors by setting the WP_GRP_SIZE sectors as specified in the CSD), and the write protection may be changed by the application. The SET_WRITE_PROT command sets the write protection of the addressed write-protect group, and the CLR_WRITE_PROT command clears the write protection of the addressed write-protect group.

The SEND_WRITE_PROT command is similar to a single block read command. The card shall send a data block containing 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits. The address field in the write protect commands is a group address in byte units. The card will ignore all LSB's below the group size.

25.4.5.2 Mechanical write protect switch

A mechanical sliding tablet on the side of the card will be used by the user to indicate that a given card is write protected or not. If the sliding tablet is positioned in such a way that the window is open that means the card is write protected. If the window is close the card is not write protected.

A proper, matched, switch on the socket side will indicated to the host that the card is write protected or not. It is the responsibility of the host to protect the card. The position of the write protect switch is un-known to the internal circuitry of the card.

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25.4.5.3 Password Protect

The password protection feature enables the host to lock a card while providing a password, which later will be used for unlocking the card. The password and its size is kept in an 128-bit PWD and 8-bit PWD_LEN registers, respectively. These registers are non-volatile so that a power cycle will not erase them.

Locked cards respond to (and execute) all commands in the basic command class (class 0) and “lock card” command class. Thus the host is allowed to reset, initialize, select, query for status, etc., but not to access data on the card. If the password was previously set (the value of PWD_LEN is not 0) will be locked automatically after power on. Similar to the existing CSD and CID register write commands the lock/unlock command is available in “trans-state” only. This means that it does not include an address argument and the card must be selected before using it. The card lock/unlock command has the structure and bus transaction type of a regular single block write command. The transferred data block includes all the required information of the command (password setting mode, PWD itself, card lock/unlock etc.). The following table describes the structure of the command data block.

Table 25-1 Command Data Block Structure

Byte #	Bit 7-4	Bit 3	Bit 2	Bit 1	Bit 0
0	Reserved	ERASE	LOCK_UNLOCK	CLR_PWD	SET_PWD
1	PWDS_LEN				
2	Password Data				
…					
PWDS_LEN + 1					

ERASE – 1 Defines Forced Erase Operation (all other bits shall be 0) and only the command byte is sent.

LOCK/UNLOCK – 1=Locks the card. 0=Unlock the card (note that it is valid to set this bit together with SET_PWD but it is not allowed to set it together with CLR_PWD).

CLR_PWD – 1=Clears PWD.

SET_PWD – 1=Set new password to PWD.

PWD_LEN – Defines the following password length (in bytes).

PWD – The password (new or currently used depending on the command).

The data block size shall be defined by the host before it send the card lock/unlock command. This will allow different password sizes.

The following paragraphs define the various lock/unlock command sequences:

Lock command sequences:

1 Setting the Password.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16), given by the 8bit card lock/unlock mode, the 8 bits password size (in bytes), and the number of bytes of the new password. In case that

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a password replacement is done, then the block size shall consider that both passwords, the old and the new one, are sent with the command.

c Send Card Lock/Unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode (SET_PWD), the length (PWD_LEN) and the password itself. In case that a password replacement is done, then the length value (PWD_LEN) shall include both passwords, the old and the new one, and the PWD field shall include the old password (currently used) followed by the new password.

d In case that the sent old password is not correct (not equal in size and content) then LOCK_UNLOCK_FAILED error bit will be set in the status register and the old password does not change. In case that PWD matches the sent old password then the given new password and its size will be saved in the PWD and PWD_LEN fields, respectively.

NOTE:

the password length register (PWD_LEN) indicates if a password is currently set. When it equals 0 there is no password set. If the value of PWD_LEN is not equal to zero the card will lock itself after power up. It is possible to lock the card immediately in the current power session by setting the LOCK/UNLOCK bit (while setting the password) or sending additional command for card lock.

2 Reset the password.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.

c Send the card lock/unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode CLR_PWD, the length (PWD_LEN) and the password (PWD) itself (LOCK/UNLOCK bit is don't care). If the PWD and PWD_LEN is set to 0. If the password is not correct then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

3 Locking a card.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of currently used password.

c Send the card lock/unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode LOCK, the length (PWD_LEN) and the password (PWD) itself.

If the PWD content equals to the sent password then the card will be locked and the card-locked status bit will be set in the status register. If the password is not correct then LOCK_UNLOCK_FAILED error bit will be set in the status register.

NOTE:

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it is possible to set the password and to lock the card in the same sequence. In such case the host shall perform all the required steps for setting the password (as described above) including the bit LOCK set while the new password command is sent. If the password was previously set (PWD_LEN is not 0), then the card will be locked automatically after power on reset. An attempt to lock a locked card or to lock a card that does not have a password will fail and the LOCK_UNLOCK_FAILED error bit will be set in the status register.

Unlock command sequences:

1 Unlocking the card.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.

c Send the card lock/unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode UNLOCK, the length (PWD_LEN) and the password (PWD) itself.

If the PWD content equals to the sent password then the card will be unlocked and the card-locked status bit will be cleared in the status register. If the password is not correct then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

NOTE:

the unlocking is done only for the current power session. As long as the PWD is not cleared the card will be locked automatically on the next power up. The only way to unlock the card is by clearing the password. An attempt to unlock an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register.

2 Forcing Erase.

In case that the user forgot the password (the PWD content) it is possible to erase all the card data content along with the PWD content. This operation is called Forced Erase.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16) to 1 byte (8bit card lock/unlock command). Send the card lock/unlock command with the appropriate data block of one byte on the data line including 16-bit CRC. The data block shall indicate the mode ERASE (the ERASE bit shall be the only bit set).

If the ERASE bit is not the only bit in the data field then the LCOK_UNLOCK_FAILED error bit will be set in the status register and the erase request is rejected. If the command was accepted then ALL THE CARD CONTENT WILL BE ERASED including the PWD and PWD_LEN register content and the locked card will get unlocked.

An attempt to force erase on an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register.

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25.4.6 Card Status

The response format R1 contains a 32-bit field named card status. This field is intended to transmit the card's status information (which may be stored in a local status register) to the host. If not specified otherwise, the status entries are always related to the previous issued command.

Table below defines the different entries of the status. The type and clear condition fields in the table are abbreviate as follows:

Type:

- E: Error bit.
- S: Status bit..
- R: Detected and set for the actual command response.
- X: Detected and set during command execution. The host must poll the card by issuing the status command in order to read these bits.

Clear Condition:

- A: According to the card current state.
- B: Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).
- C: Clear by read.

Table 25-2 Card Status Description

Bits	Identifier	Type	Description	Clear Condition
31	OUT_OF_RAGE	E R	The command's argument was out of the allowed range for this card. 0: No Error 1: Error	C
30	ADDRESS_ERROR	E R X	A misaligned address which did not match the block length was used in the command. 0: No Error 1: Error	C
29	BLOCK_LEN_ERROR	E R	The transferred block length is not allowed for this, or the number of transferred bytes does not match the block length. 0: No Error 1: Error	C
28	ERASE_SEQ_ERROR	E R	An error in the sequence of erase commands occurred. 0: No Error 1: Error	C
27	ERASE_PARAM	E X	An invalid selection of sectors or	C

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			groups for erase occurred. 0: No Error 1: Error	
26	WP_VIOLATION	E R X	Attempt to program a write protected block. 0: No Protected 1: Protected	C
25	CARD_IS_LOCKED	S X	When set, signals that the card is locked by the host. 0: Card unlocked 1: Card locked	A
24	LOCK_UNLOCK_FAILED	E R X	Set when a sequence or password error has been detected in lock/unlock card command or if there was an attempt to access a locked card. 0: No Error 1: Error	C
23	COM_CRC_ERROR	E R	The CRC check of the previous command failed. 0: No Error 1: Error	B
22	ILLEGAL_COMMAND	E R	Command not legal for the card state. 0: No Error 1: Error	B
21	CARD_ECC_FAILED	E X	Card internal ECC was applied but failed to correct the data. 0: normal 1: failure	C
20	CC_ERROR	E R X	Internal card controller error. 0: No Error 1: Error	C
19	ERROR	E R X	A general or an unknown error occurred during the operation. 0: No Error 1: Error	C
18	UNDERRUN	E X	The card could not sustain data transfer in stream read mode. 0: No Error 1: Error	C
17	OVERRUN	E X	The card could not sustain data programming in stream write mode.	C

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			0: No Error 1: Error	
16	CID/CSD_OVERWRITE	E R X	Can be either one of the following errors. 0: No Error 1: Error	C
15	WP_ERASE_SKIP	S X	Only partial address space was erased due to existing write protected blocks. 0: No Protected 1 : Protected	C
14	CARD_ECC_DISABLED	S X	The command has been executed without using the internal ECC. 0: enabled 1: disabled	A
13	ERASE_RESET	S R	An erase sequence was cleared before executing because an out of erase sequence command was received. 0: normal 1: set	C
12:9	CURRENT_STATE	S X	The state of the card when receiving the command. If the command execution causes a state change, it will be visible to the host in the response to the next command. The four bits are interpreted as binary coded number between 0 and 15. 0: idle 1: ready 2: identify 3: standby 4: transition 5: data 6: receive 7: program 8 : disable (9 – 15) : received	B
8	READY_FOR_DATA	S X	Corresponds to buffer empty signaling on the bus. 0: No Ready 1: Ready	A
7:6	Reserved	-	-	-

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5	APP_CMD	S R	The card will expect ACMD, or indication that the command has been interpreted as ACMD. 0: Disable 1: Enable	C
4:0	Reserved	-	-	-

25.4.7 SD Status

The SD status contains status bits that are related to the SD card proprietary features and may be used for future application specific usage. The size of the SD status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with 16-bit CRC. The SD status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in tran_state (card is selected). SD status structure is described in below.

The same abbreviation for *type* and *clear condition* were used as for the Card Status above.

Table 25-3 SD Status Structure

Bits	Identifier	Type	Description	Clear Condition
511:510	DAT_BUS_WIDTH	S R	Shows the currently defined data bus width that was defined by SET_BUS_WIDTH command. 00: 1 (default) 01: Reserved 10: 4 bit width 11: Reserved	A
509	SECURED_MODE	S R	Card is in Secured Mode of operation. 0: Not in the Mode 10: In the mode	A
508:496	Reserved.			
495:480	SD_CARD_TYPE	S R	All 0, is SD Memory cards.	A
479:448	SIZE_OF_PROTECTED_AREA	S R	Size of protected area.	A
447:312	Reserved.			
311:0	Reserved for manufacturer.			

25.4.8 SDIO

I/O access differs from memory in that the registers can be written and read individually and directly without a FAT file structure or the concept of blocks (although block access is supported). These registers allow access to the IO data, control of the IO function, and report on status or transfer I/O

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data to and from the host.

Each SDIO card may have from 1 to 7 functions plus one memory function built into it. A function is a self contained I/O device. I/O functions may be identical or completely different from each other. All I/O functions are organized as a collection of registers, and there is a maximum of 131,072 registers possible for each I/O function.

25.4.8.1 SDIO Interrupts

In order to allow the SDIO card to interrupt the host, and interrupt function is added to a pin on the SD interface. Pin number 8 which is used as DAT[1] when operating in the 4 bit SD mode is used to signal the card's interrupt to the host. The use of interrupt is optional for each card or function within a card. The SDIO interrupt is "level sensitive", that is, the interrupt line must be held active (low) until it is either recognized and acted upon by the host or de-asserted due to the end of the Interrupt Period. Once the host has serviced the interrupt, it is cleared via an IO write to the appropriate bit in the CCCR. The interrupt output of all SDIO cards is active low.

As Pin 8 of the card is shared between the IRQ and DAT[1] use in the 4 bit SD mode, and interrupt shall only be sent by the card and recognized by the host during a specific time. The time that a low on Pin 8 will be recognized as an interrupt is defined as the Interrupt Period.
The host here will only sample the level of Pin 8 (DAT[1]/IRQ) into the interrupt detector during the Interrupt Period. At all other times, the host will ignore the level on Pin 8. Note that the Interrupt Period is applicable for both memory and IO operations. The definition of the Interrupt Period is different for operations with single block and multiple block data transfer.

25.4.8.2 SDIO Suspend/Resume

Within a multi-function SDIO or a Combo (Mix IO and Memory) card, there are multiple devices (I/O and memory) that must share access to the SD bus. In order to allow the sharing of access to the host among multiple devices, SDIO and combo cards can implement the optional concept of suspend/resume. In a card supports suspend/resume, the host may temporarily halt a data transfer operation to one function or memory (suspend) in order to free the bus for a higher priority transfer to a different function of memory. Once this higher-priority transfer is complete, the original transfer is re-started where it left off (resume). The host controller here is supported by all IO functions except zero, and the memory of a combo card, and can suspend multiple transactions and resume them in any order desired. IO function zero does not support suspend/resume.

The procedure used to perform the Suspend/Resume operation on the SD bus is:

- The host determines which function currently used the DAT[] line(s).
- The host requests the lower priority or slower transaction to suspend.
- The host checks for the transaction suspension to complete.
- The host begins the higher priority transaction.
- The host waits for the completion of the higher priority transaction.

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– The host restores the suspended transaction.

25.4.8.3 SDIO Read Wait

The optional Read Wait (RW) operation is defined only for the SD 1-bit and 4-bit modes. The read wait operation allows a host to signal a card that it is doing a read multiple (CMD53) operation to temporarily stall the data transfer while allowing the host to send commands to any function within the SDIO device. To determine if a card supports the Read Wait protocol, the host must test capability bits in CCCR. The timing for Read Wait is base on the Interrupt Period.

25.4.9 Clock Control

The software should guarantee that the card identification process starts in open-drain mode with the clock rate fod (0 ~ 400khz). In addition, the software should also make the card into interrupt mode with fod (only for MMC). The commands that require fod are CMD0, CMD1, CMD2, CMD3, CMD5, CMD40 and ACMD41. In data transfer mode, the MSC controller can operate card with clock rate fpp (0 ~ 25Mhz).

25.4.10 Application Specified Command Handling

The MMC/SD system is designed to provide a standard interface for a variety applications types. In this environment it is anticipate that there will be a need for specific customers/applications features. To enable a common way of implementing these features, two types of generic commands are defined in the standard: Application Specific Command, ACMD, and General Command, GEN_CMD.

GEN_CMD, this command, when received by the card, will cause the card to interpret the following command as an application specific command, ACMD. The ACMD has the same structure as of regular MMC standard commands and it may have the same CMD number. The card will recognize it as ACMD by the fact that it appears after APP_CMD.

The only effect of the APP_CMD is that if the command index of the, immediately, following command has an ACMD overloading, the none standard version will used. If, as an example, a card has a definition for ACMD13 but not for ACMD7 then, if received immediately after APP_CMD command, Command 13 will be interpreted as the non standard ACMD13 but, command 7 as the standard CMD7.

In order to use one of the manufacturer specific ACMD's the host will:

1 Send APP_CMD. The response will have the APP_CMD bit (new status bit) set signaling to the host that ACMD is now expected.
2 Send the required ACMD. The response will have the APP_CMD bit set, indicating that the accepted command was interpreted as ACMD. If a non-ACMD is sent then it will be respected by the card as normal MMC command and the APP_CMD bit in the Card Status stays clear.

If a non valid command is sent (neither ACMD nor CMD) then it will be handled as a standard MMC

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illegal command error.

The bus transaction of the GEN_CMD is the same as the single block read or write commands (CMD24 or CMD17). The difference is that the argument denotes the direction of the data transfer (rather than the address) and the data block is not a memory payload data but has a vendor specific format and meaning.

The card shall be selected before sending CMD56. The data block size is the BLOCK_LEN that was defined with CMD16. The response to CMD56 will be R1b (card status + busy indication).

25.5 Pins Description

- MSC_CLK, output, host to card clock signal.
- MSC_CMD, inout, bidirectional command/response signal.
- MSC_DAT[3:0], inout, bidirectional data bus.

25.6 Data Format Description

MSC0 and MSC1 supports two kinds of data bits width:1bits, 4bits.

8bits mode is not used.

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Figure 25-2 msc data format

25.7 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R- Read only

   W- Write only

   RW- Read and Write

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RCW- Read and Write, but Clear to 0 by Read
RSW- Read and Write, but Set to 1 by Read
RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
RC- Read only, and Clear to 0 by read
RS- Read only, and Set to 1 by read

3. Reset Value
1 - reset to 1
0 - reset to 0
? - value unknown after reset

25.7.1 Register Memory Map

Table 25-4 Registers Memory Map Base Address

Name	Base	Description
MSC0	0x13450000	Address base of MSC0
MSC1	0x13460000	Address base of MSC1

The MMC-SD-CE_ATA controller is controlled by a set of registers that the application configures before every operation. The following table lists all the MSC registers.

Table 25-5 MSC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
MSC_CTRL	RW	0x0000_0000	0x0000	32
MSC_STAT	R	0x??00_0040	0x0004	32
MSC_CLKRT	RW	0x0000_0000	0x0008	32
MSC_CMDAT	RW	0x0000_5000	0x000C	32
MSC_RESTO	RW	0x0000_0100	0x0010	32
MSC_RDTO	RW	0x00FF_FFFF	0x0014	32
MSC_BLKLEN	RW	0x0000_0000	0x0018	32
MSC_NOB	RW	0x0000_0000	0x001C	32
MSC_SNOB	R	0x0000_????	0x0020	32
MSC_IMASK	RW	0xFFFF_FFFF	0x0024	32
MSC_IFLG	RW	0x??00_2000	0x0028	32
MSC_CMD	RW	0x0000_0000	0x002C	32
MSC_ARG	RW	0x0000_0000	0x0030	32
MSC_RES	R	0x0000_????	0x0034	32
MSC_RXFIFO	R	0x????_????	0x0038	32
MSC_TXFIFO	W	0x????_????	0x003C	32
MSC_LPM	RW	0x0000_0000	0x0040	32
MSC_DMAC	RW	0x0000_0000	0x0044	32
MSC_DMANDA	RW	0x0000_0000	0x0048	32
MSC_DMADA	R	0x0000_0000	0x004C	32

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MSC_DMALEN	R	0x0000_0000	0x0050	32
MSC_DMACMD	R	0x0000_0000	0x0054	32
MSC_CTRL2	RW	0x0080_0000	0x0058	32
MSC_RTCNT	R	0x0000_0000	0x005C	32

25.7.2 Register and Fields Description

25.7.2.1 MSC Control Register (MSC_CTRL,0x0000)

	MSC_CTRL																																		
																																			Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SEND_CCSD	SEND_AD_CCSD	Reserved						EXIT_MULTIPLE	EXIT_TRANSFER	START_READ WAIT	STOP_READ WAIT	RESET	START_OP	CLOCK_CTRL				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. read as zero.	R
15	SEND_CCSD	0: clear bit 1: Send Command Completion Signal Disable (CCSD) to CE_ATA device when set, host sends CCSD to CE_ATA device. Software set the bit only if current command is expecting CCS and interrupts are enabled in CE_ATA devices. Once the CCSD pattern is sent to device, host automatically clears the SEND_CCSD bit.	W
14	SEND_AS_CCSD	0: clear bit 1: send internally generated stop after sending CCSD to CE_ATA device When set, host automatically sends internally-generated STOP command(CMD12) to CE_ATA device. After sending CMD12, MSC_STAT. AUTO_CMD12_DONE is set and generates interrupt to CPU. After sending the CCSD, controller automatically clears the SEND_AS_CCSD bit.	W
13:8	Reserved	Writing has no effect. read as zero.	R
7	EXIT_MULTIPLE	If CMD12 or CMD52 (I/O abort) is to be sent to terminate multiple block read/write in advance, set this bit to 1. 0: No effect 1: Exit from multiple block read/write	W
6	EXIT_TRANSFER	**Only used for SDIO suspend/resume and MMC stream read.**	W

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		For SDIO, after suspend is accepted, set this bit with 1. For MMC, after the data of the expected number are received, set this bit with 1. 0: No effect 1: Exit from multiple block read/write after suspend is accepted, or exit from stream read	
5	START_READ WAIT	Only used for SDIO Read Wait. Start the Read Wait cycle. 0: No effect 1: Start Read Wait	W
4	STOP_READ WAIT	Only used for SDIO Read Wait. Stop the Read Wait cycle. 0: No effect 1: Start Read Wait	W
3	RESET	Reset the MSC controller. 0: No effect 1: Reset the MSC controller	W
2	START_OP	This bit is used to start the new operation. When starting the clock, this bit can be 1. When stopping the clock, this bit can only be 0. 0: Do nothing 1: Start the new operation	W
1:0	CLOCK_CTRL	These bits are used to start or stop clock. 00: Do nothing 01: Stop MMC/SD clock 10: Start MMC/SD clock 11: Reserved	W

25.7.2.2 MSC Status Register (MSC_STAT,0x0004)

	MSC_STAT																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUTO_CMD12_DONE	Reserved		PIN_LEVEL					Reserved			BCE	BDE	BAE	BAR	DMAEND	IS_RESETTING	SDIO_INT_ACTIVE	PRG_DONE	DATA_TRAN_DONE	END_CMD_RES	DATA_FIFO_AFULL	IS_READ WAIT	CLK_EN	DATA_FIFO_FULL	DATA_FIFO_EMPTY	CRC_RES_ERR	CRC_READ_ERROR	CRC_WRITE_ERRO	R		TIME_OUT_RES	TIME_OUTREAD
RST	0	0	0	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31	AUTO_CMD12_DONE	Indicates that the stop command (CMD12) that is internally generated by controller has finished.	R
30:29	Reserved	Writing has no effect, read as zero.	R
28:24	PIN_LEVEL	MSC Interface Pin Level	R

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		PIN_LEV[4:0] indicates the pin level of MSC_CMD, MSC_DAT[3:0] separately.	
23:21	Reserved	Writing has no effect, read as zero.	R
20	BCE	Boot CRC error. 0: No boot CRC error occurs. 1: Boot CRC is not correct.	R
19	BDE	Boot data end. 0: No boot data or boot data is not finished. 1: Boot data is received completely.	R
18	BAE	Boot acknowledge is error. 0: No boot acknowledge is received or boot acknowledge is correct (decided by BAR) 1: The received boot acknowledge is not correct.	R
17	BAR	Boot acknowledge received. 0: No boot acknowledge received. 1: Boot acknowledge received.	R
16	DMAEND	Indicates that the DMA has finished the current transfer.	R
15	IS_RESETTING	MSC is resetting after power up or MSC_CTRL[RESET] is written with 1. 0: Reset has been finished 1: Reset has not been finished	R
14	SDIO_INT_ACTIVE	Indicates whether an interrupt is detected at the SD I/O card. A separate acknowledge command to the card is required to clear this interrupt. 0: No interrupt detected 1: The interrupt from SDIO is detected	R
13	PRG_DONE	Indicates whether card has finished programming. 0: not finished 1: finished	R
12	DATA_TRAN_DONE	Indicates whether data transmission to card has completed. 0: not completed 1: completed	R
11	END_CMD_RES	Indicates whether command and response/no-response sequence have been completed 0: not completed 1: completed	R
10	DATA_FIFO_AFULL	Indicates whether the data FIFO is almost full. 0: The number of words in FIFO is less then 127. 1: The number of words in FIFO is equal to or great then 127	R
9	IS_READ WAIT	Indicates whether SDIO card has entered Read Wait	R

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		State. 0: Card has not entered Read Wait 1: Card has entered Read Wait	
8	CLK_EN	Clock enabled. 0: Clock is off 1: Clock is on	R
7	DATA_FIFO_FULL	Indicates whether the data FIFO is full. 0: Data FIFO is not full 1: Data FIFO is full	R
6	DATA_FIFO_EMPTY	Indicates whether data FIFO is empty. 0: Data FIFO is not empty 1: Data FIFO is empty	R
5	CRC_RES_ERR	Response CRC error. 0: No error on the response CRC 1: CRC error occurred on the response	R
4	CRC_READ_ERROR	Read CRC error. 0: No error on received data 1: CRC error occurred on received data	R
3:2	CRC_WRITE_ERROR	Write CRC error. 00: No error on transmission of data 01: Card observed erroneous transmission of data 10: No CRC status is sent back 11: Reserved	R
1	TIME_OUT_RES	Response Time Out. 0: Card response has not timed out 1: Card response has time out	R
0	TIME_OUT_READ	Read time out. 0: Card read data has not timed out 1: Card read data has timed out	R

25.7.2.3 MSC Clock Rate Register (MSC_CLKRT,0x0008)

The MSC_CLKRT register specifies the frequency division of the MMC/SD bus clock. The software is responsible for setting this register.

	MSC_CLKRT																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													CLK_RATE		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2:0	CLK_RATE	Clock rate. 000: DEV_CLK 001: 1/2 of DEV_CLK 010: 1/4 of DEV_CLK 011: 1/8 of DEV_CLK 100: 1/16 of DEV_CLK 101: 1/32 of DEV_CLK 110: 1/64 of DEV_CLK 111: 1/128 of DEV_CLK This field must be set to 0 when the controller works during normal writing or reading.	RW

25.7.2.4 MSC Command and Data Control Register (MSC_CMDAT,0x000C)

	MSC_CMDAT																															Base + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCS_EXPECTED	READ_CEATA	Reserved		DIS_BOOT	Reserved_0	EXP_BOOT_ACK	BOOT_MODE	Reserved					Reserved_0	SDIO_PDRT	AUTO_CMD12	RTRG		TTRG		IO_ABORT	BUS_WIDTH		Reserved	INIT	BUSY	STREAM_BLOCK	WRITE_READ	DATA_EN	RESPONSE_FORMAT		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CCS_EXPECTED	0: interrupts are not enabled in CE-ATA device, or commands does not expect CCS from device 1: interrupts are enabled in CE_ATA device, or RW_BLK command expects command completion signal from device If the command expects Command Completion Signal (CCS) from the device, the software should set the control bit. It is auto cleared 0 by hardware.	RW
30	READ_CEATA	0: host is not performing read access (RW_BLK or RW_REG) towards CE_ATA device 1: host id performing read access (RW_BLK or RW_REG) towards CE_ATA device Software should set the bit to indicate that CE_ATA device is being accessed for read transfer. The bit is used to	RW

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		disable read data timeout indication while performing CE_ATA read transfers. It is auto cleared 0 by hardware.	
29:28	Reserved	Writing has no effect, read as zero.	R
27	DIS_BOOT	0: Do nothing 1: Stop boot operation DIS_BOOT should not be used with ENA_BOOT at the same time.	RW
26	Reserved_0	Inner usage, keep to 0.	RW
25	EXP_BOOT_ACK	Whether boot acknowledge pattern is expected or not 0: Boot acknowledge pattern is not expected 1: Boot acknowledge pattern is expected	RW
24	BOOT_MODE	Boot mode operation selection. 0: Ignore. 1: Alternative boot operation	RW
23:19	Reserved	Writing has no effect, read as zero.	R
18	Reserved_0	Inner usage, keep to 0.	RW
17	SDIO_PRDT	Determine whether SDIO interrupt is 2 cycle or extend more cycle when data block last is transferred. 0: more cycle (like single block) 1: exact 2 cycle	RW
16	AUTO_CMD12	This field controls use of auto command functions. 0: Auto CMD12 is disabled 1: MSC controller will issue CMD12 automatically after the last data block transfer is finished. when stop command has finished, it is auto cleared 0 by hardware.	RW
15:14	RTRG	Receive FIFO Trigger Value Select. These bits set the receive FIFO half-empty threshold value, when the number of transmit FIFO >= threshold value , RXFIFO_RD_REQ will be set to 1. 00: more than or equal to 16 01: more than or equal to 32 10: more than or equal to 64 11: more than or equal to 96	RW
13:12	TTRG	Transmit FIFO Trigger Value Select. These bits set the transmit FIFO half-empty threshold value, when the number of transmit FIFO < threshold value , TXFIFO_WR_REQ will be set to 1. 00: less than 16 01: less than 32 10: less than 64 11: less than 96	RW

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11	IO_ABORT	Specifies the current command is used to abort data transfer. 0: Nothing 1: The current command is used to abort transfer It is auto cleared 0 by hardware.	WR
10:9	BUS_WIDTH	Specifies the width of the data bus. 00: 1-bit 01: Reserved 10: 4-bit 11: 8bit	WR
8	Reserved	Writing has no effect, read as zero.	R
7	INIT	80 initialization clocks. 0: Issues command directly 1: Issues 80 clocks before command	W
6	BUSY	Specifies whether a busy signal is expected after the current command. This bit is for no data command/response transactions only. 0: Not expect a busy signal 1: Expects a busy signal. If the response is R1b, then set it	WR
5	STREAM_BLOCK	Stream mode. 0: Data transfer of the current command sequence is not in stream mode 1: Data transfer of the current command sequence is in stream mode	WR
4	WRITE_READ	Data Transfer Direction Selection. 0: Read (from card to host) 1: Write (from host to card)	RW
3	DATA_EN	Specifies whether the current command includes data transfer or not. It is also used to reset RX_FIFO and TX_FIFO. 0: Current command without data transfer 1: Current command with data transfer	RW
2:0	RESPONSE_FORMAT	Response Type Selection. 000: No response 001: Format R1 and R1b 010: Format R2 011: Format R3 100: Format R4 101: Format R5 110: Format R6 111: Format R7	RW

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25.7.2.5 MSC Response Time Out Register (MSC_RESTO,0x0010)

	MSC_RESTO																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RES_TO															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Write has no effect, read as zero.	R
15:0	RES_TO	Specifies the maximum number of MSC_CLK clock cycles between the end bit of the command and the response from the SD card. The default value is 128.	RW

25.7.2.6 MSC Read Time Out Register (MSC_RDTO,0x0014)

	MSC_RDTO																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ_TO																															
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:0	READ_TO	Specifies the maximum number of clocks between the command and when the MMC/SD host controller turns on the time-out error for the received data. The unit is MSC_CLK.	RW

25.7.2.7 MSC Block Size Register (MSC_BLKLEN,0x0018)

	MSC_BLKLEN																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BLK_LEN															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:16	Reserved	Write has no effect, read as zero.	R
15:0	BLK_LEN	Specifies the number of bytes in a block, and is normally set to 0x200 for MMC/SD data transactions. The value Specified in the cards CSD.	RW

25.7.2.8 MSC Block Count Register (MSC_NOB,0x001C)

	MSC_NOB																															Base + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																NOB															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Write has no effect, read as zero.	R
15:0	NOB	Specifies the number of blocks in a data transfer. One block is a possibility.	RW

25.7.2.9 MSC Successfully-transferred Blocks Count Register (MSC_SNOB,0x0020)

In block mode, the MSC_SNOB register records the number of successfully transferred blocks. If the last block has CRC error, this register also summaries it. It is used to query blocks for multiple block transfer.

	MSC_SNOB																															Base + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																MSC_SNOB															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	Reserved	Write has no effect, read as zero.	R
15:0	MSC_SNOB	Specify the number of successfully transferred blocks for a multiple block transfer.	R

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25.7.2.10 MSC Interrupt Mask Register (MSC_IMASK,0x0024)

	MSC_IMASK																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_DATA_DONE	Reserved_1		PIN_LEVEL					WR_ALL_DONE	Reserved		BCE	BDE	BAE	BAR	DMAEND	AUTO_CMD12_DONE	DATA_FIFO_FULL	DATA_FIFO_EMP	CRC_RES_ERR	CRC_READ_ERR	CRC_WRITE_ERR	TIME_OUT_RES	TIME_OUT_READ	SDIO	TXFIFO_WR_REQ	RXFIFO_RD_REQ	Reserved		END_CMD_RES	PRG_DONE	DATA_TRAN_DONE
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31	DMA_DATA_DONE	Mask the interrupt DMA_DATA_DONE 0: Not masked 1: Masked	RW
30:29	Reserved_1	Inner usage, keep to 1.	RW
28:24	PIN_LEVEL	Mask the interrupt of PIN_LEVEL separately 0: Not masked 1: Masked	RW
23	WR_ALL_DONE	Mask the interrupt WR_ALL_DONE 0: Not masked 1: Masked	RW
22:21	Reserved	Writing has no effect, read as zero.	R
20	BCE	Boot CRC error. 0: Not masked 1: Masked	RW
19	BDE	Boot data end. 0: Not masked 1: Masked	RW
18	BAE	Mask the interrupt of BAE. 0: Not masked. 1: Masked.	RW
17	BAR	Mask the interrupt of BAR. 0: Not masked. 1: Masked.	RW
16	DMAEND	Mask the interrupt of DMA end. 0: Not masked. 1: Masked.	RW
15	AUTO_CMD12_DONE	Mask the interrupt AUTO_CMD12_DONE. 0: Not masked	RW

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		1: Masked	
14	DATA_FIFO_FULL	0: Not masked 1: Masked	RW
13	DATA_FIFO_EMP	0: Not masked 1: Masked	RW
12	CRC_RES_ERR	0: Not masked 1: Masked	RW
11	CRC_READ_ERR	0: Not masked 1: Masked	RW
10	CRC_WRITE_ERR	0: Not masked 1: Masked	RW
9	TIME_OUT_RES	0: Not masked 1: Masked	RW
8	TIME_OUT_READ	0: Not masked 1: Masked	RW
7	SDIO	Mask the interrupt from the SD I/O card. 0: Not masked 1: Masked	WR
6	TXFIFO_WR_REQ	Mask the Transmit FIFO write request interrupt. 0: Not masked 1: Masked	WR
5	RXFIFO_RD_REQ	Mask the Receive FIFO read request interrupt. 0: Not masked 1: Masked	WR
4:3	Reserved	Writing has no effect, read as zero.	R
2	END_CMD_RES	Mask the End command response interrupt. 0: Not masked 1: Masked	WR
1	PRG_DONE	Mask the Programming done interrupt. 0: Not masked 1: Masked	WR
0	DATA_TRAN_DONE	Mask the Data transfer done interrupt. 0: Not masked 1: Masked	WR

25.7.2.11 MSC Interrupt Flag Register (MSC_IFLG,0x0028)

The MSC_IFLG register shows the currently requested interrupt. The FIFO request interrupts, TXFIFO_WR_REQ, and RXFIFO_RD_REQ are masked off with the DMA function is used. The software is responsible for monitoring these bit in program I/O mode.

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	MSC_IFLG																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_DATA_DONE	Reserved_0		PIN_LEVEL					WR_ALL_DONE	Reserved_0		BCE	BDE	BAE	BAR	DMAEND	AUTO_CMD12_DONE	DATA_FIFO_FULL	DATA_FIFO_EMP	CRC_RES_ERR	CRC_READ_ERR	CRC_WRITE_ERR	TIME_OUT_RES	TIME_OUT_READ	SDIO	TXFIFO_WR_REQ	RXFIFO_RD_REQ	Reserved		END_CMD_RES	PRG_DONE	DATA_TRAN_DONE
RST	0	0	0	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	DMA_DATA_DONE	This field will be set to 1 when DATA_TRAN_DONE and DMAEND are valid. 0: the interrupt is not detected 1: the interrupt is detected	RW
30:29	Reserved_0	Inner usage, keep to 0.	RW
28:24	PIN_LEVEL	Indicates PIN_LEVEL interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
23	WR_ALL_DONE	This field will be set to 1 when DATA_TRAN_DONE, DMAEND and PRG_DONE are valid. 0: the interrupt is not detected 1: the interrupt is detected	RW
22:21	Reserved_0	Inner usage, keep to 0	R
20	BCE	Boot CRC error. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
19	BDE	Boot data end. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
18	BAE	Indicates the BAE interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
17	BAR	Indicates the BAR interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
16	DMAEND	Indicates the DMA end interrupt.	RWC

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		0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	
15	AUTO_CMD12_DONE	Indicates AUTO_CMD12_DONE interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
14	DATA_FIFO_FULL	Indicate data FIFO is full interrupt. 0: the interrupt is not detected 1: the interrupt is detected	R
13	DATA_FIFO_EMP	Indicate data FIFO is empty interrupt. 0: the interrupt is not detected 1: the interrupt is detected	R
12	CRC_RES_ERR	Indicate response CRC error interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
11	CRC_READ_ERR	Indicate CRC read error interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
10	CRC_WRITE_ERR	Indicate CRC write error interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
9	TIME_OUT_RES	Indicate response time out interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
8	TIME_OUT_READ	Indicate read time out interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
7	SDIO	Indicates whether the interrupt from SDIO is detected. 0: The interrupt from SDIO is not detected 1: The interrupt from SDIO is detected	R
6	TXFIFO_WR_REQ	Transmit FIFO write request. Set if data FIFO becomes half empty. (the number of words is < 8) 0: No Request for data Write to MSC_TXFIFO 1: Request for data write to MSC_TXFIFO	R
5	RXFIFO_RD_REQ	Receive FIFO read request. Set if data FIFO becomes half full (the number of words is >= 8) or the entries in data FIFO	R

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		are the last read data. 0: No Request for data read from MSC_RXFIFO 1: Request for data read from MSC_RXFIFO	
4:3	Reserved	Writing has no effect, read as zero.	R
2	END_CMD_RES	Indicates whether the command/response sequence has been finished. 0: The command/response sequence has not been finished 1: The command/response sequence has been finished Write 1 to clear.	RWC
1	PRG_DONE	Indicates whether card has finished programming. 0: Card has not finished programming and is busy 1: Card has finished programming and is no longer busy Write 1 to clear.	RWC
0	DATA_TRAN_DONE	Indicates whether data transfer is done. Note that for stream read/write, only when CMD12 (STOP_TRANS) has been sent, is this bit set. 0: Data transfer is not complete 1: Data transfer has completed or an error has occurred Write 1 to clear.	RWC

25.7.2.12 MSC Command Index Register (MSC_CMD,0x002C)

	MSC_CMD																															Base + 0x002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CMD_INDEX					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5:0	CMD_INDEX	Specifies the command index to be executed.	RW

25.7.2.13 MSC Command Argument Register (MSC_ARG,0x0030)

	MSC_ARG																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ARG																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	ARG	Specifies the argument for the current command.	RW

25.7.2.14 MSC Response FIFO Register (MSC_RES,0x0034)

The read-only MMC/SD Response FIFO register (RES_FIFO) holds the response sent back to the MMC/SD controller after every command. The size of this FIFO is 8 x 16-bit. The RES_FIFO does not contain the 7-bit CRC for the response. The Status for CRC checking and response time-out status is in the status register MSC_STAT.

The first half-word read from the response FIFO is the most significant half-word of the received response.

	MSC_RES																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	DATA	Contains the response to the command that is sent by the MMC/SD controller.	R

25.7.2.15 MSC Receive FIFO Port Register (MSC_RXFIFO,0x0038)

The MSC_RXFIFO is used to read the data from a card. It is read-only to the software, and is read on 32-bit boundary. The size of this FIFO is 128 x 32-bit.

	MSC_RXFIFO																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	DATA	One word of read data.	R

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25.7.2.16 MSC Transmit FIFO Port Register (MSC_TXFIFO,0x003C)

The MSC_TXFIFO is used to write the data to a card. It is write-only to the software, and is written on 32-bit boundary. The size of this FIFO is 128 x 32-bit.

	MSC_TXFIFO																															Base + 0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	DATA	One word of write data.	W

25.7.2.17 MSC Low Power Mode Register (MSC_LPM,0x0040)

The MSC_LPM is used to control whether MSC controller enters Low-Power Mode.

	MSC_LPM																															Base + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV_SEL		SMP_SEL	Reserved																												LPM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	DRV_SEL	Drive clock selection 0: CMD and data are driven by MSC_CLK falling edge 1: CMD and data are driven by clock rising edge which is 1ns delayed by MSC_CLK 2: CMD and data are driven by clock rising edge which is 1/4 phase delayed by MSC_CLK 3: Reserved When this field is not zero, MSC_CLKRT.CLK_RATE must be set to 0.	RW
29	SMP_SEL	Sample clock selection 0: CMD and data are sampled by MSC_CLK rising edge 1: CMD and data are sampled by clock rising edge which is 1/4 or 1/2 phase delayed by MSC_CLK. When this field is 1, MSC_CLKRT.CLK_RATE must be set to 0.	
28:1	Reserved	Writing has no effect, read as zero.	R

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0	LPM	Low Power Mode Enable 0: Disable low power mode 1: Enable low power mode Clock will stop when card in idle (should be normally set to only MMC and SD cards. For SDIO cards, if interrupts must be detected, clock should not be stopped) When software sets the bit, MSC clock can auto be stopped. **NOTE:** when set the bit, the clock start and stop can be not use.	RW

25.7.2.18 MSC DMA Control Register (MSC_DMAC,0x0044)

The MSC_DMAC register is used to control the DMA transfer.

	MSC_DMAC																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								MODE_SEL	AOFST		ALIGNEN	INCR		DMASEL	DMAEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	MODE_SEL	Transfer mode selection. 0: Do not specify the transfer length. This is the standard transfer. 1: Specify the transfer length. If this mode is selected, the transfer performance can be improved.	
6:5	AOFST	Address Offset. This field is effective only when ALIGNEN is 1b. 00b:The lowest 2 bit of the data transfer start address is 00b 01b: The lowest 2 bit of the data transfer start address is 01b 10b: The lowest 2 bit of the data transfer start address is 10b 11b: The lowest 2 bit of the data transfer start address is 11b	RW
4	ALIGNEN	Align Enable 0: Only word boundary data transfer is supported 1: Byte boundary data transfer is supported	RW
3:2	INCR	Burst type selection. The field only effects to special DMA in MSC controller. 2'b00: The burst type of DMA is INCR16. 2'b01: The burst type of DMA is INCR32. 2'b10: The burst type of DMA is INCR64.	RW

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1	DMASEL	One of supported DMA modes is selected. 0: Special DMA in MSC controller is used 1: Common DMA in DMAC controller is used	RW
0	DMAEN	DMA Function Enable 0: Disable DMA function 1:Enable DMA function	RW

25.7.2.19 MSC DMA Descriptor Address Register (MSC_DMANDA,0x0048)

	MSC_DMANDA																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	NDA	SDMA Next Descriptor Physical Address The SDMA will change the register when a descriptor is read in. It should be 4-word aligned.	RW

25.7.2.20 MSC DMA Data Address Register (MSC_DMADA,0x004C)

	MSC_DMADA																															Base + 0x004C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DA	SDMA Data Physical Address The data address of the current descriptor will be copied to this field. The SDMA will increment it during the data transfer automatically.	R

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25.7.2.21 MSC DMA Data Length Register (MSC_DMALEN,0x0050)

	MSC_DMALEN																															Base + 0x0050
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LEN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LEN	SDMA Data Length to be Transferred Its unit is byte. The data length of the current descriptor will be copied to this field. The SDMA will decrement it during the data transfer automatically.	R

25.7.2.22 MSC DMA Command Register (MSC_DMACMD,0x0054)

	MSC_DMACMD																															Base + 0x0054
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDI								ID								Reserved					OFFSET		ALIGN_EN	Reserved						ENDI	LINK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	IDI	Identification of the Interrupt DMA. This field will copy the ID when a DMA transfer interrupt occurs. If the interrupt of DMA is disabled, the field will not change.	R
23:16	ID	Identification of Current DMA Transfer.	R
15:11	Reserved	It has no use in the current version.	R
10:9	OFFSET	Address Offset. This field is effective when ALIGN_EN is set to 1b. 00: data address[1:0] is 00b 01: data address[1:0] is 01b 10: data address[1:0] is 10b 11: data address[1:0] is 11b	R
8	ALIGN_EN	Address Align Enable.	R

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		This bit should be set to 1b if the data address is not word-aligned.	
7:2	Reserved	It has no use in the current version.	R
1	ENDI	Interrupt Enable for Current DMA Transfer End 0: Disable interrupt 1: Enable interrupt	R
0	LINK	Control the end of DMA Descriptor. 0: DMA will go to idle state after the current transmission is finished. The MSC_STAT.DMAEND will be set to 1b when the current read/write is finished. If the interrupt mask bit MSC_IMASK.DMAEND is 0b, the interrupt flag MSC_IFLG. DMAEND will be set to 1b also. 1: DMA will continue to fetch another descriptor.	R

25.7.2.23 MSC Control 2 Register (MSC_CTRL2,0x0058)

	MSC_CTRL2																															Base + 0x0058
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			PIP					Reserved_1	Reserved																		STPRM	Reserved_0	SMS		
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero.	R
28:24	PIP	Pin Level Interrupt Polarity 1: Interrupt can be trigged when pin level is high 0: Interrupt can be trigged when pin level is low	RW
23	Reserved_1	Inner usage, keep to 1.	RW
22:5	Reserved	Writing has no effect, read as zero.	R
4	STPRM	Stop Read Operation Mode Selection 0: Host can stop read operation during data transfer 1: Host only can stop read operation during block gap	RW
3	Reserved_0	Inner usage, keep to 0.	RW
2:0	SMS	Speed Mode Selection 000: Default speed 001: High speed 010: SDR12 011: SDR25 100: SDR50 Others: reserved	RW

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25.7.2.24 MSC RTFIFO Data Counter Register(MSC_RTCNT,0x005C)

	MSC_RTCNT																															Base + 0x005C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCNT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RTCNT	This field indicates how many data in word units are stored in RTFIFO.	R

25.8 Operation Flow

25.8.1 Data FIFOs

The controller FIFOs for the response tokens, received data, and transmitted data are MSC_RES, MSC_RXFIFO, and MSC_TXFIFO, respectively. These FIFOs are accessible by the software and are described in the following paragraphs.

25.8.1.1 Response FIFO (MSC_RES)

The response FIFO, MSC_RES, contains the response received from an MMC/SD card after a command is sent from the controller. MSC_RES is a read-only, 16-bit, and 8-entry deep FIFO.

The FIFO will hold all possible response lengths. Responses that are only one byte long are located on the LSB of the 16-bit entry in the FIFO. The first half-word read from the response FIFO is the most significant half-word of the received response. For example, if the response format is R1, then the response read from RES_FIFO is bit [47:32], bit[31:16], bit[15:0] and in the third half-word only the low 8-bit is effective response [15:8] and the high 8-bit is ignored. If the response format is R2, then the response read from MSC_RES is bit [135:8] and needs reading 8 times.

The FIFO does not contain the response CRC. The status of the CRC check is in the status register, MSC_STAT.

25.8.1.2 Receive/Transmit Data FIFO (MSC_RXFIFO/MSC_TXFIFO)

The receive data FIFO and transmit data FIFO share one 16-entry x 32-bit FIFO, because at one time data are only received or are only transmitted. If it is used to receive data, it is called MSC_RXFIFO and read-only. If it is used to transmit data, it is called MSC_TXFIFO and write-only.

Data FIFO and its controls are cleared to a starting state after a system reset or at the beginning of the

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operations which include data transfer. (MSC_CMDAT[DATA_EN] == 1)

If at any time MSC_RXFIFO becomes full and the data transmission is not complete, the controller turns the MSC_CLK off to prevent any overflows. When the clock is off, data transmission from the card stops until the clock is turned back on. After MSC_RXFIFO is not full, the controller turns the clock on to continue data transmission. The full status of the FIFO is registered in the MSC_STAT [DATA_FIFO_FULL] bit.

If at any time MSC_TXFIFO becomes empty and the data transmission is not complete, the controller turns the MSC_CLK off to prevent any under run. When the clock is off, data transmission to the card stops until the clock is turned back on. When MSC_TXFIFO is no longer empty, the controller automatically restarts the clock. The empty status of the FIFO is registered in the MSC_STAT [DATA_FIFO_EMPTY] bit.

The FIFO is readable on word (32-bit) boundaries. The max read/written number is 16 words. The controller can correctly process big-endian and little-endian data.

Because at the beginning of the operation which include data transfer (MSC_CMDAT [DATA_EN] == 1), Data FIFO and its controls are cleared, software should guarantee data in FIFO have been read/written before beginning a new command.

25.8.2 DMA and Program I/O

Software may communicate to the MSC controller via the DMA or program I/O. The SDMA and CDMA are supported at the same time. SDMA is the special DMA in MSC controller, while CDMA is the common DMA in DMAC controller.

25.8.2.1 Structure of SDMA Descriptor

SDMA is a descriptor DMA. And a descriptor can be linked to another one by the NDA until the LINK in the 4th word is set to 1b.

A SDMA descriptor includes 4 words.

Word 1: The physical address of the next SDMA descriptor.

Bits	Name	Description
31:0	NDA	Next descriptor physical address. It should be 4-word aligned.

Word 2: The system memory address where the data will be read from or stored to.

Bits	Name	Description
31:0	DA	Data Address.

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Word 3: The length of data to be transferred.

Bits	Name	Description
31:0	LEN	Unit is byte.

Word 4: The command for the current SDMA.

Bits	Name	Description
31:24	Reserved	It has no use in the current version.
23:16	ID	Identification of Current DMA Transfer.
15:2	Reserved	It has no use in the current version.
1	ENDI	Interrupt Enable for Current DMA Transfer End 0: Disable interrupt 1: Enable interrupt
0	LINK	Control the end of DMA Descriptor. 0: DMA will continue to fetch another descriptor. 1: DMA will go to idle state after the current transfer. The MSC_STAT.DMAEND will be set to 1b when the current read/write is finished. If the interrupt mask bit MSC_IMASK.DMAEND is 0b, the interrupt flag MSC_IFLG. DMAEND will be set to 1b also.

25.8.2.2 Operation of SDMA

Step 1: Prepare the descriptor in system memory

Step 2: If the address is not word boundary, it is suggested to configure MSC_DMAC.ALIGNEN and MSC_DMAC.AOFST

Step 3: Write the descriptor address to MSC_DMANDA

Step 4: Configure MSC controller to read or write operation, e,g, set MSC_NOB, MSC_BLEN and MSC_CMDAT.WRITE_READ etc.

Step 5: If DMAEND interrupt is wanted, clear MSC_IMASK.DMAEND, otherwise, set this bit

Step 6: Select SDMA by setting MSC_DMAC.DMASEL to 0b

Step 7: Start DMA transfer by setting MSC_DMAC.DMAEN

Step 8: Waiting the DMAEND interrupt (if interrupt is used) or status (if interrupt is not used)

Step 9: Disable the SDMA by configuring MSC_DMAC.DMAEN to 0b

25.8.2.3 Operation of CDMA

To access MSC_RXFIFO/MSC_TXFIFO with the DMA, the software must program the DMA to read or write the FIFO with source port width 32-bit, destination port width 32-bit, transfer data size 32-byte, transfer mode single. For example, to write 64 bytes of data to the MSC_TXFIFO, the software must program the DMA as follows:

```
DMA_DCTRn = 2                    // Write 2 32-bytes (64 bytes)
```


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DMA_DCCRn[SWDH] = 0 // source port width is 32-bit
DMA_DCCRn[DWDH] = 0 // destination port width is 32-bit
DMA_DCCRn[DS] = 4 // transfer data size is 32-byte
DMA_DCCRn[TM] = 4 // transfer mode is single
DMA_DCCRn[RDIL] = 0 // request detection interval length is 0

The number of 32-bytes should be calculated from the number of transferred bytes as follows:

The number of words = (The number of bytes + 31) / 32

If the number of transferred bytes is not the multiple of 4, the controller can correctly process endian.

The DMA trigger level is 8 words, that is to say, the DMA read trigger is when data words in MSC_RXFIFO is >= 8 and the DMA write trigger is when data words in MSC_TXFIFO is < 8. Software can also configure DMA registers based on requirements, but the above 32-byte transfer data size is most efficient.

25.8.2.4 Operation of Program I/O

With program I/O, the software waits for the MSC_IFLG [RXFIFO_RD_REQ] or MSC_IFLG [TXFIFO_WR_REQ] interrupts before reading or writing the respective FIFO.

NOTES:

1. The MSC_CMDAT [DMA_EN] bit must be set to a 1 to enable communication with the DMA and it must be set to a 0 to enable program I/O.
2. DMA can be enabled only after MSC_CMDAT is written, because MSC_CMDAT [DATA_EN] is used to reset TX/RXFIFO.

25.8.3 Start and Stop clock

The software stops the clock as follows:

1. Write MSC_CTRL with 0x01 to stop the MMC/SD bus clock.
2. Wait until MSC_STAT[CLK_EN] becomes zero.

To start the clock the software writes MSC_CTRL with 0x02.

25.8.4 Software Reset

Reset includes the MSC reset and the card reset.

The MSC reset is through MSC_CTRL [RESET] bit.

The card reset is to make the card into idle state. CMD0 (GO_IDLE_STATE) sets the MMC and SD memory cards into idle state. CMD52 (IO_RW_DIRECT, with argument 0x88000C08) reset the SD I/O card. The MMC/SD card are initialized with a default relative card address (RCA = 0x0001 for MMC and RCA = 0x0000 for SD) and with a default driver stage register setting (lowest speed, highest driving current capability).

The following registers must be set before the clock is started:

Step 1. Stop the clock.
Step 2. Set MSC_CTRL register to 0x08 to reset MSC.

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Step 3. Wait while MSC_STAT [IS_RESETTING] is 1.
Step 4. Set MSC_CMD with CMD0.
Step 5. Update the MSC_CMDAT register as follows:
  a Write 0x0000 to MSC_CMDAT [RESPONSE_FORMAT].
  b Clear the MSC_CMDAT [DATA_EN] bit.
  c Clear the MSC_CMDAT [BUSY] bit.
  d Clear the MSC_CMDAT [INIT] bit.
Step 6. Start the clock.
Step 7. Start the operation. (write MSC_CTRL with 0x04)
Step 8. Wait for the END_CMD_RES interrupt.
Step 9. Set MSC_CMD with CMD52.
Step 10. Set MSC_ARG with 0x88000C08.
Step 11. Update the MSC_CMDAT register as follows:
  a Write 0x005 to MSC_CMDAT [RESPONSE_FORMAT].
  b Clear the MSC_CMDAT [DATA_EN] bit.
  c Clear the MSC_CMDAT [BUSY] bit.
  d Clear the MSC_CMDAT [INIT] bit.
Step 12. Start the operation.
Step 13. Wait for the END_CMD_RES interrupt.

25.8.5 Voltage Validation and Card Registry

At most 10 MMC and 1 SD (either SDMEM or SDIO) can be inserted MMC/SD bus at the same time, and their voltage validation and card registry steps are different, so the software should be programmed as follows:

Step 1. Check whether SDIO card is inserted.
Step 2. Check whether SDMEM card is inserted.
Step 3. Check whether MMC cards are inserted.

25.8.5.1 Check SDIO

The commands are sent as follows:

Step 1. (Optional) Send CMD52 (IO_RW_DIRECT) with argument 0x88000C08 to reset SDIO card.
Step 2. Send CMD5 (IO_SEND_OP_CMD) to validate voltage.
Step 3. If the response is correct and the number of IO functions > 0, then continue, else go to check SDMEM.
Step 4. If C-bit in the response is ready (the initialization has finished), go to 6.
Step 5. Send CMD5 (IO_SEND_OP_CMD) to validate voltage, then go to 4.
Step 6. If memory-present-bit in the response is true, then it is a combo card (SDIO + Memory), else it is only a SDIO card.
Step 7. If it is a combo card, go to check SDMEM to initialize the memory part.
Step 8. Send CMD3 (SET_RELATIVE_ADDR) to let the card publish a RCA. The RCA is

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returned from the response.

Step 9. If do not accept the new RCA, go to 8, else record the new RCA.

Step 10. Go to check MMC, because we can assure that there is no SDMEM card.

25.8.5.2 Check SDMEM

If there is no SDIO card or there is a combo card, continue to check SDMEM.

The commands are sent as follows:

Step 1. (Optional) Send CMD0 (GO_IDLE_STATE) to reset MMC and SDMEM card. This command has no response.

Step 2. Send CMD55. Here the default RCA 0x0000 is used for CMD55.

Step 3. If the response is correct (CMD55 has response), then continue, else go to check MMC.

Step 4. Send ACMD41 (SD_SEND_OP_CMD) to validate voltage (the general OCR value is 0x00FF8000).

Step 5. If the initialization has finished, go to 7. (The response is the OCR register and it includes a status information bit (bit [31]). This status bit is set if the card power up procedure has been finished. As long as the card is busy, the corresponding bit[31] is set to LOW.)

Step 6. Send CMD55 and ACMD41 to validate voltage, and then go to 5.

Step 7. Send CMD2 (ALL_SEND_CID) to get the card CID.

Step 8. Send CMD3 (SET_RELATIVE_ADDR) to let card publish a RCA. The RCA is returned from the response.

Step 9. If do not accept the new RCA, go to 8, else record the new RCA.

Step 10. Go to check MMC.

25.8.5.3 Check MMC

Because there may be several MMC card, so some steps (5 ~ 8) should be repeated several times.

The commands are sent as follows:

Step 1. Send CMD1 (SEND_OP_CMD) to validate voltage (the general OCR value is 0x00FF88000).

Step 2. If the response is correct, then continue, else go to 9.

Step 3. If the initialization has finished, go to 5. (The response is the OCR register and it includes a status information bit (bit [31]). This status bit is set if the card power up procedure has been finished. As long as the card is busy, the corresponding bit[31] is set to LOW.)

Step 4. Send CMD1 (SEND_OP_CMD) to validate voltage, and then go to 3.

Step 5. Send CMD2 (ALL_SEND_CID) to get the card CID.

Step 6. If the response timeout occurs, go to 9.

Step 7. Send CMD3 (SET_RELATIVE_ADDR) to assign the card a RCA.

Step 8. If there are other MMC cards, then go to 5.

Step 9. Finish.

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25.8.6 Single Data Block Write

In a single block write command, the following registers must be set before the operation is started:

Step 1. Set MSC_NOB register to 0x0001.

Step 2. Set MSC_BLKLEN to the number of bytes per block.

Step 3. Update the MSC_CMDAT register as follows:

a Write 0x001 to MSC_CMDAT [RESPONSE_FORMAT].

b Write 0x2 to MSC_CMDAT [BUS_WIDTH] if the card is SD, else clear it.

c Set the MSC_CMDAT [DATA_EN] bit.

d Set the MSC_CMDAT [WRITE_READ] bit.

e Clear the MSC_CMDAT [STREAM_BLOCK] bit.

f Clear the MSC_CMDAT [BUSY] bit.

g Clear the MSC_CMDAT [INIT] bit.

Step 4. Start the operation.

Step 5. Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

Step 1. Wait for the MSC_IFLG [END_CMD_RES] interrupt.

Step 2. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.

At the same time write data to the MSC_TXFIFO and continue until all of the data have been written to the FIFO.

Step 3. Wait for MSC_IFLG [PROG_DONE] interrupt. This interrupt indicates that the card has finished programming. Certainly software may start another command sequence on a different card.

Step 4. Read the MSC_STAT register to verify the status of the transaction (i.e. CRC error status).

To address a different card, the software sends a select command to that card by sending a basic no data command and response transaction. To address the same card, the software must wait for MSC_IFLG [PROG_DONE] interrupt. This ensures that the card is not in the busy state.

In addition, CMD26 (PROGRAM_CID), CMD27 (PROGRAM_CSD), CMD42 (LOCK/UNLOCK), CMD56 (GEN_CMD: write) and CMD53 (single block write) operations are similar to single block write.

25.8.7 Single Block Read

In a single block read command, the following registers must be set before the operation is started:

Step 1. Set MSC_NOB register to 0x0001.

Step 2. Set MSC_BLKLEN register to the number of bytes per block.

Step 3. Update the following bits in the MSC_CMDAT register:

a Write 0x001 to MSC_CMDAT [RESPONSE_FORMAT].

b Write 0x2 to MSC_CMDAT [BUS_WIDTH] if the card is SD, else clear it.

c Set the MSC_CMDAT [DATA_EN] bit.

d Clear the MSC_CMDAT [WRITE_READ] bit.

e Clear the MSC_CMDAT [STREAM_BLOCK] bit.

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f Clear the MSC_CMDAT [BUSY] bit.

g Clear the MSC_CMDAT [INIT] bit.

Step 4. Start the operation.

Step 5. Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

Step 1. Wait for the MSC_IFLG [END_CMD_RES] interrupt.

Step 2. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
At the same time read data from the MSC_RXFIFO as data becomes available in the FIFO, and continue reading until all data is read from the FIFO.

Step 3. Read the MSC_STAT register to verify the status of the transaction (i.e. CRC error status).

In addition, CMD30 (SEND_WRITE_PROT), ACMD13 (SD_STATUS), CMD56 (GEN_CMD-read), ACMD51 (SEND_SCR) and CMD53 (single block read) are similar to single block read.

25.8.8 Multiple Block Write

The multiple block write mode is similar to the single block write mode, except that multiple blocks of data are transferred. Each block is the same length. All the registers are set as they are for the single block write, except that the MSC_NOB register is set to the number of blocks to be written.

The multiple block write mode also requires a stop transmission command, CMD12, after the data is transferred to the card. After the MSC_IFLG [DATA_TRAN_DONE] interrupt occurs, the software must program the controller register to send a stop data transmission command.

If multiple block write with pre-defined block count (refer to MMC spec v-3.3) is used, CMD12 should not be sent.

For SDIO card, CMD53 (multiple block write) is also similar, but when IO abort (CMD52) is sent, MSC_CMDAT [IO_ABORT] should be 1.

Table 25-6 How to stop multiple block write

Operation	Stop condition	Software processing
Open-ended or SDIO infinite	After write MSC_NOB blocks	1 Wait for DATA_TARN_DONE interrupt. 2 Send CMD12 or CMD52. (IO abort) 3 Wait for END_CMD_RES and PRG_DONE interrupt.
Open-ended or SDIO infinite	Stop writing in advance (not write MSC_NOB blocks)	1 Set MSC_CTRL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES and PRG_DONE interrupt.

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Predefined block or SDIO finite	After writing MSC_NOB blocks	1 Wait for DATA_TRAN_DONE interrupt.
Predefined block or SDIO finite	Stop writing in advance (not write MSC_NOB blocks)	1 Set MSC_CTRL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES and PRG_DONE interrupt.

25.8.9 Multiple Block Read

The multiple blocks read mode is similar to the single block read mode, except that multiple blocks of data are transferred. Each block is the same length. All the registers are set as they are for the single block read, except that the MSC_NOB register is set to the number of blocks to be read.

The multiple blocks read mode requires a stop transmission command, CMD12, after the data from the card is received. After the MSC_IFLG [DATA_TRAN_DONE] interrupt has occurred, the software must program the controller registers to send a stop data transmission command.

If multiple block read with pre-defined block count (refer to MMC spec v-3.3) is used, CMD12 should not be sent.

For SDIO card, CMD53 (multiple block read) is also similar, but when IO abort (CMD52) is sent, MSC_CMDAT [IO_ABORT] should be 1.

Table 25-7 How to stop multiple block read

Operation	Stop condition	Software processing
Open-ended or SDIO infinite	After reading MSC_NOB blocks	1 Wait for DATA_TRAN_DONE interrupt. 2 Send CMD12 or CMD52. (IO abort) 3 Wait for END_CMD_RES interrupt.
Open-ended or SDIO infinite	Stop reading in advance (not write MSC_NOB blocks)	1 Set MSC_CTRL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES interrupt.
Predefined block or SDIO finite	After reading MSC_NOB blocks	1 Wait for DATA_TRAN_DONE interrupt.
Predefined block or SDIO finite	Stop reading in advance (not write MSC_NOB blocks)	1 Set MSC_CTRL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES interrupt.

25.8.10 Stream Write (MMC)

In a stream write command, the following registers must be set before the operation is started:

1 Update MSC_CMDAT register as follows:
   - a Write 0x001 to the MSC_CMDAT [RESPONSE_FORMAT].
   - b Clear the MSC_CMDAT [BUS_WIDTH] because only MMC support stream write.

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   c Set the MSC_CMDAT [DATA_EN] bit.
   d Set the MSC_CMDAT [WRITE_READ] bit.
   e Set the MSC_CMDAT [STREAM_BLOCK] bit.
   f Clear the MSC_CMDAT [BUSY] bit.
   g Clear the MSC_CMDAT [INIT] bit.
2 Start the operation.
3 Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

1 Wait for the MSC_IFLG [END_CMD_RES] interrupt.
2 Write data to the MSC_TXFIFO and continue until all of the data is written to the Data FIFO.
3 Stop clock. Wait until MSC_STAT[CLK_EN] becomes 0. The clock must be stopped.
4 Set the command registers for a stop transaction command (CMD12) and other registers.
5 Start the clock and start the operation.
6 Wait for the MSC_IFLG [END_CMD_ERS] interrupt.
7 Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
8 Wait for the MSC_IFLG [PRG_DONE] interrupt. This interrupt indicates that the card has finished programming. Certainly software may start another command sequence on a different card.
9 Read the MSC_STAT register to verify the status of the transaction.

To address a different card, the software must send a select command to that card by sending a basic no data command and response transaction. To address the same card, the software must wait for MSC_IFLG [PRG_DONE] interrupt. This ensures that the card is not in the busy state.

If partial blocks are allowed (if CSD parameter WRITE_BL_PARTIAL is set) the data stream can start and stop at any address within the card address space, otherwise it shall start and stop only at block boundaries. If WRITE_BL_PARTIAL is not set, 16 more stuff bytes need to be written after the useful written data, otherwise only write the useful written data.

25.8.11 Stream Read (MMC)

In a stream read command, the following registers must be set before the operation is turned on:

1 Update the MSC_CMDAT register as follows:
   a Write 0x01 to the MSC_CMDAT [RESPONSE_FORMAT].
   b Clear the MSC_CMDAT [BUS_WIDTH] because only MMC support stream read.
   c Clear the MSC_CMDAT [WRITE_READ] bit.
   d Set the MSC_CMDAT [STREAM_BLOCK] bit.
   e Clear the MSC_CMDAT [BUSY] bit.
   f Clear the MSC_CMDAT [INIT] bit.
2 Start the operation.
3 Write MSC_IMASK with some value to unmask the expected interrupts.

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Then the software must perform the following steps:

1. Wait for the MSC_IFLG [END_CMD_RES] interrupt.
2. Read data from the MSC_RXFIFO and continue until all of the expected data has been read from the FIFO.
3. Write MSC_CTRL [EXIT_TRANSER] with 1. If MSC_STAT[DATA_FIFO_FULL] is 1, then read MSC_RXFIFO to make it not full. Because if data FIFO is full, MSC_CLK is stopped. Here, the data FIFO contains useless data.
4. Set the command registers for a stop transaction command (CMD12) and send it. There is no need to stop the clock.
5. Wait for the MSC_IFLG [END_CMD_RES].
6. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
7. Read the MSC_STAT register to verify the status of the transaction.

25.8.12 Erase, Select/Deselect and Stop

For CMD7 (SELECT/DESELECT_CARD), CMD12 (STOP_TRANSMISSION) and CMD38 (ERASE), the following registers must be set before the operation is started:

1. Update the MSC_CMDAT register as follows:
   a. Write 0x01 to the MSC_CMDAT [RESPONSE_FORMAT].
   b. Clear the MSC_CMDAT [DATA_EN] bit.
   c. Clear the MSC_CMDAT [WRITE_READ] bit.
   d. Clear the MSC_CMDAT [STREAM_BLOCK] bit.
   e. Set the MSC_CMDAT [BUSY] bit.
   f. Clear the MSC_CMDAT [INIT] bit.
2. Start the operation.
3. Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

1. Wait for the MSC_IFLG [END_CMD_RES] interrupt.
2. Wait for the MSC_IFLG [PRG_DONE] interrupt. If CMD12 is sent to terminate data read operation, then there is no need to wait for MSC_IFLG [PRG_DONE] interrupt. This interrupt indicates that the card has finished programming. Certainly software may start another command sequence on a different card.

25.8.13 SDIO Suspend/Resume

The actual suspend/resume steps are as follows:

1. During data transfer, send CMD52 to require suspend. BR and RAW flag should be 1.
2. If BS flag in the response is 0, then suspend has been accepted and goto 4.
3. Send CMD52 to query card status. R flag should be 1. Go to 2.
4. Write MSC_CTRL [EXIT_TRANSFER] with 1.
5. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
6. Read MSC_NOB, MSC_SNOB and etc, save them into variables.

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7 Set registers for high priority transfer and start it.
8 Wait until high priority transfer is finished.
9 Restore registers from variables, but MSC_NOB should be (MSC_NOB – MSC_SNOB).
10 Send CMD52 to require resume. FSx should be resumed function number.

25.8.14 SDIO Read Wait

The actual Read Wait steps are as follows:

1 During multiple block read, read MSC_SNOB. If MSC_SNOB is nearby or equal to MSC_NOB, no need to use Read Wait.
2 Write MSC_CTRL [START_READ WAIT] with 1.
3 Wait until MSC_STAT [IS_READ WAIT] becomes 1.
4 Send CMD52 to query card status.
5 Write MSC_CTRL [STOP_READ WAIT] with 1.

25.8.15 Operation and Interrupt

The software can use polling-status method to operate the MMC/SD card, but this is not the proposed method, because its performance is very low. The proposed method is to use interrupt. Generally there are fixed necessary steps to finish each command. The steps are as follows:

1 (Optional) Stop clock. Poll CLK_EN.
2 Fill the registers (MSC_CMD, MSC_CMDAT, MSC_ARG, MSC_CLKRT, and etc).
3 (Optional) Start clock.
4 Start the operation. Wait for the MSC_IFLG [END_CMD_RES] interrupt.
5 Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
6 Send STOP_TRANS (CMD12) or I/O abort (CMD52). Wait for the MSC_IFLG [END_CMD_ERS] interrupt.
7 Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
8 Wait for the MSC_IFLG [PRG_DONE] interrupt.

25.9 Index

Table 25-8 Description of Proprietary Vocabulary

Name	Description
Block	A number of bytes, basic data transfer unit
CID	Card Identification number register
CRC	Cyclic Redundancy Check
CSD	Card specific Data register
OCR	Operation Conditions Register
Open-drain	A logical interface operation mode. An external resistor or current source is used to pull the interface level to HIGH, the internal transistor pushes it to LOW.

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Push-pull	A logical interface operation mode, a complementary pair of transistors is used to push the interface level to High or Low

Table 25-9 The mapping between Commands and Steps

Index	Abbreviation	1	2	3	4	5	6	7	8	Comments
CMD0	GO_IDLE_STATE	Y	Y	Y	Y					
CMD1	SEND_OP_COND	Y	Y	Y	Y					
CMD2	ALL_SEND_CID	Y	Y	Y	Y					
CMD3	SET_RELATIVE_ADDR	Y	Y	Y	Y					
CMD4	SET_DSR	Y	Y	Y	Y					
CMD7	SELECT/DSELECT_CARD	Y	Y	Y	Y				Y	
CMD9	SEND_CID	Y	Y	Y	Y					
CMD10	SEND_CSD	Y	Y	Y	Y					
CMD11	READ_DAT_UNTIL_STOP	Y	Y	Y	Y		Y	Y		
CMD12	STOP_TRANSMISSION	Y	Y	Y	Y				Y	
CMD13	SEND_STATUS	Y	Y	Y	Y					
CMD15	GO_INACTIVE_STATE	Y	Y	Y	Y					
CMD16	SET_BLOCKLEN	Y	Y	Y	Y					
CMD17	READ_SINGLE_BLOCK	Y	Y	Y	Y	Y				
CMD18	READ_MULTIPLE_BLOCK	Y	Y	Y	Y	Y	Y			Open-ended
CMD18	READ_MULTIPLE_BLOCK	Y	Y	Y	Y	Y				Predefine blocks
CMD20	WRITE_DAT_UNTIL_STOP	Y	Y	Y	Y		Y	Y	Y	
CMD23	SET_BLOCK_COUNT	Y	Y	Y	Y					
CMD24	WRITE_SINGLE_BLOCK	Y	Y	Y	Y	Y			Y	
CMD25	WRITE_MULTIPLE_BLOCK	Y	Y	Y	Y	Y	Y		Y	Open-ended
CMD25	WRITE_MULTIPLE_BLOCK	Y	Y	Y	Y	Y			Y	Predefine blocks
CMD26	PROGRAM_CID	Y	Y	Y	Y	Y			Y	
CMD27	PROGRAM_CSD	Y	Y	Y	Y	Y			Y	
CMD28	SET_WRITE_PROT	Y	Y	Y	Y				Y	
CMD29	CLR_WRITE_PROT	Y	Y	Y	Y				Y	
CMD30	SEND_WRITE_PROT	Y	Y	Y	Y	Y				
CMD32	ERASE_WR_BLOCK_START	Y	Y	Y	Y					
CMD33	ERASE_WR_BLOCK_END	Y	Y	Y	Y					
CMD35	ERASE_GROUP_START	Y	Y	Y	Y					
CMD36	ERASE_GROUP_END	Y	Y	Y	Y					
CMD38	ERASE	Y	Y	Y	Y				Y	
CMD39	FAST_IO	Y	Y	Y	Y					
CMD40	GO_IRQ_STATE	Y	Y	Y	Y					
CMD42	LOCK/UNLOCK	Y	Y	Y	Y	Y			Y	
CMD55	APP_CMD	Y	Y	Y	Y					
CMD56	GEN_CMD	Y	Y	Y	Y	Y				Read

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CMD56	GEN_CMD	Y	Y	Y	Y	Y			Y	Write
ACMD6	SET_BUS_WIDTH	Y	Y	Y	Y					
ACMD13	SD_STATUS	Y	Y	Y	Y	Y				
ACMD22	SEND_NUM_WR_BLOCKS	Y	Y	Y	Y					
ACMD23	SET_WR_BLOCK_COUNT	Y	Y	Y	Y					
ACMD41	SD_SEND_OP_COND	Y	Y	Y	Y					
ACMD42	SET_CLR_CARD_DETECT	Y	Y	Y	Y					
ACMD51	SEND_SCR	Y	Y	Y	Y	Y				

Note:

For stream read/write, STOP_CMD is sent after finishing data transfer. For write, STOP_CMD is with the last six bytes. For read, STOP_CMD is sent after receiving data and card sends some data which MSC ignores.

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26 ON-THE-GO Controller(OTG)

26.1 Overview

This chapter describes the USB On-The-Go (OTG) implemented in the processor.

The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously accessible portable peripherals. Many of these portable devices would benefit a lot from being able to communicate to each other over the USB interface. And OTG make this possible. An OTG device can plays the role of both host and device.

Familiarity with the Universal Serial Bus Specification, Revision 1.1 and OTG supplement are necessary to fully understand the material contained in this section.

26.2 Features

- Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the *On-The-Go* supplement to the USB 2.0 specification
- Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- UTMI+ Level 3 Transceiver Interface
- Soft connect/disconnect
- 16 Endpoints
- Supports control, interrupt, ISO and bulk transfer

26.3 Functional Description

The OTG is a Dual-Role Device(DRD) controller that supports both device and host functions and complies fully with the On-The-Go Supplement to the USB 2.0 Specification ,Revision 1.3a and Revision 2.0.It can also be configured as a host-only or device-only controller , fully compliant with the USB 2.0 Specification.

26.4 Pins Description

DRV_VBUS：PC17,USB 5-V Signal.

Function: This is the USB 5-V supply. A charge pump external to USB2.0 picoPHY must provide power to this pin. The nominal voltage for this pin is 5V. If VBUS is not used ,leave it floating.

26.5 Data Format Description

Support UTMI 8/16 for the USB-Phy Interface.

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26.6 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   RC- Read only, and Clear to 0 by read
   RS- Read only, and Set to 1 by read
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

26.6.1 Register Memory Map

Table 26-1 Registers Memory Map Base Address

Name	Base	Description
OTG	0x13500000	Address base of OTG

The On-The-Go Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 26-2 On-The-Go（OTG） Registers Map

Name	RW	Reset Value	Address Offset	Access Size
GOTGCTL	RW	0x0???_0000	0x000	32
GOTGINT	RW	0x0000_0000	0x004	32
GAHBCFG	RW	0x0000_0000	0x008	32
GUSBCFG	RW	0x0?00_140?	0x00C	32
GRSTCTL	RW	0x8000_0000	0x010	32
GINTSTS	RW	0x0400_0020	0x014	32
GINTMSK	RW	0x0000_0000	0x018	32
GRXSTSR	R	0x0000_0000	0x01C	32
GRXSTSP	R	0x0000_0000	0x020	32
GRXFSIZ	RW	0x0000_????	0x024	32
GNPTXFSIZ	RW	0x????_????	0x028	32
GNPTXSTS	RW	0x00??_????	0x02C	32

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GHWCFG1	R	0x????_????	0x044	32
GHWCFG2	R	0x????_????	0x048	32
GHWCFG3	R	0x????_????	0x04C	32
GHWCFG4	R	0x????_?0??	0x050	32
GDFIFOCFG	RW	0x????_????	0x05C	32
HPTXFSIZ	RW	0x????_????	0x100	32
DIEPTXFn	RW	0x????_????	0x104+n*0x4	32
HCFG	RW	0x0000_0200	0x400	32
HFIR	RW	0x0000_EA60	0x404	32
HFNUM	R	0x0000_3FFF	0x408	32
HPTXSTS	R	0x00??_????	0x410	32
HAINT	R	0x0000_0000	0x414	32
HAINTMAK	RW	0x0000_0000	0x418	32
HPRT	RW	0x0000_0000	0x440	32
HCCHARn	RW	0x0000_0000	0x500+n*0x20	32
HCSPLTn	RW	0x0000_0000	0x504+n*0x20	32
HCINTn	RW	0x0000_0000	0x508+n*0x20	32
HCINTMSKn	RW	0x0000_0000	0x50c+n*0x20	32
HCTSIZn	RW	0x0000_0000	0x510+n*0x20	32
HCDMAn	RW	0x0000_0000	0x514+n*0x20	32
HCDMABn	R	0x????_????	0x51C+n*0x20	32
DCFG	RW	0x0820_0000	0x800	32
DCTL	RW	0x0000_0002	0x804	32
DSTS	R	0x0000_0002	0x808	32
DIEPMSK	RW	0x0000_0000	0x810	32
DOEPMSK	RW	0x0000_0000	0x814	32
DAINT	R	0x0000_0000	0x818	32
DAINTMSK	RW	0x0000_0000	0x81C	32
DTKNQR1	R	0x0000_0000	0x820	32
DTKNQR2	R	0x0000_0000	0x824	32
DTKNQR3	R	0x0000_0000	0x830	32
DTKNQR4	R	0x0000_0000	0x834	32
DVBUSDIS	RW	0x0000_????	0x828	32
DVBUSPULSE	RW	0x0000_0???	0x82C	32
DTHRCTL	RW	0x0810_0020	0x830	32
DIEPEMPMSK	RW	0x0000_0000	0x834	32
DEACHINT	R	0x0000_0000	0x838	32
DEACHINTMSK	RW	0x0000_0000	0x83C	32
DIEPEACHMSKn	RW	0x0000_0000	0x840	32
DOEPEACHMSKn	RW	0x0000_0000	0x844	32
DIEPCTL0	RW	0x0000_8000	0x900	32
DOEPCTL0	RW	0x0000_8000	0xB00	32

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DIEPCTLn/DOEPCTLn	RW	0x0000_0000	0x900/0xB00+n*0x20	32
DIEPINTn/DOEPINTn	RW	0x0000_0080	0x908/0xB08+n*0x20	32
DIEPTSIZ0/DOEPTSIZ0	RW	0x0000_0000	0x910/0xB10	32
DIEPTSIZn/DOEPTSIZn	RW	0x0000_0000	0x910/0xB10+n*0x20	32
DIEPDMAn/DOEPDMAn	RW	0x????_????	0x914/0xB14+n*0x20	32
DIEPDMABn/DOEPDMABn	R	0x????_????	0x91C/0xB1C+n*0x20	32
DTXFSTSn	R	0x0000_0000	0x918	32

26.6.2 Register and Fields Description

26.6.2.1 Control and Status Register (GOTGCTL,0x000)

	GOTGCTL																															Base + 0x000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				chirpen	MultValIdBc					Reserved	OTGVer	BSesVld	ASesVld	DbncTime	ConIDSts	Reserved				DevHNPEn	HstSetHNPEn	HNPReq	HstNegScs	BvalidOvVa	BvalidOvEn	AvalidOvVal	AvalidOvEn	VbvalidOvVal	VbvalidOvEn	SesReq	SesReqScs
RST	0	0	0	0	0	?	?	?	?	?	0	0	?	?	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31:26	Reserved	Host and Device	R
27	Chirp On Enable (ChirpEn) This bit when programmed to 1'b1 results in the core asserting chirp_on before sending an actual Chirp "K" signal on USB. This bit is present only if OTG_BC_SUPPORT = 1.If OTG_BC_SUPPORT!=1, this bit is a reserved bit.	Device only	RW
26:22[1]	Multi Valued ID pin (MultValIdBc) Battery Charger ACA inputs in the following order: Bit 26 - rid_float. Bit 25 - rid_gnd Bit 24 - rid_a Bit 23 - rid_b Bit 22 - rid_c These bits are valid only if OTG_BC_SUPPORT=1, otherwise they are reserved.	Host and Device	R
21	Reserved	Host and Device	R
20	OTG Version (OTGVer) Indicates the OTG revision. 1'b0: OTG Version 1.3. In this version the core supports Data line pulsing and VBus pulsing for SRP. 1'b1: OTG Version 2.0. In this version the core supports only	Host and Device	RW

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	Data line pulsing for SRP.		
19	B-Session Valid (BSesVld) Indicates the Device mode transceiver status. 1'b0: B-session is not valid. 1'b1: B-session is valid. In OTG mode, you can use this bit to determine if the device is connected or disconnected. **Note:** If you do not enable OTG features (such as SRP and HNP), the read reset value will be 1.The vbus assigns the values internally for non- SRP or non-HNP configurations. In case of OTG_MODE=0, the reset value of this bit is 1'b0.	Device only	R
18	A-Session Valid (ASesVld) Indicates the Host mode transceiver status. 1'b0: A-session is not valid 1'b1: A-session is valid **Note:** If you do not enable OTG features (such as SRP and HNP), the read reset value will be 1.The vbus assigns the values internally for non- SRP or non-HNP configurations. In device mode, this bit is reserved.	Host only	R
17	Long/Short Debounce Time (DbncTime) Indicates the debounce time of a detected connection. 1'b0: Long debounce time, used for physical connections (100 ms + 2.5 μs) 1'b1: Short debounce time, used for soft connections (2.5 μs)	Host only	R
16	Connector ID Status (ConIDSts) Indicates the connector ID status on a connect event. 1'b0: The DWC_otg core is in A-Device mode 1'b1: The DWC_otg core is in B-Device mode	Host and Device	R
15:12	Reserved	Host and Device	R
11	Device HNP Enabled (DevHNPEn) The application sets this bit when it successfully receives a SetFeature.SetHNPEnable command from the connected USB host. 1'b0: HNP is not enabled in the application 1'b1: HNP is enabled in the application	Device Only OTG configurations	RW
10	Host Set HNP Enable (HstSetHNPEn) The application sets this bit when it has successfully enabled HNP (using the SetFeature.SetHNPEnable command) on the connected device. 1'b0: Host Set HNP is not enabled 1'b1: Host Set HNP is enabled	Device Only OTG configurations	RW
9	HNP Request (HNPReq)	Device Only	RW

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	The application sets this bit to initiate an HNP request to the connected USB host. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. 1'b0: No HNP request 1'b1: HNP request	OTG configurations	
8	Host Negotiation Success (HstNegScs) The core sets this bit when host negotiation is successful. The core clears this bit when the HNP Request (HNPReq) bit in this register is set. 1'b0: Host negotiation failure 1'b1: Host negotiation success	Device only	R
7	B-Peripheral Session Valid OverrideValue (BvalidOvVal) This bit is used to set the Override value for Bvalid signal when GOTGCTL.BvalidOvEn is set. 1'b0: Bvalid value is 1'b0 when GOTGCTL.BvalidOvEn = 1. 1'b1: Bvalid value is 1'b1 when GOTGCTL.BvalidOvEn = 1.	Device only	RW
6	B-Peripheral Session Valid Override Enable (BvalidOvEn) This bit is used to enable/disable the software to override the Bvalid signal using the GOTGCTL.BvalidOvVal. 1'b1: Internally Bvalid received from the PHY is overridden with GOTGCTL.BvalidOvVal. 1'b0: Override is disabled and Bvalid signal from the respective PHY selected is used internally by the core.	Device only	RW
5	A-Peripheral Session Valid OverrideValue (AvalidOvVal) This bit is used to set the Override value for Avalid signal when GOTGCTL.AvalidOvEn is set. 1'b0: Avalid value is 1'b0 when GOTGCTL.AvalidOvEn = 1. 1'b1: Avalid value is 1'b1 when GOTGCTL.AvalidOvEn = 1.	Host only	RW
4	A-Peripheral Session Valid Override Enable (AvalidOvEn) This bit is used to enable/disable the software to override the Avalid signal using the GOTGCTL.AvalidOvVal. 1'b1: Internally Avalid received from the PHY is overridden with GOTGCTL.AvalidOvVal. 1'b0: Override is disabled and Avalid signal from the respective PHY is used internally by the core.	Host only	RW
3	VBUS Valid OverrideValue (VbvalidOvVal) This bit is used to set the Override value for vbus valid signal when GOTGCTL.VbusvalidOvEn is set. 1'b0: vbusvalid value is 1'b0 when GOTGCTL.VbvalidOvEn = 1.	Host only	RW

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	1'b1: vbusvalid value is 1'b1 when GOTGCTL.VbvalidOvEn = 1.		
2	VBUS Valid Override Enable (VbvalidOvEn) This bit is used to enable/disable the software to override the vbus-valid signal using the GOTGCTL.vbvalidOvVal. 1'b1: The vbus-valid signal received from the PHY is overridden with GOTGCTL.vbvalidOvVal. 1'b0: Override is disabled and avalid signal from the respective PHY is used internally by the core.	Host only	RW
1	Session Request (SesReq) The application sets this bit to initiate a session request on the USB. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. If you use the USB 1.1 Full-Speed Serial Transceiver interface to initiate the session request, the application must wait until the VBUS discharges to 0.2 V, after the B-Session Valid bit in this register (GOTGCTL.BSesVld) is cleared. This discharge time varies between different PHYs and can be obtained from the PHY vendor. 1'b0: No session request 1'b1: Session request	Device only	RW
0	Session Request Success (SesReqScs) The core sets this bit when a session request initiation is successful. 1'b0: Session request failure 1'b1: Session request success	Device only	R

Note:

[1]. bits [26:22]: configurable. The reset value is unknown if OTG_BC_ SUPPORT=1 and 0 otherwise.

26.6.2.2 Interrupt Register (GOTGINT,0x004)

	GOTGINT																															Base + 0x004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												MVIC	DbnceDone	ADevTOUTCh		Reserved						HstNegSucStsChng	SesReqSucStsChng	Reserved					SesEndDet	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	Mode	R/W
31:21	Reserved	Host and Device	R
20	Multi-Valued input changed (MVIC) This bit when set indicates that there is a change in the value of at least one ACA pin value. This bit is present only if OTG_BC_SUPPORT = 1, otherwise it is reserved.	Host and Device	RW[1]
19	Debounce Done (DbnceDone) The core sets this bit when the debounce is completed after the device connect. The application can start driving USB reset after seeing this interrupt. This bit is only valid when the HNP Capable or SRP Capable bit is set in the Core USB Configuration register (GUSBCFG.HNPCap or GUSBCFG.SRPCap, respectively).	Host Only	RW[2]
18	A-Device Timeout Change (ADevTOUTChg) The core sets this bit to indicate that the A-device has timed out while waiting for the B-device to connect.	Host and Device	RW[3]
17	Host Negotiation Detected (HstNegDet) The core sets this bit when it detects a host negotiation request on the USB.	Host and Device	RW[4]
16:10	Reserved	Host and Device	R
9	Host Negotiation Success Status Change (HstNegSucStsChng) The core sets this bit on the success or failure of a USB host negotiation request. The application must read the Host Negotiation Success bit of the OTG Control and Status register (GOTGCTL.HstNegScs) to check for success or failure.	Host and Device	RW[5]
8	Session Request Success Status Change (SesReqSucStsChng) The core sets this bit on the success or failure of a session request. The application must read the Session Request Success bit in the OTG Control and Status register (GOTGCTL.SesReqScs) to check for success or failure.	Host and Device	RW[6]
7:3	Reserved	Host and Device	R
2	Session End Detected (SesEndDet) The core sets this bit when the utmisrp_bvalid signal is deasserted.	Device only	RW[7]
1:0	Reserved	Host and Device	R

Note:

[1]~[7]: This bits will operate with Self set , Write clear function.

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26.6.2.3 AHB Configuration Register (GAHBCFG,0x008)

	GAHBCFG																															Base + 0x008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								AHBSingle	NotiAllDmaWrit	RemMemSupp	Reserved												PTxFEmpLvl	NPTxFEmpLvl	Reserved	DMAEn	HBstLen				GlblIntrMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31:24	Reserved	Host and Device	R
23	AHB Single Support (AHBSingle) This bit when programmed supports Single transfers for the remaining data in a transfer when the DWC_otg core is operating in DMA mode. 1'b0: This is the default mode. When this bit is set to 1'b0, the remaining data in the transfer is sent using INCR burst size. 1'b1: When set to 1'b1, the remaining data in a transfer is sent using Single burst size. Note: if this feature is enabled, the AHB RETRY and SPLIT transfers still have INCR burst type. Enable this feature when the AHB Slave connected to the DWC_otg core does not support INCR burst (and when Split, and Retry transactions are not being used in the bus).	Host and Device	RW
22	Notify All Dma Write Transactions (NotiAllDmaWrit) This bit is programmed to enable the System DMA Done functionality for all the DMA write Transactions corresponding to the Channel/Endpoint. This bit is valid only when GAHBCFG.RemMemSupp is set to 1. GAHBCFG.NotiAllDmaWrit = 1 HS OTG core asserts int_dma_req for all the DMA write transactions on the AHB interface along with int_dma_done, chep_last_transact and chep_number signal informations. The core waits for sys_dma_done signal for all the DMA write transactions in order to complete the transfer of a particular Channel/Endpoint. GAHBCFG.NotiAllDmaWrit = 0 HS OTG core asserts int_dma_req signal only for the last transaction of DMA write transfer corresponding to a particular Channel/Endpoint. Similarly, the core waits for	Host and Device	RW

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	sys_dma_done signal only for that transaction of DMA write to complete the transfer of a particular Channel/Endpoint.		
21	Remote Memory Support (RemMemSupp) This bit is programmed to enable the functionality to wait for the system DMA Done Signal for the DMA Write Transfers. GAHBCFG.RemMemSupp=1 The int_dma_req output signal is asserted when HS OTG DMA starts write transfer to the external memory. When the core is done with the Transfers it asserts int_dma_done signal to flag the completion of DMA writes from HS OTG. The core then waits for sys_dma_done signal from the system to proceed further and complete the Data Transfer corresponding to a particular Channel/Endpoint. GAHBCFG.RemMemSupp=0 The int_dma_req and int_dma_done signals are not asserted and the core proceeds with the assertion of the XferComp interrupt as soon as the DMA write transfer is done at the HS OTG Core Boundary and it doesn't wait for the sys_dma_done signal to complete the DATA transfers.	Host and Device	RW
20:9	Reserved	Host and Device	R
8	Periodic TxFIFO Empty Level (PTxFEmpLvl) Indicates when the Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.PTxFEmp) is triggered. This bit is used only in Slave mode. 1'b0: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is half empty 1'b1: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is completely empty	Host only	RW
7	Non-Periodic TxFIFO Empty Level (NPTxFEmpLvl) This bit is used only in Slave mode. In host mode and with Shared FIFO with device mode, this bit indicates when the Non-Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.NPTxFEmp) is triggered. With dedicated FIFO in device mode, this bit indicates when IN endpoint Transmit FIFO empty interrupt (DIEPINTn.TxFEmp) is triggered. Host mode and with Shared FIFO with device mode: 1'b0: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is half empty 1'b1: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is completely empty Dedicated FIFO in device mode:	Host and Device	RW

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	1'b0: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is half empty 1'b1: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is completely empty		
6	Reserved	Host and Device	R
5	DMA Enable (DMAEn) 1'b0: Core operates in Slave mode 1'b1: Core operates in a DMA mode	Host and Device	RW
4:1	Burst Length/Type (HBstLen) This Bits is used in both External and Internal DMA modes. In External DMA mode, these bits appear on dma_burst[3:0] ports, which can be used by an external wrapper to interface the External DMA Controller interface to Synopsys DW_ahb_dmac or ARM PrimeCell. External DMA Mode — defines the DMA burst length in terms of 32-bit words: 4'b0000: 1 word 4'b0001: 4 words 4'b0010: 8 words 4'b0011: 16 words 4'b0100: 32 words 4'b0101: 64 words 4'b0110: 128 words 4'b0111: 256 words Others: Reserved Internal DMA Mode — AHB Master burst type: 4'b0000 Single 4'b0001 INCR 4'b0011 INCR4 4'b0101 INCR8 4'b0111 INCR16 Others: Reserved Slave Mode: Only single burst is supported.	Host and Device	RW
0	Global Interrupt Mask (GlblIntrMsk) The application uses this bit to mask or unmask the interrupt line assertion to itself. Irrespective of this bit's setting, the interrupt status registers are updated by the core. 1'b0: Mask the interrupt assertion to the application. 1'b1: Unmask the interrupt assertion to the application.	Host and Device	RW

26.6.2.4 USB Configuration Register (GUSBCFG,0x00C)

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	GUSBCFG																															Base + 0x00C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Txpacket	ForceDevMode	ForceHstMode	TxEndDelay	IC_USBTrafCtl	C_USBCap	ULIPPectDis	IndiPass	IndiComp	TermSelDLPulse	ULPIExtVbusIndicator	ULPIExtVbusDrv	ULPIClkSusM	ULPIAutoRes	ULPIFsLs	Otgl2CSel	PhyLPwrClkSel	Reserved	USBTrdTim				HNPCap	SRPCap	DDRSel	PHYSel	FSIntf	ULPI_UTMI_Sel	PHYIf	TOutCal		
RST	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	?	0	0	0

Bits	Description	Mode	R/W
31	Corrupt Tx packet(Txpacket) This bit is for debug purposes only. Never set this bit to 1.	Host and Device	W
30	Force Device Mode (ForceDevMode) Writing a 1 to this bit forces the core to device mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Device Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 µs is sufficient.	Host and Device	RW
29	Force Host Mode (ForceHstMode) Writing a 1 to this bit forces the core to host mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Host Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 µs is sufficient.	Host and Device	RW
28	Tx End Delay (TxEndDelay) Writing a 1 to this bit enables the TxEndDelay timers in the core as per the section 4.1.5 on Opmode of the USB 2.0 Transceiver Macrocell Interface (UTMI) version 1.05. 1'b0: Normal mode 1'b1: Introduce Tx end delay timers	Device Only	RW
27	IC_USB TrafficPullRemove Control (IC_USBTrafCtl) When this bit is set, pullup/pulldown resistors are detached from the USB during traffic signaling, per section 6.3.4 of the IC_USB specification. This bit is invalid.	Device	RW
26	IC_USB-Capable (IC_USBCap)	Host and Device	R

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	The application uses this bit to control the DWC_otg core's IC_USB capabilities. 1'b0: IC_USB PHY Interface is not selected. 1'b1: IC_USB PHY Interface is selected. This bit is set to 1'b0 and the bit is read only.		
25	ULPI Interface Protect Disable (ULIPPectDis) Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states STP and data. Any pull-ups or pull-downs employed by this feature can be disabled. 1'b0: Enables the interface protect circuit 1'b1: Disables the interface protect circuit This bit is reserved and read-only.	Host only	R
24	Indicator Pass Through(IndiPass) Controls wether the Complement Output is qualified with the Internal Vbus Valid comparator before being used in the Vbus State in the RX CMD. Please refer to the ULPI Specification for more detail. 1'b0: Complement Output signal is qualified with the Internal VbusValid comparator. 1'b1: Complement Output signal is not qualified with the Internal VbusValid comparator. This bit is reserved and read-only.	Host Only	R
23	Indicator Complement(IndiComp) Controls the PHY to invert the ExternalVbusIndicator input signal, generating the Complement Output. Please refer to the ULPI Specification for more detail 1'b0: PHY does not invert ExternalVbusIndicator signal 1'b1: PHY does invert ExternalVbusIndicator signal This bit is reserved and read-only.	Host Only	R
22	TermSel DLine Pulsing Selection (TermSelDLPulse) This bit selects utmi_termselect to drive data line pulse during SRP. 1'b0: Data line pulsing using utmi_txvalid (default). 1'b1: Data line pulsing using utmi_termsel.	Device Only	RW
21	ULPI External VBUS Indicator (ULPIExtVbusIndicator) This bit indicates to the ULPI PHY to use an external VBUS over-current indicator. 1'b0: PHY uses internal VBUS valid comparator. 1'b1: PHY uses external VBUS valid comparator.	Host Only	RW

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	This bit is invalid.		
20	ULPI External VBUS Drive (ULPIExtVbusDrv) This bit selects between internal or external supply to drive 5V on VBUS, in ULPI PHY. 1'b0: PHY drives VBUS using internal charge pump (default). 1'b1: PHY drives VBUS using external supply. This bit is invalid.	Host Only	RW
19	ULPI Clock SuspendM (ULPIClkSusM) This bit sets the ClockSuspendM bit in the Interface Control register on ULPI PHY. 1'b0: PHY powers down internal clock during suspend. 1'b1: PHY does not power down internal clock. This bit is invalid.	Host and Device	RW
18	ULPI Auto Resume (ULPIAutoRes) This bit sets the AutoResume bit in the Interface Control register on the ULPIPHY. 1'b0: PHY does not use AutoResume feature. 1'b1: PHY uses AutoResume feature. This bit is invalid.	Host and Device	RW
17	ULPI FS/LS Select (ULPIFsLs) The application uses this bit to select the FS/LS serial interface for the ULPI PHY. This bit is valid only when the FS serial transceiver is selected on the ULPI PHY. 1'b0: ULPI interface 1'b1: ULPI FS/LS serial interface	Host and Device	RW
16	UTMIFS or I2C Interface Select (OtgI2CSel) The application uses this bit to select the I2C interface. 1'b0: UTMI USB 1.1 Full-Speed interface for OTG signals 1'b1: I 2C interface for OTG signals This bit is writable only if I 2C and UTMIFS were specified for Enable I2C Interface	Host and Device	R/RW
15	PHY Low-Power Clock Select (PhyLPwrClkSel) Selects either 480-MHz or 48-MHz (low-power) PHY mode. In FS and LS modes, the PHY can usually operate on a 48-MHz clock to save power. 1'b0: 480-MHz Internal PLL clock 1'b1: 48-MHz External Clock In 480 MHz mode, the UTMI interface operates at either 60 or 30-MHz, depending upon whether 8- or 16-bit data width is selected. In 48-MHz mode, the UTMI interface operates at 48 MHz in FS and LS modes. This bit drives the utmi_fsls_low_power core output signal, and is valid only for UTMI+ PHYs.	Host and Device	RW

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14	Reserved	Host and Device	R
13:10	USB Turnaround Time (USBTrdTim) Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). This must be programmed to 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+. Note: The values above are calculated for the minimum AHB frequency of 30 MHz. USB turnaround time is critical for certification where long cables and 5-Hubs are used, so if you need the AHB to run at less than 30 MHz, and if USB turnaround time is not critical, these bits can be programmed to a larger value.	Device Only	RW
9	HNP-Capable (HNPCap) The application uses this bit to control the DWC_otg core's HNP capabilities. 1'b0: HNP capability is not enabled. 1'b1: HNP capability is enabled. This bit is writable only if an HNP mode was specified for Mode of operation in coreConsultant (parameter OTG_MODE). Otherwise, reads return 0. If HNP functionality is disabled by the software, the OTG signals on the PHY domain must be tied to the appropriate values.	Host and Device	R/RW
8	SRP-Capable (SRPCap) The application uses this bit to control the DWC_otg core SRP capabilities. If the core operates as a non-SRP-capable B-device, it cannot request the connected A-device (host) to activate VBUS and start a session. 1'b0: SRP capability is not enabled. 1'b1: SRP capability is enabled. If SRP functionality is disabled by the software, the OTG signals on the PHY domain must be tied to the appropriate values.	Host and Device	RW
7	ULPI DDR Select (DDRSel) The application uses this bit to select a Single Data Rate (SDR) or Double Data Rate (DDR) or ULPI interface. 1'b0: Single Data Rate ULPI Interface, with 8-bit-wide data bus 1'b1: Double Data Rate ULPI Interface, with 4-bit-wide data bus	Host and Device	RW

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	This bit is invalid.		
6	USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select (PHYSel) The application uses this bit to select either a high-speed UTMI+ or ULPI PHY, or a full-speed transceiver. 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY 1'b1: USB 1.1 full-speed serial transceiver This bit is always 0, with Read Only access.	Host and Device	R/RW
5	Full-Speed Serial Interface Select (FSIntf) The application uses this bit to select either a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. 1'b0: 6-pin unidirectional full-speed serial interface 1'b1: 3-pin bidirectional full-speed serial interface This bit is always 0, with Read Only access.	Host and Device	R/RW
4	ULPI or UTMI+ Select (ULPI_UTMI_Sel) The application uses this bit to select either a UTMI+ interface or ULPI Interface. 1'b0: UTMI+ Interface 1'b1: ULPI Interface This bit takes effect only if GUSBCFG.PHYSel = 1'b0.	Host and Device	R/RW
3	PHY Interface (PHYIf) The application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. When a ULPI PHY is chosen, this must be set to 8-bit mode. 1'b0: 8 bits 1'b1: 16 bits This bit is writable only if UTMI+ and ULPI were selected in coreConsultant configuration (parameter = 2). Otherwise, this bit returns the value for the power-on interface selected during configuration.	Host and Device	R/RW
2:0	HS/FS Timeout Calibration (TOutCal) The number of PHY clocks that the application programs in this Bits is added to the high-speed/full-speed interpacket timeout duration in the core to account for any additional delays introduced by the PHY. This can be required, because the delay introduced by the PHY in generating the line state condition can vary from one PHY to another. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this Bits based on the speed of enumeration. The number of bit times added per PHY clock are:	Host and Device	RW

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	High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times Using the HS as an example, if you set ToutCal to '001' you add one 30MHz PHY clock or 16 bit times. If you set ToutCal to '010' you add two 30MHz PHY clocks or 32 bit times, and so on. The 3 bits allow you to add up to 7 PHY clocks, and the number of bit times depend on the speed, and the PHY clock you are using.		

26.6.2.5 Reset Register (GRSTCTL,0x010)

	GRSTCTL																															Base + 0x010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AHBIdle	DMAReq	Reserved																			DMAReq					TxFFlsh	RxFFlsh	INTknQFlsh	FrmCntrRst	Reserved	CSftRst
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31	AHB Master Idle (AHBIdle) Indicates that the AHB Master State Machine is in the IDLE condition.	Host and Device	R
30	DMA Request Signal (DMAReq) Indicates that the DMA request is in progress. Used for debug.	Host and Device	R
29:11	Reserved	Host and Device	R
10:6	TxFIFO Number (TxFNum) This is the FIFO number that must be flushed using the TxFIFO Flush bit. This Bits must not be changed until the core clears the TxFIFO Flush bit. 5'h0: Non-periodic TxFIFO flush in Host mode Non-periodic TxFIFO flush in device mode when in shared FIFO operation	Host and Device	RW

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	Tx FIFO 0 flush in device mode when in dedicated FIFO mode 5'h1: Periodic TxFIFO flush in Host mode Periodic TxFIFO 1 flush in Device mode when in shared FIFO operation TXFIFO 1 flush in device mode when in dedicated FIFO mode 5'h2: Periodic TxFIFO 2 flush in Device mode when in shared FIFO operation TXFIFO 2 flush in device mode when in dedicated FIFO mode ... 5'hF: Periodic TxFIFO 15 flush in Device mode when in shared FIFO operation TXFIFO 15 flush in device mode when in dedicated FIFO mode 5'h10: Flush all the transmit FIFOs in device or host mode.		
5	TxFIFO Flush (TxFFlsh) This bit selectively flushes a single or all transmit FIFOs, but cannot do so if the core is in the midst of a transaction. The application must write this bit only after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. Verify using these registers: Read—NAK Effective Interrupt ensures the core is not reading from the FIFO. Write—GRSTCTL.AHBIdle ensures the core is not writing anything to the FIFO. Flushing is normally recommended when FIFOs are re-configured or when switching between Shared FIFO and Dedicated Transmit FIFO operation. FIFO flushing is also recommended during device endpoint disable. The application must wait until the core clears this bit before performing any operations. This bit takes eight clocks to clear, using the slower clock of phy_clk or hclk.	Host and Device	RW[1]
4	RxFIFO Flush (RxFFlsh) The application can flush the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a transaction.	Host and Device	RW[2]

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	The application must only write to this bit after checking that the core is neither reading from the RxFIFO nor writing to the RxFIFO. The application must wait until the bit is cleared before performing any other operations. This bit requires 8 clocks (slowest of PHY or AHB clock) to clear.		
3	IN Token Sequence Learning Queue Flush (INTknQFlsh) This bit is valid only if OTG_EN_DED_TX_FIFO = 0. The application writes this bit to flush the IN Token Sequence Learning Queue.	Device Only	RW[3]
2	Host Frame Counter Reset (FrmCntrRst) The application writes this bit to reset the (micro)frame number counter inside the core. When the (micro)frame counter is reset, the subsequent SOF sent out by the core has a (micro)frame number of 0.	Host Only	RW[4]
1	Reserved	Host and Device	R
0	Core Soft Reset (CSftRst) Resets the hclk and phy_clock domains as follows: Clears the interrupts and all the CSR registers except the following register bits: PCGCCTL.RstPdwnModule PCGCCTL.GateHclk PCGCCTL.PwrClmp GUSBCFG.DDRSel GUSBCFG.PHYSel GUSBCFG.FSIntf GUSBCFG.ULPI_UTMI_Sel GUSBCFG.PHYIf HCFG.FSLSPclkSel DCFG.DevSpd DCTL.SftDiscon GGPIO GUSBCFG.TxEndDelay GUSBCFG.TermSelDLPulse GUSBCFG.ULPIClkSusM GUSBCFG.ULPIAutoRes GUSBCFG.ULPIFsLs GPWRDN GADPCTL All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. Any transactions on the AHB Master are terminated as soon	Host and Device	RW[5]

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	as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. When Hibernation or ADP feature is enabled, the PMU module is not reset by the Core Soft Reset. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which can take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before doing any access to the PHY domain (synchronization delay). Software must also must check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation.		

***Notes*:**

[1]~[5]: This bits will operate with Write set , self clear function.

26.6.2.6 Interrupt Register (GINTSTS,0x014)

	GINTSTS																															Base + 0x014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WkUpInt	SessReqInt	DisconnInt	ConIDStsChng	LPM_Int	PTxFEmp	HChInt	PrtInt	ResetDet	FetSusp	incomplP	incomplSOIN	OEPInt	IEPInt	EPMis	RstrDoneInt	EOPF	ISOOutDrop	EnumDone	USBRst	USBSusp	ErlySusp	I2CINT	ULPICKINT	GOUTNakEff	GINNakEff	NPTxFEmp	RxFLvl	Sof	OTGInt	ModeMis	CurMod
RST	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Description	Mode	R/W
31	Resume/Remote Wakeup Detected Interrupt (WkUpInt) Wakeup Interrupt during Suspend(L2) or LPM(L1) state. During Suspend(L2): Device Mode - This interrupt is asserted only when Host Initiated Resume is detected on USB. Host Mode - This interrupt is asserted only when Device	Host and Device	RW[1]

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	Initiated Remote Wakeup is detected on USB. During LPM(L1): Device Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. Host Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB.		
30	Session Request/New Session Detected Interrupt (SessReqInt) In Host mode, this interrupt is asserted when a session request is detected from the device. In Host mode, this interrupt is asserted when a session request is detected from the device. In Device mode, this interrupt is asserted when the utmisrp_bvalid signal goes high. For more information on how to use this interrupt, see "FIFO RAM Allocation" in the Programming Guide.	Host and Device	RW[2]
29	Disconnect Detected Interrupt (DisconnInt) This interrupt is asserted when a device disconnect is detected.	Host Only	RW[3]
28	Connector ID Status Change (ConIDStsChng) This interrupt is asserted when there is a change in connector ID status.	Host and Device	RW[4]
27	LPM Transaction Received Interrupt (LPM_Int) Device Mode - This interrupt is asserted when the device receives an LPM transaction and responds with a non-ERRORed response. Host Mode - This interrupt is asserted when the device responds to an LPM transaction with a non-ERRORed response or when the host core has completed LPM transactions for the programmed number of times (GLPMCFG.RetryCnt). This Bits is valid only if the Core LPM Configuration register's LPM- Capable (LPMCap) Bits is set to 1 and the User HW Config3 register's OTG_ENABLE_LPM bit is set to 1.	Host and Device	RW[5]
26	Periodic TxFIFO Empty (PTxFEmp) This interrupt is asserted when the Periodic Transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the Periodic Request Queue. The half or completely empty status is determined by the Periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.PTxFEmpLvl).	Host Only	R
25	Host Channels Interrupt (HChInt)	Host Only	R

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	The core sets this bit to indicate that an interrupt is pending on one of the channels of the core (in Host mode). The application must read the Host All Channels Interrupt (HAINT) register to determine the exact number of the channel on which the interrupt occurred, and then read the corresponding Host Channel-n Interrupt (HCINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the HCINTn register to clear this bit.		
24	Host Port Interrupt (PrtInt) The core sets this bit to indicate a change in port status of one of the DWC_otg core ports in Host mode. The application must read the Host Port Control and Status (HPRT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the Host Port Control and Status register to clear this bit.	Host Only	R
23	Reset Detected Interrupt (ResetDet) The core sets this status bit in device mode when reset is detected on the USB in L2 Suspend state. This bit is valid only when the core is Device Mode and is operating in Partial Power-Down, or Clock Gating modes of Suspend. This bit is not valid when device is in Hibernation mode of Suspend.	Device Only	RW[6]
22	Data Fetch Suspended (FetSusp) This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data for IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm. For example, after detecting an endpoint mismatch, the application: Sets a global non-periodic IN NAK handshake Disables In endpoints Flushes the FIFO Determines the token sequence from the IN Token Sequence Learning Queue Re-enables the endpoints Clears the global non-periodic IN NAK handshake If the global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token is received: the core generates an "IN token received when	Device Only	RW[7]

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	FIFO empty" interrupt. The OTG then sends the host a NAK response. To avoid this scenario, the application can check the GINTSTS.FetSusp interrupt, which ensures that the FIFO is full before clearing a global NAK handshake. Alternatively, the application can mask the "IN token received when FIFO empty" interrupt when clearing a global IN NAK handshake.		
21	Incomplete Periodic Transfer (incomplP) In Host mode, the core sets this interrupt bit when there are incomplete periodic transactions still pending which are scheduled for the current microframe. Incomplete Isochronous OUT Transfer (incompISOOUT) The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.	Host only Device only	RW[8]
20	Incomplete Isochronous IN Transfer (incompISOIN) The core sets this interrupt to indicate that there is at least one isochronousIN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Note: This interrupt is not asserted in Scatter/Gather DMA mode.	Device only	RW[9]
19	OUT Endpoints Interrupt (OEPInt) The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-*n* Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit.	Device only	R
18	IN Endpoints Interrupt (IEPInt) The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN endpoint on which the interrupt occurred, and then read the	Device only	R

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	corresponding Device IN Endpoint-*n* Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.		
17	Endpoint Mismatch Interrupt (EPMis) Note: This interrupt is valid only in shared FIFO operation. ndicates that an IN token has been received for a non-periodic endpoint, but the data for another endpoint is present in the top of the Non-periodic Transmit FIFO and the IN endpoint mismatch count programmed by the application has expired.	Device only	RW[10]
16	Restore Done Interrupt (RstrDoneInt) The core sets this bit to indicate that the restore command after Hibernation was completed by the core. The core continues from Suspended state into the mode dictated by PCGCCTL.RestoreMode bits. This bit is valid only when Hibernation feature is enabled (OTG_EN_PWROPT=2)	Host and Device mode	RW[11]
15	End of Periodic Frame Interrupt (EOPF) Indicates that the period specified in the Periodic Frame Interval bits of the Device Configuration register (DCFG.PerFrInt) has been reached in the current microframe.	Device only	RW[12]
14	Isochronous OUT Packet Dropped Interrupt (ISOOutDrop) The core sets this bit when it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.	Device only	RW[13]
13	Enumeration Done (EnumDone) The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.	Device only	RW[14]
12	USB Reset (USBRst) The core sets this bit to indicate that a reset is detected on the USB.	Device only	RW[15]
11	USB Suspend (USBSusp) The core sets this bit to indicate that a suspend was detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time.	Device only	RW[16]
10	Early Suspend (ErlySusp) The core sets this bit to indicate that an Idle state has been detected on the USB for 3 ms.	Device only	RW[17]
9	I^2C Interrupt (I2CINT)	Host and	RW[18]

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	The core sets this interrupt when I^{2}C access is completed on the I ^{2}C interface. This Bits is used only if the I^{2}C interface was enabled. Otherwise, reads return 0.	Device	
8	ULPI Carkit Interrupt (ULPICKINT) This Bits is used only if the Carkit interface was enabled. Otherwise, reads return 0.	Host and Device	RW[19]
7	Global OUT NAK Effective (GOUTNakEff) Indicates that the Set Global OUT NAK bit in the Device Control register (DCTL.SGOUTNak), set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CGOUTNak).	Device only	R
6	Global IN Non-Periodic NAK Effective (GINNakEff) Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SGNPInNak), set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit set by the application. This bit can be cleared by clearing the Clear Global Non- periodic IN NAK bit in the Device Control register (DCTL.CGNPInNak). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.	Device only	R
5	Non-Periodic TxFIFO Empty (NPTxFEmp) This interrupt is valid only when OTG_EN_DED_TX_FIFO = 0. This interrupt is asserted when the Non-periodic TxFIFO is either half or completely empty, and there is space for at least one entry to be written to the Non-periodic Transmit Request Queue. The half or completely empty status is determined by the Non-periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl).	Host and Device	R
4	RxFIFO Non-Empty (RxFLvl) Indicates that there is at least one packet pending to be read from the RxFIFO.	Host and Device	R
3	Start of (micro)Frame (Sof) In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF (HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, in the core sets this bit to indicate that an SOF token has been received on the USB. The application can read the Device Status register to get the current (micro)frame number. This interrupt is seen only when the	Host and Device	RW[20]

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	core is operating at either HS or FS. Note: This register may return 1'b1 if read immediately after power on reset. If the register bit reads 1'b1 immediately after power on reset it does not indicate that an SOF has been sent (in case of host mode) or SOF has been received (in case of device mode). The read value of this interrupt is valid only after a valid connection between host and device is established. If the bit is set after power on reset the application can clear the bit.		
2	OTG Interrupt (OTGInt) The core sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit.	Host and Device	R
1	Mode Mismatch Interrupt (ModeMis) The core sets this bit when the application is trying to access: A Host mode register, when the core is operating in Device mode A Device mode register, when the core is operating in Host mode The register access is completed on the AHB with an OKAY response, but is ignored by the core internally and does not affect the operation of the core.	Host and Device	RW[21]
0	Current Mode of Operation (CurMod) Indicates the current mode. 1'b0: Device mode 1'b1: Host mode	Host and Device	R

Note:

[1]~[21]: This bits will operate with Write set , self clear function.

26.6.2.7 Interrupt Mask Register (GINTMSK,0x018)

	GINTMSK																															Base + 0x018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WkUpInt	SessReqInt	DisconnInt	ConIDStsChng	LPM_Int	PTxFEmp	HChInt	PrtInt	ResetDet	FetSusp	incomplP	incomplSOIN	OEPInt	IEPInt	EPMis	RstrDoneInt	EOPF	ISOOutDrop	EnumDone	USBRst	USBSusp	ErlySusp	I2CINT	ULPICKINT	GOUTNakEff	GINNakEff	NPTxFEmp	RxFLvl	Sof	OTGInt	ModeMis	CurMod
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	Mode	R/W
31	Resume/Remote Wakeup Detected Interrupt Mask (WkUpIntMsk)	Host and Device	RW
30	Session Request/New Session Detected Interrupt Mask (SessReqIntMsk)	Host and Device	RW
29	Disconnect Detected Interrupt Mask (DisconnIntMsk)	Host Only	RW
28	Connector ID Status Change Mask (ConIDStsChngMsk)	Host and Device	RW
27	LPM Transaction Received Interrupt Mask (LPM_IntMsk)	Host and Device	RW
26	Periodic TxFIFO Empty Mask (PTxFEmpMsk)	Host Only	RW
25	Host Channels Interrupt Mask (HChIntMsk)	Host Only	RW
24	Host Port Interrupt Mask (PrtIntMsk)	Host Only	RW
23	Reset Detected Interrupt Mask (ResetDetMsk)	Device Only	RW
22	Data Fetch Suspended Mask (FetSuspMsk)	Device Only	RW
21	Incomplete Periodic Transfer Mask (incomplPMsk) Incomplete Isochronous OUT Transfer Mask (incompISOOUTMsk)	Host only Device only	RW
20	Incomplete Isochronous IN Transfer Mask (incompISOINMsk) This bit is enabled only when device periodic endpoints are enabled in Dedicated TxFIFO mode.	Device only	RW
19	OUT Endpoints Interrupt Mask (OEPIntMsk)	Device only	RW
18	IN Endpoints Interrupt Mask (IEPIntMsk)	Device only	RW
17	Endpoint Mismatch Interrupt Mask (EPMisMsk)	Device only	RW
16	Restore Done Interrupt Mask (RstrDoneIntMsk) This Bits is valid only when Hibernation feature is enabled (OTG_EN_PWROPT=2).	Host and Device mode	RW
15	End of Periodic Frame Interrupt Mask (EOPFMsk)	Device only	RW
14	Isochronous OUT Packet Dropped Interrupt Mask (ISOOutDropMsk)	Device only	RW
13	Enumeration Done Mask (EnumDoneMsk)	Device only	RW
12	USB Reset Mask (USBRstMsk)	Device only	RW
11	USB Suspend Mask (USBSuspMsk)	Device only	RW
10	Early Suspend Mask (ErlySuspMsk)	Device only	RW
9	I^2C Interrupt Mask (I2CIntMsk)	Host and Device	RW
8	ULPI Carkit Interrupt Mask (ULPICKINTMsk) I^2C Carkit Interrupt Mask (I2CCKINTMsk)	Host and Device	RW
7	Global OUT NAK Effective Mask (GOUTNakEffMsk)	Device only	RW
6	Global Non-periodic IN NAK Effective Mask (GINNakEffMsk)	Device only	RW
5	Non-periodic TxFIFO Empty Mask (NPTxFEmpMsk)	Host and Device	RW
4	Receive FIFO Non-Empty Mask (RxFLvlMsk)	Host and Device	RW
3	Start of (micro)Frame Mask (SofMsk)	Host and Device	RW
2	OTG Interrupt Mask (OTGIntMsk)	Host and Device	RW

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1	Mode Mismatch Interrupt Mask (ModeMisMsk)	Host and Device	RW
0	Reserved	Host and Device	R

26.6.2.8 Receive Status Debug Read/Status Read and Pop Registers (GRXSTSR/GRXSTSP)

when host mode:

	GRXSTSR/GRXSTSP																															Base + 0x01C/Base + 0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											PktSts				DPID	BCnt												ChNum			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:21	Reserved	R
20:17	Packet Status (PktSts) 4'b0010: IN data packet received 4'b0011: IN transfer completed (triggers an interrupt) 4'b0101: Data toggle error (triggers an interrupt) 4'b0111: Channel halted (triggers an interrupt) Others: Reserved	R
16:15	Data PID (DPID) Indicates the Data PID of the received packet	R
14:4	Byte Count (BCnt) Indicates the byte count of the received IN data packet.	R
3:0	Channel Number (ChNum) Indicates the channel number to which the current received packet belongs.	R

when device mode:

	GRXSTSR/GRXSTSP																															Base + 0x01C/Base + 0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							FN				PktSts				DPID	BCnt												EPNum			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	R/W
31:25	Reserved	R
24:21	Frame Number (FN) This is the least significant 4 bits of the (micro)frame number in which the packet is received on the USB. This Bits is supported only when isochronous OUT endpoints are supported.	R
20:17	Packet Status (PktSts) Indicates the status of the received packet 4'b0001: Global OUT NAK (triggers an interrupt) 4'b0010: OUT data packet received 4'b0011: OUT transfer completed (triggers an interrupt) 4'b0100: SETUP transaction completed (triggers an interrupt) 4'b0110: SETUP data packet received Others: Reserved	R
16:15	Data PID (DPID) Indicates the Data PID of the received OUT data packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA	R
14:4	Byte Count (BCnt) Indicates the byte count of the received data packet.	R
3:0	Endpoint Number (EPNum) Indicates the endpoint number to which the current received packet belongs.	R

26.6.2.9 Receive FIFO Size Register (GRXFSIZ,0x024)

	GRXFSIZ																															Base + 0x024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RxFDep															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Reserved	R
15:0	RxFIFO Depth (RxFDep) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648.	RW

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26.6.2.10 Non-Periodic Transmit FIFO Size Register (GNPTXFSIZ,0x028)

	GNPTXFSIZ																															Base + 0x028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NPTxFDep																NPTxFStAddr															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Non-periodic TxFIFO Depth (NPTxFDep) For host mode, this Bits is always valid. For Device mode, this Bits is invalid. This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648	R/RW
15:0	Non-periodic Transmit RAM Start Address (NPTxFStAddr) For host mode, this Bits is always valid. This Bits contains the memory start address for Non-periodic Transmit FIFO RAM. The application can write a new value in this Bits. Programmed values must not exceed the power-on value set	RW

26.6.2.11 Non-Periodic Transmit FIFO/Queue Status Register (GNPTXSTS,0x02C)

	GNPTXSTS																															Base + 0x02C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NPTxQTop								NPTxQSpcAvail								NPTxFSpcAvail															
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:24	Top of the Non-periodic Transmit Request Queue (NPTxQTop) Entry in the Non-periodic Tx Request Queue that is currently being processed by the MAC. Bits [30:27]: Channel/endpoint number Bits [26:25]: 2'b00: IN/OUT token 2'b01: Zero-length transmit packet (device IN/host OUT) 2'b10: PING/CSPLIT token	R

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	2'b11: Channel halt command Bit [24]: Terminate (last entry for selected channel/endpoint)	
23:16	Non-periodic Transmit Request Queue Space Available (NPTxQSpcAvail) Indicates the amount of free space available in the Non-periodic Transmit Request Queue. This queue holds both IN and OUT requests in Host mode. Device mode has only IN requests. 8'h0: Non-periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n : n locations available (0⩽n⩽8) Others: Reserved	R
15:0	Non-periodic TxFIFO Space Avail (NPTxFSpcAvail) Indicates the amount of free space available in the Non-periodic TxFIFO. Values are in terms of 32-bit words. 16'h0: Non-periodic TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'h*n*: *n* words available (where 0⩽n⩽32,768) 16'h8000: 32,768 words available Others: Reserved	R

26.6.2.12 User HW Config1 Register (GHWCFG1,0x044)

	GHWCFG1																															Base + 0x044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	epdir																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	Endpoint Direction (epdir) This 32-bit Bits uses two bits per endpoint to determine the endpoint direction. Endpoint Bits [31:30]: Endpoint 15 direction Bits [29:28]: Endpoint 14 direction ... Bits [3:2]: Endpoint 1 direction Bits[1:0]: Endpoint 0 direction (always BIDIR) Direction 2'b00: BIDIR (IN and OUT) endpoint	R

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	2'b01: IN endpoint 2'b10: OUT endpoint 2'b11: Reserved This Bits is configured using "Name: OTG_EP_DIR_1(n)".	

26.6.2.13 User HW Config2 Register (GHWCFG2,0x048)

	GHWCFG2																															Base + 0x048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	otgenicusb	TknQDepth					PTxQDepth		NPTxQDepth		Reserved	MultiProcIntrpt	DynFifoSizing	PerioSupport	NumHstChnl				NumDevEps				FSPhyType		HSPhyType		SingPnt	OtgArch		OtgMode		
RST	?	?	?	?	?	?	?	?	?	?	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31	OTG_ENABLE_IC_USB(otgenicusb) IC_USB mode specified for mode of operation (parameter OTG_ENABLE _IC_USB) in coreConsultant. To choose IC_USB_MODE, both OTG_FSPHY_INTERFACE and OTG_ENABLE_IC_USB must be 1.	R
30:26	Device Mode IN Token Sequence Learning Queue Depth (TknQDepth) Range: 0-30 This Bits is configured using "Name: OTG_TOKEN_QUEUE_DEPTH".	R
25:24	Host Mode Periodic Request Queue Depth (PTxQDepth) 2'b00: 2 2'b01: 4 2'b10: 8 2'b11: 16 This Bits is configured using parameter "Name: OTG_PERIO_TX_QUEUE_DEPTH"	R
23:22	Non-periodic Request Queue Depth (NPTxQDepth) 2'b00: 2 2'b01: 4 2'b10: 8 Others: Reserved This Bits is configured using parameter "Name: OTG_NPERIO_TX_QUEUE_DEPTH".	R
21	Reserved	R
20	Multi Processor Interrupt Enabled (MultiProcIntrpt) 1'b0: No	R

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	1'b1: Yes This Bits is configured using parameter "Name: OTG_MULTI_PROC_INTRPT".	
19	Dynamic FIFO Sizing Enabled (DynFifoSizing) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_DFIFO_DYNAMIC".	R
18	Periodic OUT Channels Supported in Host Mode (PerioSupport) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_EN_PERIO_HOST".	R
17:14	Number of Host Channels (NumHstChnl) Indicates the number of host channels supported by the core in Host mode. The range of this Bits is 0-15: 0 specifies 1 channel, 15 specifies 16 channels. This Bits is configured using parameter "Name: OTG_NUM_HOST_CHAN".	R
13:10	Number of Device Endpoints (NumDevEps) Indicates the number of device endpoints supported by the core in Device mode in addition to control endpoint 0. The range of this Bits is 1-15. This Bits is configured using parameter "Name: OTG_NUM_EPS".	R
9:8	Full-Speed PHY Interface Type (FSPhyType) 2'b00: Full-speed interface not supported 2'b01: Dedicated full-speed interface 2'b10: FS pins shared with UTMI+ pins 2'b11: FS pins shared with ULPI pins This Bits is configured using parameter "Name: OTG_FSPHY_INTERFACE".	R
7:6	High-Speed PHY Interface Type (HSPhyType) 2'b00: High-Speed interface not supported 2'b01: UTMI+ 2'b10: ULPI 2'b11: UTMI+and ULPI This Bits is configured using parameter "Name: OTG_HSPHY_INTERFACE".	R
5	Point-to-Point (SingPnt) 1'b0: Multi-point application (hub and split support) 1'b1: Single-point application (no hub and no split support) This Bits is configured using parameter "Name: OTG_SINGLE_POINT".	R
4:3	Architecture (OtgArch) 2'b00: Slave-Only 2'b01: External DMA 2'b10: Internal DMA Others: Reserved This Bits is configured using parameter "Name: OTG_ARCHITECTURE".	R
2:0	Mode of Operation (OtgMode) 3'b000: HNP- and SRP-Capable OTG (Host and Device) 3'b001: SRP-Capable OTG (Host and Device)	R

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	3'b010: Non-HNP and Non-SRP Capable OTG (Host and Device) 3'b011: SRP-Capable Device 3'b100: Non-OTG Device 3'b101: SRP-Capable Host 3'b110: Non-OTG Host Others: Reserved This Bits is configured using parameter "Name: OTG_MODE".	

26.6.2.14 User HW Config3 Register (GHWCFG3,0x04C)

																																Base + 0x04C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DfifoDepth																OTG_ENABLE_LPM	OTG_BC_SUPPORT	OTG_ENABLE_HSIC	OTG_ADP_SUPPORT	RstType	OptFeature	VndctlSupt	I2CIntSel	OtgEn	PktSizeWidth			XferSizeWidth			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	DFIFO Depth (DfifoDepth minus EP_LOC_CNT) This value is in terms of 32-bit words. Minimum value is 32 Maximum value is 32,768 This Bits is configured using parameter "Name: OTG_DFIFO_DEPTH" and EP_LOC_CNT. For more information on EP_LOC_CNT, see "Endpoint Information Controller (EPINFO_CTL)".	R
15	OTG_ENABLE_LPM LPM mode specified for Mode of Operation (parameter OTG_ENABLE_LPM) in coreConsultant configuration.	R
14	OTG_BC_SUPPORT This bit indicates the HS OTG controller support for Battery Charger. 0 - No Battery Charger Support 1 - Battery Charger support present.	R
13	OTG_ENABLE_HSIC HSIC mode specified for Mode of Operation in coreConsultant configuration (parameter OTG_ENABLE_HSIC). Value Range: 0-1 1: HSIC-capable with shared UTMI PHY interface 0: Non-HSIC-capable Parameter Name: OTG_ENABLE_HSIC	R

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	Dependencies: OTG_HSPHY_INTERFACE Default: Non-HSIC-capable	
12	OTG_ADP_SUPPORT This bit indicates whether ADP logic is present within or external to the HS OTG controller 0 - No ADP logic present with HS OTG controller 1- ADP logic is present along with HS OTG controller.	R
11	Reset Style for Clocked always Blocks in RTL (RstType) 1'b0: Asynchronous reset is used in the core 1'b1: Synchronous reset is used in the core This Bits is configured using parameter "Name: OTG_SYNC_RESET_TYPE".	R
10	Optional Features Removed (OptFeature) Indicates whether the User ID register, GPIO interface ports, and SOF toggle and counter ports were removed for gate count optimization by enabling Remove Optional Features? during coreConsultant configuration. 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_RM_OPT_FEATURES".	R
9	Vendor Control Interface Support (VndctlSupt) 1'b0: Vendor Control Interface is not available on the core. 1'b1: Vendor Control Interface is available. This Bits is configured using parameter "Name: OTG_VENDOR_CTL_INTERFACE".	R
8	I^2C Selection (I2CIntSel) 1'b0: I 2C Interface is not available on the core. 1'b1: I 2C Interface is available on the core. This Bits is configured using parameter "Name: OTG_I2C_INTERFACE".	R
7	OTG Function Enabled (OtgEn) The application uses this bit to indicate the DWC_otg core's OTG capabilities. 1'b0: Not OTG capable 1'b1: OTG Capable This Bits is configured using parameter "Name: OTG_MODE".	R
6:4	Width of Packet Size Counters (PktSizeWidth) 3'b000: 4 bits 3'b001: 5 bits 3'b010: 6 bits 3'b011: 7 bits 3'b100: 8 bits 3'b101: 9 bits 3'b110: 10 bits Others: Reserved This Bits is configured using parameter "Name: OTG_PACKET_COUNT_WIDTH".	R

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3:0	Width of Transfer Size Counters (XferSizeWidth) 4'b0000: 11 bits 4'b0001: 12 bits ... 4'b1000: 19 bits Others: Reserved This Bits is configured using parameter "Name: OTG_TRANS_COUNT_WIDTH".	R

26.6.2.15 User HW Config4 Register (GHWCFG4,0x050)

	GHWCFG4																															Base + 0x050
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SGDMA	SGDMACFG	INEps				DedFifoMode	SessEndFltr	BValidFltr	AValidFltr	VBusValidFltr	IddgFltr	NumCtlEps				PhyDataWidth		Reserved								AhbFreq	enPartPwrDn	NumDevPerioEps			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	?	?	?	?	?	?

Bits	Description	R/W
31	Scatter/Gather DMA(SGDMA) 1'b1: Dynamic configuration This Bits is configured using parameter "Name: OTG_EN_DESC_DMA" .	R
30	Scatter/Gather DMA configuration(SGDMACFG) 1'b0: Non-Scatter/Gather DMA configuration 1'b1: Scatter/Gather DMA configuration This Bits is configured using parameter "Name: OTG_EN_DESC_DMA".	R
29:26	Number of Device Mode IN Endpoints Including Control Endpoints (INEps) Range 0 -15 0:1 IN Endpoint 1:2 IN Endpoints .... 15:16 IN Endpoints This Bits is configured using parameter "Name: OTG_NUM_IN_EPS".	R
25	Enable Dedicated Transmit FIFO for device IN Endpoints (DedFifoMode) 1'b0: Dedicated Transmit FIFO Operation not enabled. 1'b1: Dedicated Transmit FIFO Operation enabled. This Bits is configured using parameter "Name: OTG_EN_DED_TX_FIFO".	R
24	session_end Filter Enabled (SessEndFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name:	R

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	OTG_EN_SESSIONEND_FILTER"	
23	"b_valid" Filter Enabled (BValidFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_B_VALID_FILTER".	R
22	"a_valid" Filter Enabled (AValidFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_A_VALID_FILTER".	R
21	"vbus_valid" Filter Enabled (VBusValidFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_VBUSVALID_FILTER".	R
20	"iddig" Filter Enable (IddgFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_IDDIG_FILTER".	R
19:16	Number of Device Mode Control Endpoints in Addition to Endpoint 0 (NumCtlEps) Range: 0-15 This Bits is configured using parameter "Name: OTG_NUM_CRL_EPS".	R
15:14	UTMI+ PHY/ULPI-to-Internal UTMI+ Wrapper Data Width (PhyDataWidth) When a ULPI PHY is used, an internal wrapper converts ULPI to UTMI+. 2'b00: 8 bits 2'b01: 16 bits 2'b10: 8/16 bits, software selectable Others: Reserved This Bits is configured using parameter "Name: OTG_HSPHY_DWIDTH".	R
13:6	Reserved	R
6	Enable Hibernation 1'b0: Hibernation feature not enabled 1'b1: Hibernation feature enabled This Bits is configured using parameter "Name: OTG_EN_PWROPT".	R
5	Minimum AHB Frequency Less Than 60 MHz (AhbFreq) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_MIN_AHB_FREQ_LESSTHAN_60".	R
4	Enable Partial Power Down(enPartPwrDn) 1'b0: Partial Power Down Not Enabled 1'b1: Partial Power Down Enabled This Bits is configured using parameter "Name: OTG_EN_PWROPT".	R

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3:0	Number of Device Mode Periodic IN Endpoints (NumDevPerioEps) Range: 0-15 This Bits is configured using parameter "Name: OTG_NUM_PERIO_EPS".	R

26.6.2.16 DFIFO Software Config Register (GDFIFOCFG,0x05C)

	GDFIFOCFG																															Base + 0x05C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPInfoBaseAddr																GDFIFOCfg															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	Mode	R/W
31:16	EPInfoBaseAddr This Bits provides the start address of the EP info controller.	Host and Device	RW
15:0	GDFIFOCfg This Bits is for dynamic programming of the DFIFO Size. This value takes effect only when the application programs a non zero value to this register. The value programmed must conform to the guidelines described in "FIFO RAM Allocation" in the Programming Guide. The DWC_otg core does not have any corrective logic if the FIFO sizes are programmed incorrectly.	Host and Device	RW

26.6.2.17 Host Periodic Transmit FIFO Size Register (HPTXFSIZ,0x100)

	HPTXFSIZ																															Base + 0x100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTxFSize																PTxFStAddr															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Host Periodic TxFIFO Depth (PTxFSize) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648	RW

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15:0	Host Periodic TxFIFO Start Address (PTxFStAddr) The power-on reset value of this register is the sum of the Largest Rx Data FIFO Depth and Largest Non-periodic Tx Data FIFO Depth specified .These parameters are: In shared FIFO operation:- OTG_RX_DFIFO_DEPTH(3648) + OTG_TX_NPERIO_DFIFO_DEPTH(1024) In dedicated FIFO mode:- OTG_RX_DFIFO_DEPTH(3648) + OTG_TX_HNPERIO_DFIFO_DEPTH(3648)	R/RW

26.6.2.18 Device IN Endpoint Transmit FIFO Size Register: (DIEPTXFn,0x104+(FIFO_num - 1)*0x04)

	DIEPTXFn																Base + 0x104+(FIFO_num - 1)*0x4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INEPnTxFDep																INEPnTxFStAddr															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648	RW
15:0	IN Endpoint FIFO*n* Transmit RAM Start Address (INEPnTxFStAddr) This Bits contains the memory start address for IN endpoint Transmit FIFOn (0 < n <= 15). The power-on reset value of this register is calculated according to the following formula: OTG_RX_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'x' (where x = 0 to n - 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C - 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFIFO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1.	R/RW

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26.6.2.19 Host Configuration Register (HCFG,0x400)

	HCFG																															Base + 0x400
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ModeChTimEn	Reserved				PerSchedEna	FrListEn		DescDMA	Reserved							ResValid								Ena32KHzS	Reserved				FSLSSupp	FSLSPclkSel	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Mode Change Ready Timer Enable (ModeChTimEn) This bit is used to enable or disable the host core to wait for 200 PHY clock cycles at the end of Resume to change the opmode signal to the PHY to 00 after Suspend or LPM. 1'b0: The Host core waits for either 200 PHY clock cycles or a linestate of SE0 at the end of resume to change the opmode from 2'b10 to 2'b00. 1'b1: The Host core waits only for a linestate of SE0 at the end of resume to change the opmode from 2'b10 to 2'b00.	RW
30:27	Reserved	R
26	Enable Periodic Scheduling (PerSchedEna) Applicable in Scatter/Gather DMA mode only. Enables periodic scheduling within the core. Initially, the bit is reset. The core will not process any periodic channels. As soon as this bit is set, the core will get ready to start scheduling periodic channels. In non Scatter/Gather DMA mode, this bit is reserved.	RW
25:24	Frame List Entries (FrListEn). The value in the register specifies the number of entries in the Frame list. This Bits is valid only in Scatter/Gather DMA mode. 2'b00: 8 Entries 2'b01:16 Entries 2'b10: 32 Entries 2'b11: 64 Entries In modes other than Scatter/Gather DMA mode, these bits are reserved.	RW
23	Enable Scatter/gather DMA in Host mode (DescDMA) When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming: GAHBCFG.DMAEn=0, HCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0, HCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1, HCFG.DescDMA=0 => Buffered DMA mode GAHBCFG.DMAEn=1, HCFG.DescDMA=1 => Scatter/Gather DMA mode	RW

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	In non Scatter/Gather DMA mode, this bit is reserved.	
22:16	Reserved	RW
15:8	Resume Validation Period (ResValid) This Bits is effective only when HCFG.Ena32KHzS is set. It controls the resume period when the core resumes from suspend. The core counts the ResValid number of clock cycles to detect a valid resume when this is set.	RW
7	Enable 32-KHz Suspend Mode (Ena32KHzS) This bit can only be set if the USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero. When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a suspend.	RW
6:3	Reserved	R
2	FS- and LS-Only Support (FSLSSupp) The application uses this bit to control the core's enumeration speed. Using this bit, the application can make the core enumerate as a FS host, even if the connected device supports HS traffic. Do not make changes to this Bits after initial programming. 1'b0: HS/FS/LS, based on the maximum speed supported by the connected device 1'b1: FS/LS-only, even if the connected device can support HS	RW
1:0	FS/LS PHY Clock Select (FSLSPclkSel) When the core is in FS Host mode 2'b00: Internal PHY clock is running at 30/60 MHZ (For UTMI+/ULPI PHY Interfaces) 2'b01: Internal PHY clock is running at 48MHZ (For 1.1 FS transceiver Interface) Others: Reserved When the core is in LS Host mode 2'b00: Internal PHY clock is running at 30/60 MHZ (For UTMI+/ULPI PHY Interfaces) 2'b10: Internal PHY clock is running at 6 MHZ and the external clock is running at 48MHZ. When you select a 6 MHz clock during LS Mode, you must do a soft reset (for 1.1 FS transceiver Interface) Others: Reserved Notes: When Core in FS mode, the internal and external clocks have the same frequency. When Core in LS mode, If FSLSPclkSel = 2'b00: Internal and external clocks have the same frequency If FSLSPclkSel = 2'b10: Internal clock is divided by eight version of external 48 MHz clock (utmifs_clk).	RW

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26.6.2.20 Host Frame Interval Register (HFIR,0x404)

	HFIR																															Base + 0x404
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															HFIRRldCtrl	FrInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	0	0

Bits	Description	R/W
31:17	Reserved	R
16	Reload Control (HFIRRldCtrl) This bit allows dynamic reloading of the HFIR register during runtime. 1'b0: The HFIR cannot be reloaded dynamically 1'b1: the HFIR can be dynamically reloaded during runtime. This bit needs to be programmed during initial configuration and its value must not be changed during runtime.	RW
15:0	Frame Interval (FrInt) The value that the application programs to this Bits specifies the interval between two consecutive SOFs (FS) or micro-SOFs (HS) or Keep-Alive tokens (LS). This Bits contains the number of PHY clocks that constitute the required frame interval. The default value set in this Bits for a FS operation when the PHY clock frequency is 60 MHz. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been set. If no value is programmed, the core calculates the value based on the PHY clock specified in the FS/LS PHY Clock Select Bits of the Host Configuration register (HCFG.FSLSPclkSel). 125 μs * (PHY clock frequency for HS) 1 ms * (PHY clock frequency for FS/LS)	RW

26.6.2.21 Host Frame Number/Frame Time Remaining Register (HFNUM,0x408)

	HFNUM																															Base + 0x408
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FrRem																FrNum															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Bits	Description	R/W
31:16	Frame Time Remaining (FrRem) Indicates the amount of time remaining in the current microframe (HS) or frame (FS/LS), in terms of PHY clocks. This Bits decrements on each PHY clock. When it reaches zero, this Bits is reloaded with the value in the Frame Interval register and a new SOF is transmitted on the USB.	R
15:0	Frame Number (FrNum) This Bits increments when a new SOF is transmitted on the USB, and is reset to 0 when it reaches 16'h3FFF.	R

26.6.2.22 Host Periodic Transmit FIFO/Queue Status Register (HPTXSTS,0x410)

	HPTXSTS																															Base + 0x410
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTxQTop								PTxQSpcAvail								PTxFSpcAvail															
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:24	Top of the Periodic Transmit Request Queue (PTxQTop) This indicates the entry in the Periodic Tx Request Queue that is currently being processes by the MAC. This register is used for debugging. Bit [31]: Odd/Even (micro)frame 1'b0: send in even (micro)frame 1'b1: send in odd (micro)frame Bits [30:27]: Channel/endpoint number Bits [26:25]: Type 2'b00: IN/OUT 2'b01: Zero-length packet 2'b10: CSPLIT 2'b11: Disable channel command Bit [24]: Terminate (last entry for the selected channel/endpoint)	R
23:16	Periodic Transmit Request Queue Space Available (PTxQSpcAvail) Indicates the number of free locations available to be written in the Periodic Transmit Request Queue. This queue holds both IN and OUT requests. 8'h0: Periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n : n locations available (0 ≤n ≤16)	R

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	Others: Reserved	
15:0	Periodic Transmit Data FIFO Space Available (PTxFSpcAvail) Indicates the number of free locations available to be written to in the Periodic TxFIFO. Values are in terms of 32-bit words 16'h0: Periodic TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0 ≤n ≤32,768) 16'h8000: 32,768 words available Others: Reserved	R

26.6.2.23 Host All Channels Interrupt Register (HAINT,0x414)

	HAINT																															Base + 0x414
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HAINT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved	R
15:0	Channel Interrupts (HAINT) One bit per channel: Bit 0 for Channel 0, bit 15 for Channel 15	R

26.6.2.24 Host All Channels Interrupt Mask Register (HAINTMSK,0x418)

	HAINTMSK																															Base + 0x418
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HAINTMsk															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved	R
15:0	Channel Interrupt Mask (HAINTMsk) One bit per channel: Bit 0 for channel 0, bit 15 for channel 15	RW

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26.6.2.25 Host Port Control and Status Register (HPRT,0x440)

	HPRT																															Base + 0x440
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													PrtSpd			PrtTstCtl			PrtPwr	PrtLnSts		Reserved	PrtRst	PrtSusp	PrtRes	PrtOvrCurrChng	PrtOvrCurrAct	PrtEnChng	PrtEna	PrtConnDet	PrtConnSts
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:19	Reserved	R
18:17	Port Speed (PrtSpd) Indicates the speed of the device attached to this port. 2'b00: High speed 2'b01: Full speed 2'b10: Low speed 2'b11: Reserved	R
16:13	Port Test Control (PrtTstCtl) The application writes a nonzero value to this Bits to put the port into a Test mode, and the corresponding pattern is signaled on the port. 4'b0000: Test mode disabled 4'b0001: Test_J mode 4'b0010: Test_K mode 4'b0011: Test_SE0_NAK mode 4'b0100: Test_Packet mode 4'b0101: Test_Force_Enable Others: Reserved For more information on moving the DWC_otg host core into test mode, see "Moving the Host Core to Test Mode" on page 89.	RW
12	Port Power (PrtPwr) The application uses this Bits to control power to this port (write 1'b1 to set to 1'b1 and write 1'b0 to set to 1'b0), and the core can clear this bit on an over current condition. 1'b0: Power off 1'b1: Power on	R
11:10	Port Line Status (PrtLnSts) Indicates the current logic level USB data lines Bit [10]: Logic level of D+ Bit [11]: Logic level of D-	R
9	Reserved	R

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8	Port Reset (PrtRst) When the application sets this bit, a reset sequence is started on this port. The application must time the reset period and clear this bit after the reset sequence is complete. 1'b0: Port not in reset 1'b1: Port in reset To start a reset on the port, the application must leave this bit set for at least the minimum duration mentioned below, as specified in the USB 2.0 specification, Section 7.1.7.5. The application can leave it set for another 10 ms in addition to the required minimum duration, before clearing the bit, even though there is no maximum limit set by the USB standard. High speed: 50 ms Full speed/Low speed: 10 ms	RW
7	Port Suspend (PrtSusp) The application sets this bit to put this port in Suspend mode. The core only stops sending SOFs when this is set. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts the suspend input pin of the PHY. The read value of this bit reflects the current suspend status of the port. This bit is cleared by the core after a remote wakeup signal is detected or the application sets the Port Reset bit or Port Resume bit in this register or the Resume/Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.WkUpInt or GINTSTS.DisconnInt, respectively). 1'b0: Port not in Suspend mode 1'b1: Port in Suspend mode	RW[1]
6	Port Resume (PrtRes) The application sets this bit to drive resume signaling on the port. The core continues to drive the resume signal until the application clears this bit. If the core detects a USB remote wakeup sequence, as indicated by the Port Resume/Remote Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.WkUpInt), the core starts driving resume signaling without application intervention and clears this bit when it detects a disconnect condition. The read value of this bit indicates whether the core is currently driving resume signaling. 1'b0: No resume driven 1'b1: Resume driven When LPM is enabled and the core is in the L1 (Sleep) state, setting this bit results in the following behavior: The core continues to drive the resume signal until a pre-determined time specified in the GLPMCFG.HIRD_Thres[3:0] Bits.	RW[2]

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	If the core detects a USB remote wakeup sequence, as indicated by the Port L1 Resume/Remote L1 Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.L1WkUpInt), the core starts driving resume signaling without application intervention and clears this bit at the end of the resume. The read value of this bit indicates whether the core is currently driving resume signaling. 1'b0: No resume driven 1'b1: Resume driven	
5	Port Overcurrent Change (PrtOvrCurrChng) The core sets this bit when the status of the Port Overcurrent Active bit (bit 4) in this register changes.	RW[3]
4	Port Overcurrent Active (PrtOvrCurrAct) Indicates the overcurrent condition of the port. 1'b0: No overcurrent condition 1'b1: Overcurrent condition	R
3	Port Enable/Disable Change (PrtEnChng) The core sets this bit when the status of the Port Enable bit [2] of this register changes.	RW[4]
2	Port Enable (PrtEna) A port is enabled only by the core after a reset sequence, and is disabled by an overcurrent condition, a disconnect condition, or by the application clearing this bit. The application cannot set this bit by a register write. It can only clear it to disable the port. This bit does not trigger any interrupt to the application. 1'b0: Port disabled 1'b1: Port enabled	RW[5]
1	Port Connect Detected (PrtConnDet) The core sets this bit when a device connection is detected to trigger an interrupt to the application using the Host Port Interrupt bit of the Core Interrupt register (GINTSTS.PrtInt). The application must write a 1 to this bit to clear the interrupt.	RW[6]
0	Port Connect Status (PrtConnSts) 0: No device is attached to the port. 1: A device is attached to the port.	R

Note:

[1],[2]: This bits will operate with Write set , self clear function.

[3],[4],[6]: This bits will operate with Self set , Write clear function.

[5]: This bits will operate with Write clear or read clear function.

26.6.2.26 Host Channel-n Characteristics Register (HCCHARn,0x500+n*0x20)

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	HCCHARn																															Base + 0x500+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ChEna	ChDis	OddFrm	DevAddr	DevAddr						EC		EPType		LSpdDev	Reserved	EPDir	EPNum				MPS										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Channel Enable (ChEna) When Scatter/Gather mode is enabled 1'b0: Indicates that the descriptor structure is not yet ready. 1'b1: Indicates that the descriptor structure and data buffer with data is setup and this channel can access the descriptor. When Scatter/Gather mode is disabled This Bits is set by the application and cleared by the OTG host. 1'b0: Channel disabled 1'b1: Channel enabled	RW[1]
30	Channel Disable (ChDis) The application sets this bit to stop transmitting/receiving data on a channel, even before the transfer for that channel is complete. The application must wait for the Channel Disabled interrupt before treating the channel as disabled.	RW[2]
29	Odd Frame (OddFrm) This Bits is set (reset) by the application to indicate that the OTG host must perform a transfer in an odd (micro)frame. This Bits is applicable for only periodic (isochronous and interrupt) transactions. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame This Bits is not applicable for Scatter/Gather DMA mode and need not be programmed by the application and is ignored by the core.	RW
28:22	Device Address (DevAddr) This Bits selects the specific device serving as the data source or sink.	RW
21:20	Multi Count (MC) / Error Count (EC) When the Split Enable bit of the Host Channel-n Split Control register (HCSPLTn.SpltEna) is reset (1'b0), this Bits indicates to the host the number of transactions that must be executed per microframe for this periodic endpoint. For non periodic transfers, this Bits is used only in DMA mode, and specifies the number packets to be fetched for this channel before the internal DMA engine changes aubitration. 2'b00: Reserved This Bits yields undefined results. 2'b01: 1 transaction	RW

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	2'b10: 2 transactions to be issued for this endpoint per microframe 2'b11: 3 transactions to be issued for this endpoint per microframe When HCSPLTn.SpltEna is set (1'b1), this Bits indicates the number of immediate retries to be performed for a periodic split transactions on transaction errors. This Bits must be set to at least 2'b01.	
19:18	Endpoint Type (EPType) Indicates the transfer type selected. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt	RW
17	Low-Speed Device (LSpdDev) This Bits is set by the application to indicate that this channel is communicating to a low-speed device. The application must program this bit when a low speed device is connected to the host through an FS HUB. The HS OTG Host core uses this Bits to drive the XCVR_SELECT signal to 2'b11 while communicating to the LS Device through the FS hub. **Note:** In a peer to peer setup, the HS OTG Host core ignores this bit even if it is set by the application software.	RW
16	Reserved	R
15	Endpoint Direction (EPDir) Indicates whether the transaction is IN or OUT. 1'b0: OUT 1'b1: IN	RW
14:11	Endpoint Number (EPNum) Indicates the endpoint number on the device serving as the data source or sink.	RW
10:0	Maximum Packet Size (MPS) Indicates the maximum packet size of the associated endpoint.	RW

Note:

[1], [2]: This bits will operate with Write set , self clear function.

26.6.2.27 Host Channel-n Split Control Register (HCSPLTn,0x504+n*0x20)

	HCSPLTn																															Base + 0x504+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SpltEna	Reserved														CompSplt	XactPos		HubAddr							PrtAddr						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	R/W
31	Split Enable (SpltEna) The application sets this Bits to indicate that this channel is enabled to perform split transactions.	RW
30:17	Reserved	R
16	Do Complete Split (CompSplt) The application sets this Bits to request the OTG host to perform a complete split trsnsaction.	RW
15:14	Transaction Position (XactPos) This Bits is used to determine whether to send all, first, middle, or last payloads with each OUT transaction. 2'b11: All. This is the entire data payload is of this transaction (which is less than or equal to 188 bytes). 2'b10: Begin. This is the first data payload of this transaction (which is larger than 188 bytes). 2'b00: Mid. This is the middle payload of this transaction (which is larger than 188 bytes). 2'b01: End. This is the last payload of this transaction (which is larger than 188 bytes).	RW
13:7	Hub Address (HubAddr) This Bits holds the device address of the transaction translator's hub.	RW
6:0	Port Address (PrtAddr) This Bits is the port number of the recipient transaction translator.	RW

26.6.2.28 Host Channel-n Interrupt Register (HCINTn,0x508+n*0x20)

	HCINTn																															Base + 0x508+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		DESC_LST_ROLLIntr	XCS_XACT_ERR	BNAIntr	DataTglErr	FrmOvrun	BblErr	XactErr	NYET	ACK	NAK	STALL	AHBErr	ChHltd	XferCompl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	Descriptor rollover interrupt (DESC_LST_ROLLIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when the corresponding channel's descriptor list rolls over.	RW[1]

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	For non Scatter/Gather DMA mode, this bit is reserved.	
12	Excessive Transaction Error (XCS_XACT_ERR) This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when 3 consecutive transaction errors occurred on the USB bus. XCS_XACT_ERR will not be generated for Isochronous channels. For non Scatter/Gather DMA mode, this bit is reserved.	RW[2]
11	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process. BNA will not be generated for Isochronous channels. For non Scatter/Gather DMA mode, this bit is reserved.	RW[3]
10	Data Toggle Error (DataTglErr) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[4]
9	Frame Overrun (FrmOvrun) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core	RW[5]
8	Babble Error (BblErr) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[6]
7	Transaction Error (XactErr) Indicates one of the following errors occurred on the USB. CRC check failure Timeout Bit stuff error False EOP In Scatter/Gather DMA mode, the interrupt due to this bit is not set.	RW[7]
6	NYET Response Received Interrupt (NYET) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[8]
5	ACK Response Received/Transmitted Interrupt (ACK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[9]
4	NAK Response Received Interrupt (NAK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[10]
3	STALL Response Received Interrupt (STALL) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[11]
2	AHB Error (AHBErr) This is generated only in DMA mode when there is an AHB error during	RW[12]

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	AHB read/write. The application can read the corresponding channel's DMA address register to get the error address.	
1	Channel Halted (ChHltd) In non Scatter/Gather DMA mode, it indicates the transfer completed abnormally either because of any USB transaction error or in response to disable request by the application or because of a completed transfer. In Scatter/Gather DMA mode, this indicates that transfer completed due to any of the following EOL being set in descriptor AHB error Excessive transaction errors In response to disable request by the application Babble Stall	RW[13]
0	Transfer Completed (XferCompl) For Scatter/Gather DMA mode, it indicates that current descriptor processing got completed with IOC bit set in its descriptor. In non Scatter/Gather DMA mode, it indicates that Transfer completed normally without any errors.	RW[14]

Note:

[1], [2]: This bits will operate with Self set , write clear function.

26.6.2.29 Host Channel-n Interrupt Mask Register (HCINTMSKn,0x50C+n*0x20)

	HCINTMSKn																															Base + 0x50C+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		ROLLIntrMsk	Reserved	BNAIntrMsk	DataTglErrMsk	DataTglErrMsk	BblErrMsk	XactErrMsk	NyetMsk	AckMsk	NakMsk	StallMsk	AHBErrMsk	ChHltdMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	Descriptor rollover interrupt Mask register (DESC_LST_ROLLIntrMsk) This bit is valid only when Scatter/Gather DMA mode is enabled. In non Scatter/Gather DMA mode, this bit is reserved.	RW
12	Reserved	R
11	BNA (Buffer Not Available) Interrupt mask register (BNAIntrMsk) This bit is valid only when Scatter/Gather DMA mode is enabled. In non Scatter/Gather DMA mode, this bit is reserved	RW

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10	Data Toggle Error Mask (DataTglErrMsk) This bit is not applicable in Scatter/Gather DMA mode.	R
9	Frame Overrun Mask (FrmOvrunMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
8	Babble Error Mask (BblErrMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
7	Transaction Error Mask (XactErrMsk) This bit is not applicable in Scatter/Gather DMA mode	RW
6	NYET Response Received Interrupt Mask (NyetMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
5	ACK Response Received/Transmitted Interrupt Mask (AckMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
4	NAK Response Received Interrupt Mask (NakMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
3	STALL Response Received Interrupt Mask (StallMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
2	AHB Error Mask (AHBErrMsk) Note: This bit is only accessible when OTG_ARCHITECTURE = 2	RW
1	Channel Halted Mask (ChHltdMsk)	RW
0	Transfer Completed Mask (XferComplMsk)	RW

26.6.2.30 Host Channel-n Transfer Size Register (HCTSIZn,0x510+n*0x20)

	HCTSIZn																															Base + 0x510+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	Pid		Reserved													NTD								SCHED_INFO							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Reserved	R
30:29	PID (Pid) The application programs this Bits with the type of PID to use for the initial transaction. The host maintains this Bits for the rest of the transfer. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA (non-control)	RW
28:16	Reserved	R
15:8	NTD (Number of Transfer Descriptors) (Non Isochronous)	RW

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	This value is in terms of number of descriptors. Maximum number of descriptor that can be present in the list is 64. The values can be from 0 to 63. 0 - 1 descriptor. 63 - 64 descriptors This Bits indicates the total number of descriptors present in that list. The core will wrap around after servicing NTD number of descriptors for that list. (Isochronous) This Bits indicates the number of descriptors present in that list.µframe The possible values for FS are 1 - 2 descriptors 3 - 4 descriptors 7 - 8 descriptors 15 - 16 descriptors 31 - 32 descriptors 63 - 64 descriptors The possible values for HS are 7 - 8 descriptors 15 - 16 descriptors 31 - 32 descriptors 63 - 64 descriptors 127 - 128 descriptors 255 - 256 descriptors	
7:0	SCHED_INFO (Schedule information) Every bit in this 8 bit register indicates scheduling for that microframe. Bit 0 indicates scheduling for 1st microframe and bit 7 indicates scheduling for 8th microframe in that frame. A value of 8'b11111111 indicates that the corresponding interrupt channel is scheduled to issue a token every microframe in that frame. A value of 8'b10101010 indicates that the corresponding interrupt channel is scheduled to issue a token every alternate microframe starting with second microframe. Note that this Bits is applicable only for periodic (Isochronous and Interrupt) channels.	RW

In Non-Scatter/Gather mode, HCTSIZn is defined as follows:

	HCTSIZn																															**Base + 0x510+n*0x20**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DoPng	Pid		PktCnt										XferSize																		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	R/W
31	Do Ping (DoPng) This bit is used only for OUT transfers. Setting this Bits to 1 directs the host to do PING protocol. Note: Do not set this bit for IN transfers. If this bit is set for IN transfers it disables the	RW
30:29	PID (Pid) The application programs this Bits with the type of PID to use for the initial transaction. The host maintains this Bits for the rest of the transfer. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA (non-control)/SETUP (control)	RW
28:19	Packet Count (PktCnt) This Bits is programmed by the application with the expected number of packets to be transmitted (OUT) or received (IN). The host decrements this count on every successful transmission or reception of an OUT/IN packet. Once this count reaches zero, the application is interrupted to indicate normal completion.	RW
18:0	Transfer Size (XferSize) For an OUT, this Bits is the number of data bytes the host sends during the transfer. For an IN, this Bits is the buffer size that the application has Reserved for the transfer. The application is expected to program this Bits as an integer multiple of the maximum packet size for IN transactions (periodic and non-periodic).	RW

26.6.2.31 Host Channel-n DMA Address Register (HCDMAn, ,0x514+n*0x20)

Buffer DMA Mode:

	HCDMAn																															
																	Base + 0x514+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAAddr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	DMA Address (DMAAddr)	RW

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	This Bits holds the start address in the external memory from which the data for the endpoint must be fetched or to which it must be stored. This register is incremented on every AHB transaction.	

Descriptor DMA Mode:

	HCDMAn																															
																	Base +0x514+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAAddr																							CTD						Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:9 (Non Isoc)	DMA Address (DMAAddr) Non-Isochronous: This Bits holds the start address of the 512 bytes page. The first descriptor in the list should be located in this address. The first descriptor may be or may not be ready. The core starts processing the list from the CTD value. Isochronous: This Bits holds the address of the 2*(nTD+1) bytes of locations in which the isochronous descriptors are present where N is based on nTD as per Table below 31:N | N-1:3 | 2:0 Base Address | Offset | 000 HS ISOC nTD N 7 6 15 7 31 8 63 9 127 10 255 11 FS ISOC nTD N 1 4 3 5 7 6 15 7 31 8 63 9	RW
8:3 (Non Isoc)	Current Transfer Desc (CTD): Non Isochronous: This value is in terms of number of descriptors. The values can be from 0 to 63. 0 - 1 descriptor. 63- 64 descriptors.	RW

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	This Bits indicates the current descriptor processed in the list. This Bits is updated both by application and the core. For example, if the application enables the channel after programming CTD=5, then the core will start processing the 6th descriptor. The address is obtained by adding a value of (8bytes*5=) 40(decimal) to DMAAddr. Isochronous: CTD for isochronous is based on the current frame/µframe value. Need to be set to zero by application.	
2:0	Reserved	R

26.6.2.32 Host Channel-n DMA Buffer Address Register (HCDMABn,0x51C+n*0x20)

	HCDMABn																															Base + 0x51C+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	buffer_address																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	Holds the current buffer address. This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this Bits is reserved.	R

26.6.2.33 Host Frame List Base Address Register (HFLBAddr,0x51C+n*0x20)

	HFLBAddr																															Base + 0x41C+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	flarm_list																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	The starting address of the Frame list. This register is used only for Isochronous and Interrupt Channels.	RW

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26.6.2.34 Device Configuration Register (DCFG,0x800)

	DCFG																															Base + 0x800
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ResValid						PerSchIntvl		DescDMA	EPMisCnt					Reserved				EnDevOutNak	PerFrInt		DevAddr							Ena32KHzS	NZStsOUTHShk	DevSpd	
RST	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:26	Resume Validation Period (ResValid) This Bits controls the period when the core resumes from a suspend. When this bit is set, the core counts for the ResValid number of clock cycles to detect a valid resume. This Bits is effective only when DCFG.Ena32KHzSusp is set.	RW
25:24	Periodic Scheduling Interval (PerSchIntvl) PerSchIntvl must be programmed only for Scatter/Gather DMA mode. Description: This Bits specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25,50 or 75% of (micro)frame. When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data. When no periodic endpoints are active, then the internal DMA engine services non- periodic endpoints, ignoring this Bits. After the specified time within a (micro)frame, the DMA switches to fetching for non- periodic endpoints. 2'b00: 25% of (micro)frame. 2'b01: 50% of (micro)frame. 2'b10: 75% of (micro)frame. 2'b11: Reserved.	RW
23	Enable Scatter/Gather DMA in Device mode (DescDMA). When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming: GAHBCFG.DMAEn=0,DCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0,DCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1,DCFG.DescDMA=0 => Buffered DMA mode GAHBCFG.DMAEn=1,DCFG.DescDMA=1 => Scatter/Gather DMA mode	RW

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22:18	IN Endpoint Mismatch Count (EPMisCnt) This Bits is valid only in shared FIFO operation. The application programs this filed with a count that determines when the core generates an Endpoint Mismatch interrupt (GINTSTS.EPMis). The core loads this value into an internal counter and decrements it. The counter is reloaded whenever there is a match or when the counter expires. The width of this counter depends on the depth of the Token Queue.	RW
17:14	Reserved	R
13	Enable Device OUT NAK (EnDevOutNak) This bit enables setting NAK for Bulk OUT endpoints after the transfer is completed when the core is operating in Device Descriptor DMA mode. 1'b0: The core does not set NAK after Bulk OUT transfer complete 1'b1: The core sets NAK after Bulk OUT transfer complete This bit is valid only when OTG_EN_DESC_DMA == 1'b1	RW
12:11	Periodic Frame Interval (PerFrInt) Indicates the time within a (micro)frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine if all the isochronous traffic for that (micro)frame is complete. 2'b00: 80% of the (micro)frame interval 2'b01: 85% 2'b10: 90% 2'b11: 95%	RW
10:4	Device Address (DevAddr) The application must program this Bits after every SetAddress control command.	RW
3	Enable 32-KHz Suspend Mode (Ena32KHzS) When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a suspend. This bit can only be set if USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero.	RW
2	Non-Zero-Length Status OUT Handshake (NZStsOUTHShk) The application can use this Bits to select the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. 1'b1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. 1'b0: Send the received OUT packet to the application (zero-length or nonzero-length) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.	RW
1:0	Device Speed (DevSpd) Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed	RW

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	is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 2'b00: High speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b01: Full speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b10: Low speed (USB 1.1 FS transceiver clock is 48 MHz) 2'b11: Full speed (USB 1.1 FS transceiver clock is 48 MHz)	

26.6.2.35 Device Control Register (DCTL,0x804)

	DCTL																																Base + 0x804
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														EnContOnBNA	NakOnBble	IgnrFrmNum	GMC		Reserved	PWROnPrgDone	CGOUTNak	SGOUTNak	CGNPInNak	SGNPInNak	TstCtl			GOUTNakSts	GNPINNakSts	SftDiscon	RmtWkUpSig
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Description	R/W
31:18	Reserved	R
17	Enable Continue on BNA (EnContOnBNA) This bit enables the DWC_otg core to continue on BNA for Bulk OUT endpoints. With this feature enabled, when a Bulk OUT endpoint receives a BNA interrupt the core starts processing the descriptor that caused the BNA interrupt after the endpoint re-enables the endpoint. 1'b0: After receiving BNA interrupt, the core disables the endpoint. When the endpoint is re-enabled by the application, the core starts processing from the DOEPDMA descriptor. 1'b1: After receiving BNA interrupt, the core disables the endpoint. When the endpoint is re-enabled by the application, the core starts processing from the descriptor that received the BNA interrupt. This bit is valid only when OTG_EN_DESC_DMA == 1'b1. It is a one-time programmable after reset bit like any other DCTL register bits.	RW
16	Set NAK automatically on babble (NakOnBble). The core sets NAK automatically for the endpoint on which babble is received.	RW
15	Ignore frame number for isochronous endpoints (IgnrFrmNum) Slave Mode (GAHBCFG.DMAEn=0): This bit is not valid in Slave mode and should not be programmed to 1.Non-Scatter/Gather DMA mode (GAHBCFG.DMAEn=1,DCFG.DescDMA=0): This bit is not used when Threshold mode is enabled and should not be programmed to 1. In non-Scatter/Gather DMA mode, the application receives transfer complete	RW

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	interrupt after transfers for multiple (micro)frames are completed. When Scatter/Gather DMA mode is disabled, this Bits is used by the application to enable periodic transfer interrupt. The application can program periodic endpoint transfers for multiple (micro)frames. 0: Periodic transfer interrupt feature is disabled; the application must program transfers for periodic endpoints every (micro)frame 1: Packets are not flushed when an ISOC IN token is received for an elapsed frame. The core ignores the frame number, sending packets as soon as the packets are ready, and the corresponding token is received. This Bits is also used by the application to enable periodic transfer interrupts. Scatter/Gather DMA Mode (GAHBCFG.DMAEn=1,DCFG.DescDMA=1): This bit is not applicable to high-speed, high-bandwidth transfers and should not be programmed to 1. In addition, this bit is not used when Threshold mode is enabled and should not be programmed to 1. 0: The core transmits the packets only in the frame number in which they are intended to be transmitted. 1: Packets are not flushed when an ISOC IN token is received for an elapsed frame. The core ignores the frame number, sending packets as soon as the packets are ready, and the corresponding token is received. When this bit is set, there must be only one packet per descriptor.	
14:13	Global Multi Count (GMC) GMC must be programmed only once after initialization. Applicable only for Scatter/Gather DMA mode. This indicates the number of packets to be serviced for that end point before moving to the next end point. It is only for non- periodic end points. 2'b00: Invalid. 2'b01: 1 packet. 2'b10: 2 packets. 2'b11: 3 packets. The value of this Bits automatically changes to 2'h1 when DCFG.DescDMA is set to 1. When Scatter/Gather DMA mode is disabled, this Bits is reserved and reads 2'b00.	RW
12	Reserved	R
11	Power-On Programming Done (PWROnPrgDone) The application uses this bit to indicate that register programming is completed after a wake-up from Power Down mode.	W
10	Clear Global OUT NAK (CGOUTNak) A write to this Bits clears the Global OUT NAK.	W
9	Set Global OUT NAK (SGOUTNak) A write to this Bits sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints.	W

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	The application must set the this bit only after making sure that the Global OUT NAK Effective bit in the Core Interrupt Register (GINTSTS.GOUTNakEff) is cleared.	
8	Clear Global Non-periodic IN NAK (CGNPInNak) A write to this Bits clears the Global Non-periodic IN NAK.	W
7	Set Global Non-periodic IN NAK (SGNPInNak) A write to this Bits sets the Global Non-periodic IN NAK.The application uses this bit to send a NAK handshake on all non-periodic IN endpoints. The core can also set this bit when a timeout condition is detected on a non-periodic endpoint in shared FIFO operation. The application must set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register (GINTSTS.GINNakEff) is cleared.	W
6:4	Test Control (TstCtl) 3'b000: Test mode disabled 3'b001: Test_J mode 3'b010: Test_K mode 3'b011: Test_SE0_NAK mode 3'b100: Test_Packet mode 3'b101: Test_Force_Enable Others: Reserved	RW
3	Global OUT NAK Status (GOUTNakSts) 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.	W
2	Global Non-periodic IN NAK Status (GNPINNakSts) 1'b0: A handshake is sent out based on the data availability in the transmit FIFO. 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.	W
1	Soft Disconnect (SftDiscon) The application uses this bit to signal the DWC_otg core to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device does not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. The minimum duration for which the core must keep this bit set is specified in Table 26-3. 1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration. 1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host.	RW

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	Note: This bit can be also used for ULPI/FS Serial interfaces. Note: This bit is not impacted by a soft reset.	
0	Remote Wakeup Signaling (RmtWkUpSig) When the application sets this bit, the core initiates remote signaling to wake the USB host. The application must set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1-15 ms after setting it.If LPM is enabled and the core is in the L1 (Sleep) state, when the application sets this bit, the core initiates L1 remote signaling to wake up the USB host. The application must set this bit to instruct the core to exit the Sleep state. As specified in the LPM specification, the hardware automatically clears this bit 50 µs ($T_{L1DevDrvResume}$) after being set by the application. The application must not set this bit when GLPMCFG bRemoteWake from the previous LPM transaction is zero.	RW

Table 26-3 Minimum Duration for Soft Disconnect

Operating Speed	Device state	Minimum Duration
High Speed	Suspend	1ms+2.5us
High Speed	Idle	3ms+2.5us
High Speed	Not Idle or Suspend	125us
Full Speed/Low Speed	Suspend	1ms+2.5us
Full Speed/Low Speed	Idle	2.5us
Full Speed/Low Speed	Not Idle or Suspend	2.5us

26.6.2.36 Device Status Register (DSTS,0x808)

	DSTS																															Base + 0x808
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										SOFFN														Reserved				ErrticErr	EnumSpd		SuspSts
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Description	R/W
31:22	Reserved	R
21:8	Frame or Microframe Number of the Received SOF (SOFFN) When the core is operating at high speed, this Bits contains a microframe number. When the core is operating at full or low speed, this Bits contains a frame number. Note: This register may return a non zero value if read immediately after power on reset.	R

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	In case the register bit reads non zero immediately after power on reset it does not indicate that SOF has been received from the host. The read value of this interrupt is valid only after a valid connection between host and device is established.	
7:4	Reserved	R
3	Erratic Error (ErrticErr) The core sets this bit to report any erratic errors (phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i is asserted for at least 2 ms, due to PHY error) seen on the UTMI+. Due to erratic errors, the DWC_otg core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register (GINTSTS.ErlySusp). If the early suspend is asserted due to an erratic error, the application can only perform a soft disconnect recover.	R
2:1	Enumerated Speed (EnumSpd) Indicates the speed at which the DWC_otg core has come up after speed detection through a chirp sequence. 2'b00: High speed (PHY clock is running at 30 or 60 MHz) 2'b01: Full speed (PHY clock is running at 30 or 60 MHz) 2'b10: Low speed (PHY clock is running at 48 MHz, internal phy_clk at 6 MHz) 2'b11: Full speed (PHY clock is running at 48 MHz) Low speed is not supported for devices using a UTMI+ PHY.	R
0	Suspend Status (SuspSts) In Device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time. The core comes out of the suspend: When there is any activity on the utmi_linestate signal When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig).	R

26.6.2.37 Device IN Endpoint Common Interrupt Mask Register (DIEPMSK,0x810)

	DIEPMSK																															Base + 0x810
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		NAKMsk	NAKMsk			BNAInIntrMsk	TxfifoUndrnMsk	Reserved	INEPNakEffMsk	INTknEPMisMsk	INTknTXFEmpMsk	TimeOUTMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	R/W
31:14	Reserved	R
13	NAK interrupt Mask (NAKMsk)	RW
12:10	Reserved	R
9	BNA Interrupt Mask (BNAInIntrMsk) This bit is valid only when Device Descriptor DMA is enabled.	RW
8	Fifo Underrun Mask (TxfifoUndrnMsk)	RW
7	Reserved	R
6	IN Endpoint NAK Effective Mask (INEPNakEffMsk)	RW
5	IN Token received with EP Mismatch Mask (INTknEPMisMsk)	RW
4	IN Token Received When TxFIFO Empty Mask (INTknTXFEmpMsk)	RW
3	Timeout Condition Mask (TimeOUTMsk) (Non-isochronous endpoints)	RW
2	AHB Error Mask (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

26.6.2.38 Device OUT Endpoint Common Interrupt Mask Register (DOEPMSK,0x814)

	DOEPMSK																															Base + 0x814
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NYETMsk	NAKMsk	BbleErrMsk	Reserved		BnaOutIntrMsk	OutPktErrMsk	Reserved	Back2BackSETup	Reserved	OUTTknEPdisMsk	SetUPMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:15	Reserved	R
14	NYET Interrupt Mask (NYETMsk)	RW
13	NAK Interrupt Mask (NAKMsk)	RW
12	Babble Interrupt Mask (BbleErrMsk)	RW
11:10	Reserved	R
9	BNA interrupt Mask (BnaOutIntrMsk)	RW
8	OUT Packet Error Mask (OutPktErrMsk)	RW
7	Reserved	R
6	Back-to-Back SETUP Packets Received Mask (Back2BackSETup) Applies to control OUT endpoints only.	RW
5	Reserved	R
4	OUT Token Received when Endpoint Disabled Mask (OUTTknEPdisMsk)	RW

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	Applies to control OUT endpoints only.	
3	SETUP Phase Done Mask (SetUPMsk) Applies to control endpoints only.	RW
2	AHB Error (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

26.6.2.39 Device All Endpoints Interrupt Register (DAINT,0x818)

	DAINT																															Base + 0x818
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OutEPInt																InEpInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT Endpoint Interrupt Bits (OutEPInt) One bit per OUT endpoint: Bit 16 for OUT endpoint 0, bit 31 for OUT endpoint 15	R
15:0	IN Endpoint Interrupt Bits (InEpInt) One bit per IN Endpoint: Bit 0 for IN endpoint 0, bit 15 for endpoint 15	R

26.6.2.40 Device All Endpoints Interrupt Mask Register (DAINTMSK,0x81C)

	DAINTMSK																															Base + 0x81C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OutEpMsk																InEpMsk															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT EP Interrupt Mask Bits (OutEpMsk) One per OUT Endpoint: Bit 16 for OUT EP 0, bit 31 for OUT EP 15 The value of this Bits depends on the number of OUT endpoints that are configured.	RW

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15:0	IN EP Interrupt Mask Bits (InEpMsk) One bit per IN Endpoint: Bit 0 for IN EP 0, bit 15 for IN EP 15 The value of this Bits depends on the number of IN endpoints that are configured.	RW

26.6.2.41 Device IN Token Sequence Learning Queue Read Register 1 (DTKNQR1,0x820)

	DTKNQP1																															Base + 0x820
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																								WrapBit	Reserved		INTknWPtr				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:8	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 5 Bits [27:24]: Endpoint number of Token 4 ..... Bits [15:12]: Endpoint number of Token 1 Bits [11:8]: Endpoint number of Token 0	R
7	Wrap Bit (WrapBit) This bit is set when the write pointer wraps. It is cleared when the learning queue is cleared.	R
6:5	Reserved	R
4:0	IN Token Queue Write Pointer (INTknWPtr)	R

26.6.2.42 Device IN Token Sequence Learning Queue Read Register 2 (DTKNQR2,0x824)

	DTKNQR2																															Base + 0x824
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	R/W
31:0	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 13 Bits [27:24]: Endpoint number of Token 12 ..... Bits [7:4]: Endpoint number of Token 7 Bits [3:0]: Endpoint number of Token 6	R

26.6.2.43 Device IN Token Sequence Learning Queue Read Register 3 (DTKNQR3,0x830)

	DTKNQR3																															Base + 0x830
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 21 Bits [27:24]: Endpoint number of Token 20 ..... Bits [7:4]: Endpoint number of Token 15 Bits [3:0]: Endpoint number of Token 14	R

26.6.2.44 Device IN Token Sequence Learning Queue Read Register 4 (DTKNQR4,0x834)

	DTKNQR4																															Base + 0x834
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	R/W
31:0	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 29 Bits [27:24]: Endpoint number of Token 28 ..... Bits [7:4]: Endpoint number of Token 23 Bits [3:0]: Endpoint number of Token 22	R

26.6.2.45 Device VBUS Discharge Time Register (DVBUSDIS,0x828)

	DVBUSDIS																															Base + 0x828
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DVBUSDis															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Reserved	R
15:0	Device VBUS Discharge Time (DVBUSDis) Specifies the VBUS discharge time after VBUS pulsing during SRP. This value equals: VBUS discharge time in PHY clocks / 1,024 The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width). Depending on your VBUS load, this value can need adjustment. The reset value is : PHY CLK 30MHz :0x0B8F PHY CLK 60MHz :0x17D7	RW

26.6.2.46 Device VBUS Pulsing Time Register (DVBUSPULSE,0x82C)

	DVBUSPULSE																															Base + 0x82C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				DVBUSPulse											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Description	R/W
31:12	Reserved	R
11:0	Device VBUS Pulsing Time (DVBUSPulse) Specifies the VBUS pulsing time during SRP. This value equals: VBUS pulsing time in PHY clocks / 1,024 The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width). The reset value is : PHY CLK 30MHz :0x2C6 PHY CLK 60MHz :0x5B8	RW

26.6.2.47 Device Threshold Control Register (DTHRCTL,0x830)

	DTHRCTL																															Base + 0x830
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				ArbPrkEn	Reserved	RxThrLen									RxThrEn	Reserved			AHBThrRatio		TxThrLen									ISOThrEn	NonISOThrEn
RST	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Description	R/W
31:28	Reserved	R
27	Arbiter Parking Enable (ArbPrkEn) This bit controls internal DMA arbiter parking for IN endpoints. When thresholding is enabled and this bit is set to one, then the arbiter parks on the IN endpoint for which there is a token received on the USB. This is done to avoid getting into underrun conditions. By default the parking is enabled.	RW
26	Reserved	R
25:17	Receive Threshold Length (RxThrLen) This Bits specifies Receive thresholding size in DWORDS. This Bits also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).	RW
16	Receive Threshold Enable (RxThrEn) When this bit is set, the core enables thresholding in the receive direction. Note: Synopsys recommends that you do not enable RxThrEn, because it may cause issues in the RxFIFO especially during error conditions such as RxError and	RW

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	Babble.	
15:13	Reserved	R
12:11	AHB Threshold Ratio (AHBThrRatio) These bits define the ratio between the AHB threshold and the MAC threshold for the transmit path only. The AHB threshold always remains less than or equal to the USB threshold, because this does not increase overhead. Both the AHB and the MAC threshold must be DWORD-aligned. The application needs to program TxThrLen and the AHBThrRatio to make the AHB Threshold value DWORD aligned. If the AHB threshold value is not DWORD aligned, the core might not behave correctly. When programming the TxThrLen and AHBThrRatio, the application must ensure that the minimum AHB threshold value does not go below 8 DWORDS to meet the USB turnaround time requirements.	RW
10:2	Transmit Threshold Length (TxThrLen) This Bits specifies Transmit thresholding size in DWORDS. This Bits also forms the MAC threshold and specifies the amount of data, in bytes, to be in the corresponding endpoint transmit FIFO before the core can start a transmit on the USB. When the value of AHBThrRatio is 2'h00, the threshold length must be at least 8 DWORDS. If the AHBThrRatio is nonzero, the application must ensure that the AHB threshold value does not go below the recommended 8 DWORDs. This Bits controls both isochronous and non-isochronous IN endpoint thresholds. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).	RW
1	ISO IN Endpoints Threshold Enable. (ISOThrEn) When this bit is set, the core enables thresholding for isochronous IN endpoints.	RW
0	Non-ISO IN Endpoints Threshold Enable. (NonISOThrEn) When this bit is set, the core enables thresholding for Non Isochronous IN endpoints.	RW

26.6.2.48 Device IN Endpoint FIFO Empty Interrupt Mask Register(DIEPEMPMSK,0x834)

	DIEPEMPMSK																															Base + 0x834
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																InEpTxfEmpMsk															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	R/W
31:16	Reserved	R
15:0	IN EP Tx FIFO Empty Interrupt Mask Bits (InEpTxfEmpMsk) These bits acts as mask bits for DIEPINTn. TxFEmp interrupt One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for endpoint 15	RW

26.6.2.49 Device Each Endpoint Interrupt Register (DEACHINT,0x838)

	DEACHINT																															Base + 0x838
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EchOutEPInt																EchInEpInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT Endpoint Interrupt Bits (EchOutEPInt) One bit per OUT endpoint: Bit 16 for OUT endpoint 0 ... Bit 31 for OUT endpoint 15	R
15:0	IN Endpoint Interrupt Bits (EchInEpInt) One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for IN endpoint 15	R

26.6.2.50 Device Each Endpoint Interrupt Register Mask (DEACHINTMSK,0x83C)

	DEACHINTMSK																															Base + 0x83C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EchOutEPInt																EchInEpInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Description	R/W
31:16	OUT EP Interrupt Mask Bits (EchOutEpMsk) One per OUT Endpoint: Bit 16 for IN endpoint 0 ... Bit 31 for IN endpoint 15	RW
15:0	IN EP Interrupt Mask Bits (EchInEpMsk) One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for IN endpoint 15	RW

26.6.2.51 Device Each In Endpoint-n Interrupt Register (DIEPEACHMSKn,0x840)

	DIEPEACHMSKn																															Base + 0x840
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		NAKMsk	Reserved			BNAInIntrMsk	TxfifoUndrnMsk	Reserved	INEPNakEffMsk	INTknEPMisMsk	INTknTXFEmpMsk	TimeOUTMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	NAK interrupt Mask (NAKMsk)	RW
12:10	Reserved	R
9	BNA interrupt Mask (BNAInIntrMsk)	RW
8	Fifo Under run Mask (TxfifoUndrnMsk)	RW
7	Reserved	R
6	IN Endpoint NAK Effective Mask (INEPNakEffMsk)	RW
5	IN Token received with EP Mismatch Mask (INTknEPMisMsk)	RW
4	IN Token Received When TxFIFO Empty Mask (INTknTXFEmpMsk)	RW
3	Timeout Condition Mask (TimeOUTMsk) (Non-isochronous endpoints)	RW
2	AHB Error Mask (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

26.6.2.52 Device Each Out Endpoint-n Interrupt Register (DOEPEACHMSKn,0x880+n*0x4)

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	DOEPEACHMSKn																															Base + 0x880+n*0x4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NYETMsk	NAKMsk	BbleErrMsk	Reserved		BnaOutIntrMsk	OutPktErrMsk	Reserved	Back2BackSETup	Reserved	OUTTknEPdisMsk	SetUPMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:15	Reserved	R
14	NYET interrupt Mask (NYETMsk)	RW
13	NAK interrupt Mask (NAKMsk)	RW
12	Babble interrupt Mask (BbleErrMsk)	RW
11:10	Reserved	R
9	BNA interrupt Mask (BnaOutIntrMsk)	RW
8	OUT Packet Error Mask (OutPktErrMsk)	RW
7	Reserved	R
6	Back-to-Back SETUP Packets Received Mask (Back2BackSETup) Applies to control OUT endpoints only.	RW
5	Reserved	R
4	OUT Token Received when Endpoint Disabled Mask (OUTTknEPdisMsk) Applies to control OUT endpoints only.	RW
3	SETUP Phase Done Mask (SetUPMsk) Applies to control endpoints only.	RW
2	AHB Error (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

26.6.2.53 Device Control IN Endpoint 0 Control Register (DIEPCTL0,0x900)

	DIEPCTL0																															Base + 0x900
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPEna	EPDis	Reserved		SNAK	CNAK	TxFNum				Stall	Reserved	EPType		NAKSts	Reserved	USBActEP	NextEp				Reserved									MPS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Endpoint Enable (EPEna)	RW[1]

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	When Scatter/Gather DMA mode is enabled, for IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. When Scatter/Gather DMA mode is disabled—such as in buffer-pointer based DMA mode—this bit indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting the following interrupts on this endpoint: Endpoint Disabled Transfer Completed	
30	Endpoint Disable (EPDis) The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. This bit is valid only when DMA mode is enabled.	RW[2]
29:28	Reserved	R
27	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint.	W
26	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.	W
25:22	TxFIFO Number (TxFNum) For Shared FIFO operation, this value is always set to 0, indicating that control IN endpoint 0 data is always written in the Non-Periodic Transmit FIFO. For Dedicated FIFO operation, this value is set to the FIFO number that is assigned to IN Endpoint 0.	RW
21	STALL Handshake (Stall) The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority.	RW[3]
20	Reserved	R
19:18	Endpoint Type (EPType) Hardcoded to 00 for control.	R
17	NAK Status (NAKSts) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status 1'b1: The core is transmitting NAK handshakes on this endpoint. When this bit is set, either by the application or core, the core stops transmitting data, even if there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	R
16	Reserved	R

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15	USB Active Endpoint (USBActEP) This bit is always set to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.	R
14:11	Next Endpoint (NextEp) Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this Bits, even when the Endpoint Enable (EPEna) bit is not set. This Bits is not valid in Slave mode. Note: This Bits is valid only for Shared FIFO operations.	RW
10:2	Reserved	R
1:0	Maximum Packet Size (MPS) Applies to IN and OUT endpoints. The application must program this Bits with the maximum packet size for the current logical endpoint.	RW

Note:

[1], [2], [3]: This bits will operate with Write set , self clear function.

26.6.2.54 Device Control OUT Endpoint 0 Control Register (DOEPCTL0,0xB00)

	DOEPCTL																															Base + 0xB00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPEna	EPDis	Reserved		SNAK	CNAK	Reserved				Stall	Snp	EPType		NAKSts	Reserved	USBActEP	Reserved													MPS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Endpoint Enable (EPEna) When Scatter/Gather DMA mode is enabled, for OUT endpoints this bit indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is disabled—(such as for buffer-pointer based DMA mode)—this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done Endpoint Disabled	RW[1]

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	Transfer Completed Note: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory.	
30	Endpoint Disable (EPDis) The application cannot disable control OUT endpoint 0.	R
29:28	Reserved	R
27	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.	W
26	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.	W
25:22	Reserved	R
21	STALL Handshake (Stall) The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	RW[2]
20	Snoop Mode (Snp) This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	RW
19:18	Endpoint Type (EPType) Hardcoded to 2'b00 for control.	R
17	NAK Status (NAKSts) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even if there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	R
16	Reserved	R
15	USB Active Endpoint (USBActEP) This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces.	R
14:2	Reserved	R
1:0	Maximum Packet Size (MPS) The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. 2'b00: 64 bytes	R

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	2'b01: 32 bytes 2'b10: 16 bytes 2'b11: 8 bytes	

Note:

[1],[2]: This bits will operate with Write set , self clear function.

26.6.2.55 Device Endpoint-n Control Register (DIEPCTLn/DOEPCTLn, 0x900/0xB00+n*0x20)

	DIEPCTLn/DOEPCTLn																Base + 0x900/0xB00+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum				Stall	Snp	EPType		NAKSts	DPID	USBActEP	NextEp				MPS										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled—such as for buffer-pointer based DMA mode: For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint. SETUP Phase Done Endpoint Disabled Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.	RW[1]
30	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the	RW[2]

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	Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.	
29	Set DATA1 PID (SetD1PID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this Bits sets the Endpoint Data PID (DPID) Bits in this register to DATA1. This Bits is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Set Odd (micro)frame (SetOddFr) Applies to isochronous IN and OUT endpoints only. Writing to this Bits sets the Even/Odd (micro)frame (EO_FrNum) Bits to odd (micro)frame. This Bits is not applicable for Scatter/Gather DMA mode.	W W
28	Set DATA0 PID (SetD0PID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this Bits sets the Endpoint Data PID (DPID) Bits in this register to DATA0. This Bits is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this Bits sets the Even/Odd (micro)frame (EO_FrNum) Bits to even (micro) frame. When Scatter/Gather DMA mode is enabled, this Bits is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure.	W
27	Set NAK (SNAK) Applies to IN and OUT endpoints. A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for OUT endpoints on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.	W
26	Clear NAK (CNAK) Applies to IN and OUT endpoints. A write to this bit clears the NAK bit for the endpoint.	W
25:22	TxFIFO Number (TxFNum) *Shared FIFO Operation*—non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. 4'h0: Non-Periodic TxFIFO Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for	RW

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	applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum Bits is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum Bits. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. *Dedicated FIFO Operation*—these bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This Bits is valid only for IN endpoints.	
21	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	RW RW[3]
20	Snoop Mode (Snp) Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	RW
19:18	Endpoint Type (EPType) Applies to IN and OUT endpoints. This is the transfer type supported by this logical endpoint. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt	RW
17	NAK Status (NAKSts) Applies to IN and OUT endpoints. Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if	R

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	there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	
16	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID Bitss of this register to program either DATA0 or DATA1 PID. 1'b0: DATA0 1'b1: DATA1 This Bits is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr Bitss in this register. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this Bits is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.	R
15	USB Active Endpoint (USBActEP) Applies to IN and OUT endpoints. Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.	RW[4]
14:11	Next Endpoint (NextEp) Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this Bits, even when the Endpoint Enable (EPEna) bit is low. This Bits is not valid in Slave mode operation. Note: This Bits is valid only for Shared FIFO operations.	RW
10:0	Maximum Packet Size (MPS) Applies to IN and OUT endpoints. The application must program this Bits with the maximum packet size for the current	RW

Note:[1]~[2]: This bits will operate with Write set , self clear function.

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26.6.2.56 Device Endpoint-n Interrupt Register (DIEPINTn/DOEPINTn, 0x908/0xB08+n*0x20)

	DIEPINTn/DOEPINTn																															
	Base + 0x908/0xB08+n*0x20																															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NYETIntrpt	NAKIntrpt	BbleErrIntrpt	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn	TxFEmp	INEPNakEff	INTknEPMis	INTknTXFEmp	TimeOUT	AHBErr	EPDisbld	XferCompl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:15	Reserved	R
14	NYET interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint.	RW[1]
13	NAK interrupt (NAKIntrpt) The core generates this interrupt when a NAK is transmitted. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to unavailability of data in the TXFifo.	RW[2]
12	BbleErr (Babble Error) interrupt (BbleErrIntrpt) The core generates this interrupt when babble is received for the endpoint.	RW[3]
11	PktDrpSts (Packet Dropped Status) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. **Dependency**: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.	RW[4]
10	Reserved	R
9	BNA (Buffer Not Available) Interrupt (BNAIntr) The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. **Dependency**: This bit is valid only when Scatter/Gather DMA mode is enabled.	RW[5]
8	FIFO Underrun (TxfifoUndrn) Applies to IN endpoints only The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. **Dependency**: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO=1 Thresholding is enabled OUT Packet Error (OutPktErr)	RW[6] RW[7]

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	Applies to OUT endpoints only This interrupt is asserted when the core detects an overflow or a CRC error for an OUT packet. **Dependency**: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO=1 Thresholding is enabled.	
7	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN Endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)).	R
6	N Endpoint NAK Effective (INEPNakEff) This bit should be cleared by writing a 1'b1 before writing a 1'b1 to corresponding DIEPCTLn.CNAK. The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. This bit is applicable only when the endpoint is enabled. Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. This bit is not valid in Slave mode.	RW[8] RW[9]
5	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Status Phase Received For Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in case of Scatter Gather DMA mode.	RW[10]
4	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Indicates that an IN token was received when the associated TxFIFO (periodic/non-	RW[11]

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	periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. OUT Token Received When Endpoint Disabled (OUTTknEPdis) Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.	
3	Timeout Condition (TimeOUT) In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.	RW[12]
2	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.	RW[13]
1	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.	RW[14]
0	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled For IN endpoint this Bits indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. For OUT endpoint this Bits indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. When Scatter/Gather DMA mode is disabled, this Bits indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.	RW[15]

Note:

[1]~[15]: This bits will operate with Self set , Write clear function.

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26.6.2.57 Device Endpoint 0 Transfer Size Register (DIEPTSIZ0/DOEPTSIZ0,0x910/0xB10)

	DIEPTSIZ0/DOEPTSIZ0																															Base + 0x910/0xB10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											PktCnt		Reserved												XferSize						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:21	Reserved	R
20:19	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This Bits is decremented every time a packet (maximum size or short packet) is read from the TxFIFO.	RW
18:7	Reserved	R
6:0	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this Bits every time a packet from the external memory is written to the TxFIFO.	RW

26.6.2.58 Device Endpoint-n Transfer Size Register (DIEPTSIZn/DOEPTSIZn, 0x910/0xB10+n*0x20)

	DIEPTSIZn/DOEPTSIZn																															Base + 0x910/0xB10+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	MC		PktCnt										XferSize																		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Reserved	R
30:29	Multi Count (MC)	RW

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	Applies to IN endpoints only. For periodic IN endpoints, this Bits indicates the number of packets that must be transmitted per microframe on the USB. The core uses this Bits to calculate the data PID for isochronous IN endpoints. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets For non-periodic IN endpoints, this Bits is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint Bits of the Device Endpoint-*n* Control register (DIEPCTLn.NextEp). Received Data PID (RxDPID) Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This Bits specifies the number of back-to-back SETUP data packets the endpoint can receive. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets	 R R RW
28:19	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for this endpoint (PktCnt = XferSize / MPS). IN Endpoints: This Bits is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. OUT Endpoints: This Bits is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.	RW
18:0	Transfer Size (XferSize) This Bits contains the transfer size in bytes for the current endpoint. The transfer size (XferSize) = Sum of buffer sizes across all descriptors in the list for the endpoint. In Buffer DMA, the core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. IN Endpoints: The core decrements this Bits every time a packet from the external	RW

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	memory is written to the TxFIFO. OUT Endpoints: The core decrements this Bits every time a packet is read from the RxFIFO and written to the external memory.	

26.6.2.59 Device Endpoint-n DMA Address Register (DIEPDMAn/DOEPDMAn, 0x914/0xB14+n*0x20)

	DIEPDMAnDOEPDMAn																Base + 0x914/0xB14+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAAddr																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	DMA Address (DMAAddr) Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this Bits stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this Bits. When Scatter/Gather DMA mode is enabled, this Bits indicates the base pointer for the descriptor list.	RW

26.6.2.60 Device Endpoint-n DMA Buffer Address Register (DIEPDMABn/DOEPDMABn, 0x91C/0xB1C+n*0x20)

	DIEPDMABn/DOEPDMABn																Base + 0x91C/0xB1C+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMABufferAddr																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Description	R/W
31:0	DMA Buffer Address (DMABufferAddr) Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this Bits is reserved.	R

26.6.2.61 Device IN Endpoint Transmit FIFO Status Register (DTXFSTSn,0x918)

	DTXFSTSn																															Base + 0x918
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																INEPTxFSpcAvail															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved.	R
15:0	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. 16'h0: Endpoint TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0≤n≤32,768) 16'h8000: 32,768 words available Others: Reserved	R

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27 Gigabit Ethernet Media Access Controller (GMAC)

27.1 Overview

The processor contains one Ethernet media access controller (GMAC), each capable of supporting 10/100Mbps Ethernet. The MAC provides the interface between the host application and the PHY layer through RMII. The PHY layer device is external to the processor.

27.2 Features

- 10, 100Mbps data transfer rates with the following PHY interfaces:
  - RMII interface to communicate with an external Fast Ethernet PHY
- Full-duplex operation:
  - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
  - forwarding of received Pause frames to the user application
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Frame bursting and frame extension in 100 Mbps half-duplex operation
- Preamble and start of frame data (SFD) insertion in Transmit path
- Preamble and SFD deletion in the Receive path
- Automatic CRC and pad generation controllable on a per-frame basis
- Automatic Pad and CRC Stripping options for receive frames
- Flexible address filtering modes, such as:
  - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
  - 64-bit Hash filter for multicast and unicast (DA) addresses
  - Option to pass all multicast addressed frames
  - Promiscuous mode to pass all frames without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report
- Support Standard or Jumbo Ethernet frames with up to 2 KB of size
- IEEE 802.1Q VLAN tag detection for reception frames
- MDIO master interface for PHY device configuration and management
- CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
- Programmable watchdog timeout limit in the receive path
- Detect remote wake-up frames and AMD magic packets

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27.3 Block Diagram

Figure 27-1 GMAC Block Diagram

27.4 Functional Description

The GMAC enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. The GMAC is a configurable product that can be optimized for gate count and latency to meet the application requirements. You can use the GMAC in number of applications such as switches and network interface cards.

27.5 Pins Description

Table 27-1 GMAC pin description

Pin	I/O	Description
PHY_CLK	Output	External PHY clock Function: The PHY_CLK is provide for External GMAC PHY, and the frequency is 50MHz
RX_DV	Input	PHY Receive Data Valid Function: This signal is driven by PHY and has multiple functions depending on which PHY interface is selected: RMII: Contains the crs and data valid information of the receive interface. Synchronous to: REF_CLK
RXD [1:0]	Input	PHY Receive Data Function: This is a bundle of two data signals received from the PHY: RMII: Bits [1:0] provide the RMII receive data. The validity of the data

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		is qualified with phy_rxdv_o. Synchronous to: REF_CLK
TX_CLK(REF_CLK)	Input	Transmission Clock Function: This is the transmission REF clock provided by the external PHY or oscillator . When in RMII mode, REF_CLK 50MZ whenever at 100-Mbps or at 10-Mbps.
TX_EN	Output	PHY Transmit Data Enable Function: This signal is driven by the MAC and has multiple functions depending on which PHY interface is selected: RMII: When high, indicates that valid data is being transmitted on the phy_txd bus. Synchronous to: REF_CLK
TXD [1:0]	Output	PHY Transmit Data Function: This is a group of two transmit data signals driven by the MAC. RMII: Bits [1:0] provide the RMII transmit data. The validity of the data is qualified with phy_txen_o. Synchronous to: REF_CLK
MDC	Output	Management Data Clock Function: The maximum frequency of this clock is 2.5 MHz. This clock is generated from the GMAC HCLK through a clock divider.
MDIO	I/O	MDIO is the bidirectional data signal between the MAC and the PHY that is clocked by MDC.

27.6 Data Format Description

For RMII mode , the data width is 2bits,

27.7 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R- Read only

   W- Write only

   RW- Read and Write

   RCW- Read and Write, but Clear to 0 by Read

   RSW- Read and Write, but Set to 1 by Read

   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect

   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect

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RC- Read only, and Clear to 0 by read

RS- Read only, and Set to 1 by read

3. Reset Value

1 - reset to 1

0 - reset to 0

? - value unknown after reset

27.7.1 Register Memory Map

Table 27-2 Registers Memory Map Base Address

Name	Base	Description
GMAC	0x134B0000	Address base of GMAC

The GMAC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 27-3 GMAC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
DMA_BMR	RW	0x0002_0101	0x1000	32
DMA_TPDR	RW	0x0000_0000	0x1004	32
DMA_RPDR	RW	0x0000_0000	0x1008	32
DMA_RDLAR	RW	0x0000_0000	0x100C	32
DMA_TDLAR	RW	0x0000_0000	0x1010	32
DMA_SR	RW	0x0000_0000	0x1014	32
DMA_OMR	RW	0x0000_0000	0x1018	32
DMA_IER	RW	0x0000_0000	0x101C	32
DMA_MFOCR	RC	0x0000_0000	0x1020	32
DMA_RIWTR	RW	0x0000_0000	0x1024	32
DMA_AHBSR	R	0x0000_0000	0x102C	32
MAC_CR	RW	0x0000_0000	0x0000	32
MAC_FFR	RW	0x0000_0000	0x0004	32
MAC_HTHR	RW	0x0000_0000	0x0008	32
MAC_HTLR	RW	0x0000_0000	0x000C	32
GMII_AR	RW	0x0000_0000	0x0010	32
GMII_DR	RW	0x0000_0000	0x0014	32
MAC_FCR	RW	0x0000_0000	0x0018	32
MAC_VTR	RW	0x0000_0000	0x001C	32
MAC_DR	R	0x0000_0000	0x0024	32
LPI_CSR	RW	0x0000_0000	0x0030	32
LPI_TCR	RW	0x03E8_0000	0x0034	32
MAC_ISR	R	0x0000_0000	0x0038	32
MAC_IMR	RW	0x0000_0000	0x003C	32
MAC_A0HR	RW	0x8000_FFFF	0x0040	32

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MAC_A0LR	RW	0xFFFF_FFFF	0x0044	32
MAC_A1HR	RW	0x0000_FFFF	0x0048	32
MAC_A1LR	RW	0xFFFF_FFFF	0x004C	32
MAC_WTR	RW	0x0000_0000	0x00DC	32

27.7.2 Register and Fields Description

27.7.2.1 DMA Bus Mode Register(DMA_BMR,0x1000)

	DMA_BMR																															Base + 0x1000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RIB	Reserved	PRWG		TXPR	MB	AAL	PLBx8	USP	RPBL						FB	PR	PBL							ATDS	DSL					DA	SWR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
31	RIB	Rebuild INCRx Burst When this bit is set high and the AHB master gets an EBT (Retry, Split, or Losing bus grant), the AHB master interface rebuilds the pending beats of any burst transfer initiated with INCRx. The AHB master interface rebuilds the beats with a combination of specified bursts with INCRx and SINGLE. By default, the AHB master interface rebuilds pending beats of an EBT with an unspecified (INCR) burst.	RW
30	Reserved	Writing has no effect. Read as zero.	R
29:28	PRWG	Channel Priority Weights This Bits sets the priority weights for Channel 0 during the round-robin arbitration between the DMA channels for the system bus. 00: The priority weight is 1. 01: The priority weight is 2. 10: The priority weight is 3. 11: The priority weight is 4	RW
27	TXPR	Transmit Priority When set, this bit indicates that the transmit DMA has higher priority than the receive DMA during arbitration for the system-side bus.	RW
26	MB	Mixed Burst When this bit is set high and the FB bit is low, the AHB master	RW

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		interface starts all bursts of length more than 16 with INCR (undefined burst), whereas it reverts to fixed burst transfers (INCRx and SINGLE) for burst length of 16 and less.	
25	AAL	Address-Aligned Beats When this bit is set high and the FB bit is equal to 1, the AHB interface generates all bursts aligned to the start address LS bits. If the FB bit is equal to 0, the first burst (accessing the start address of data buffer) is not aligned, but subsequent bursts are aligned to the address.	RW
24	PBLx8	PBLx8 Mode When set high, this bit multiplies the programmed PBL value (Bits [22:17] and Bits[13:8]) eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.	RW
23	USP	Use Separate PBL When set high, this bit configures the Rx DMA to use the value configured in Bits [22:17] as PBL. The PBL value in Bits [13:8] is applicable only to the Tx DMA operations. When reset to low, the PBL value in Bits [13:8] is applicable for both DMA engines.	RW
22:17	RPBL	Rx DMA PBL This Bits indicates the maximum number of beats to be transferred in one Rx DMA transaction. This is the maximum value that is used in a single block Read or Write. The Rx DMA always attempts to burst as specified in the RPBL bit each time it starts a Burst transfer on the host bus. You can program RPBL with values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. This Bits is valid and applicable only when USP is set high.	RW
16	FB	Fixed Burst This bit controls the AHB master interface performs fixed burst transfers or not. When set, the AHB interface uses only SINGLE, INCR4, INCR8, or INCR16 during start of the normal burst transfers. When reset, the AHB interface uses SINGLE and INCR burst transfer operations.	RW
15:14	PR	Priority Ratio These bits control the priority ratio in the weighted round-robin arbitration between the Rx DMA and Tx DMA. These bits are valid only when Bit 1 (DA) is reset. The priority ratio is Rx:Tx or Tx:Rx depending on whether Bit 27 (TXPR) is reset or set. 00: The Priority Ratio is 1:1. 01: The Priority Ratio is 2:1. 10: The Priority Ratio is 3:1.	RW

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		11: The Priority Ratio is 4:1.	
13:8	PBL	Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA transaction. This is the maximum value that is used in a single block Read or Write. The DMA always attempts to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. When USP is set high, this PBL value is applicable only for Tx DMA transactions. If the number of beats to be transferred is more than 32, then perform the following steps: 1. Set the PBLx8 mode. 2. Set the PBL. For example, if the maximum number of beats to be transferred is 64, then first set PBLx8 to 1 and then set PBL to 8. The PBL values have the following limitation: The maximum number of possible beats (PBL) is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified.	RW
7	ATDS	Alternate Descriptor Size When set, the size of the alternate descriptor increases to 32 bytes (8 DWORDS). This is required when the IPC Full Checksum Offload Engine (Type 2) is enabled in the receiver. The enhanced descriptor is not required if the IPC Full Checksum Offload Engine (Type 2) features are not enabled. In such case, you can use the 16 bytes descriptor to save 4 bytes of memory. IPC Full Checksum Offload Engine (Type 2) feature Otherwise, this bit is reserved and is read-only. When reset, the descriptor size reverts back to 4 DWORDs (16 bytes). This bit preserves the backward compatibility for the descriptor size. In versions prior to 3.50a, the descriptor size is 16 bytes for both normal and enhanced descriptors.	RW
6:2	DSL	Descriptor Skip Length This bit specifies the number of Word, Dword, or Lword (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of current descriptor to the start of next descriptor. When the DSL value is equal to zero, the descriptor table is taken as contiguous by the DMA in Ring mode.	RW
1	DA	DMA Arbitration Scheme This bit specifies the arbitration scheme between the transmit and	RW

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		receive paths of Channel 0. 0: Weighted round-robin with Rx:Tx or Tx:Rx The priority between the paths is according to the priority specified in Bits [15:14] (PR) and priority weights specified in Bit 27 (TXPR). 1: Fixed priority The transmit path has priority over receive path when Bit 27 (TXPR) is set. Otherwise, receive path has priority over the transmit path.	
0	SWR	Software Reset When this bit is set, the MAC DMA Controller resets the logic and all internal registers of the MAC. It is cleared automatically after the reset operation is complete in all of the GMAC clock domains. Before reprogramming any register of the GMAC, you should read a zero (0) value in this bit. Note: The Software reset function is driven only by this bit. Bit 0 of Register 64 (Channel 1 Bus Mode Register) or Register 128 (Channel 2 Bus Mode Register) has no impact on the Software reset function. The reset operation is completed only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for the software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock.	RW[1]

Note:

1. Only support RMII mode
2. [1]:Write Set, self clear

27.7.2.2 DMA Transmit Poll Demand Register(DMA_TPDR,0x1004)

	DMA_TPDR																															Base+ 0x1004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPD																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TPD	Transmit Poll Demand When these bits are written with any value, the DMA reads the	RW

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		current descriptor to which the Register 18 (Current Host Transmit Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the transmission returns to the Suspend state and Bit 2 (TU) of Register 5 (Status Register) is asserted. If the descriptor is available, the transmission resumes.	

Note:

Only support RMII mode

27.7.2.3 DMA Receive Poll Demand Register(DMA_RPDR,0x1008)

	DMA_RPDR																															Base + 0x1008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RPD																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	RPD	Receive Poll Demand When these bits are written with any value, the DMA reads the current descriptor to which the Register 19 (Current Host Receive Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the reception returns to the Suspended state and Bit 7 (RU) of Register 5 (Status Register) is asserted. If the descriptor is available, the Rx DMA returns to the active state.	RW

Note:

Only support RMII mode

27.7.2.4 DMA Receive Descriptor List Address Register(DMA_RDLAR,0x100C)

	DMA_RDLAR																															Base + 0x100C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDESLA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:0	RDESLA	Start of Receive List This Bits contains the base address of the first descriptor in the Receive Descriptor list. The LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO).	RW

Note:

Only support RMII mode

27.7.2.5 DMA Transmit Descriptor List Address Register(DMA_TDLAR,0x1010)

	DMA_TDLAR																															Base + 0x1010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDESLA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TDESLA	Start of Transmit List This Bits contains the base address of the first descriptor in the Transmit Descriptor list. The LSB bits (1:0, 2:0, 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and are internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO).	RW

Note:

Only support RMII mode

27.7.2.6 DMA Status Register(DMA_SR,0x1014)

	DMA_BMR																															Base + 0x1014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	GLPLL/GTMSI	TTI	GPI	GMI	GLI	EB			TS			RS			NIS	AIS	ERI	FBI	Reserved		ETI	RWT	RPS	RU	RI	UNF	OVF	TJT	TU	TPS	TI
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31	Reserved	Writing has no effect, read as zero.	R
30	GLPII OR GTMSI	GLPII: GMAC LPI Interrupt (for Channel 0) This bit indicates an interrupt event in the LPI logic of the GMAC. To reset this bit to 1'b0, the software must read the corresponding registers in the gmac to get the exact cause of the interrupt and clear its source. **Note:** GLPII status is given only in Channel 0 DMA register and is applicable only when the Energy Efficient Ethernet feature is enabled. GTMSI: GMAC TMS Interrupt (for Channel 1 and Channel 2) This bit indicates an interrupt event in the traffic manager and scheduler logic of gmac. To reset this bit, the software must read the corresponding registers (Channel Status Register) to get the exact cause of the interrupt and clear its source.	R
29	TTI	Reserved	R
28	GPI	GMAC PMT Interrupt This bit indicates an interrupt event in the PMT module of the gmac. The software must read the PMT Control and Status Register in the MAC to get the exact cause of interrupt and clear its source to reset this bit to 1'b0. The interrupt signal from the gmac subsystem is high when this bit is high.	R
27	GMI	GMAC MMC Interrupt This bit reflects an interrupt event in the MMC module of the GMAC. The software must read the corresponding registers in the GMAC to get the exact cause of the interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the gmac subsystem is high when this bit is high. This bit is applicable only when the MAC Management Counters (MMC) are enabled. Otherwise, this bit is reserved.	R
26	GLI	GMAC Line Interface Interrupt When set, this bit reflects any of the following interrupt events in the GMAC interfaces: RGMII: Link change event To identify the exact cause of the interrupt, the software must first read Bit 11 and Bits[2:0] of Register 14 (Interrupt Status Register) and then to clear the source of interrupt (which also clears the GLI interrupt), read any of the following corresponding registers: PCS (TBI, RTBI, or SGMII): Register 49 (AN Status Register) RGMII: Register 54 (RGMII Control and Status Register) General Purpose Input (GPI): Register 56 (General Purpose IO Register)	R

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25:23	EB	Error Bits This Bits indicates the type of error that caused a Bus Error, for example, error response on the AHB interface. This Bits is valid only when Bit 13 (FBI) is set. This Bits does not generate an interrupt. 0 0 0: Error during Rx DMA Write Data Transfer 0 1 1: Error during Tx DMA Read Data Transfer 1 0 0: Error during Rx DMA Descriptor Write Access 1 0 1: Error during Tx DMA Descriptor Write Access 1 1 0: Error during Rx DMA Descriptor Read Access 1 1 1: Error during Tx DMA Descriptor Read Access **Note:** 001 and 010 are reserved.	R
22:20	TS	Transmit Process State This Bits indicates the Transmit DMA FSM state. This Bits does not generate an interrupt. 3'b000: Stopped; Reset or Stop Transmit Command issued 3'b001: Running; Fetching Transmit Transfer Descriptor 3'b010: Running; Waiting for status 3'b011: Running; Reading Data from host memory buffer and queuing it to transmit buffer (Tx FIFO) 3'b100: Reserved for future use 3'b101: Reserved for future use 3'b110: Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow 3'b111: Running; Closing Transmit Descriptor	R
19:17	RS	Receive Process State This Bits indicates the Receive DMA FSM state. This Bits does not generate an interrupt. 3'b000: Stopped: Reset or Stop Receive Command issued 3'b001: Running: Fetching Receive Transfer Descriptor 3'b010: Reserved for future use 3'b011: Running: Waiting for receive packet 3'b100: Suspended: Receive Descriptor Unavailable 3'b101: Running: Closing Receive Descriptor 3'b110: TIME_STAMP write state 3'b111: Running: Transferring the receive packet data from receive buffer to host memory	R
16	NIS	Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): Register 5[0]: Transmit Interrupt Register 5[2]: Transmit Buffer Unavailable	RW[1]

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		Register 5[6]: Receive Interrupt Register 5[14]: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in Register 7) affect the Normal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes NIS to be set, is cleared.	
15	AIS	Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): Register 5[1]: Transmit Process Stopped Register 5[3]: Transmit Jabber Timeout Register 5[4]: Receive FIFO Overflow Register 5[5]: Transmit Underflow Register 5[7]: Receive Buffer Unavailable Register 5[8]: Receive Process Stopped Register 5[9]: Receive Watchdog Timeout Register 5[10]: Early Transmit Interrupt Register 5[13]: Fatal Bus Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.	RW[2]
14	ERI	Early Receive Interrupt This bit indicates that the DMA filled the first data buffer of the packet. This bit is cleared when the software writes 1 to this bit or Bit 6 (RI) of this register is set (whichever occurs earlier).	RW[3]
13	FBI	Fatal Bus Error Interrupt This bit indicates that a bus error occurred, as described in Bits [25:23]. When this bit is set, the corresponding DMA engine disables all of its bus accesses.	RW[4]
12:11	Reserved	Writing has no effect, read as zero.	R
10	ETI	Early Transmit Interrupt This bit indicates that the frame to be transmitted is fully transferred to the MTL Transmit FIFO.	RW[5]
9	RWT	Receive Watchdog Timeout When set, this bit indicates that the Receive Watchdog Timer expired while receiving the current frame and the current frame is truncated after the watchdog timeout.	RW[6]
8	RPS	Receive Process Stopped This bit is asserted when the Receive Process enters the Stopped	RW[7]

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		state.	
7	RU	Receive Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Receive List and the DMA cannot acquire it. The Receive Process is suspended. To resume processing Receive descriptors, the host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, the Receive Process resumes when the next recognized incoming frame is received. This bit is set only when the previous Receive Descriptor is owned by the DMA.	RW[8]
6	RI	Receive Interrupt This bit indicates that the frame reception is complete. When reception is complete, the Bit 31 of RDES1 (Disable Interrupt on Completion) is reset in the last Descriptor, and the specific frame status information is updated in the descriptor. The reception remains in the Running state.	RW[9]
5	UNF	Transmit Underflow This bit indicates that the Transmit Buffer had an Underflow during frame transmission. Transmission is suspended and an Underflow Error TDES0[1] is set.	RW[10]
4	OVF	Receive Overflow This bit indicates that the Receive Buffer had an Overflow during frame reception. If the partial frame is transferred to the application, the overflow status is set in RDES0[11].	RW[11]
3	TJT	Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired, which happens when the frame size exceeds 2,048 (10,240 bytes when the Jumbo frame is enabled). When the Jabber Timeout occurs, the transmission process is aborted and placed in the Stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert.	RW[12]
2	TU	Transmit Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Transmit List and the DMA cannot acquire it. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions. To resume processing Transmit descriptors, the host should change the ownership of the descriptor by setting TDES0[31] and then issue a Transmit Poll Demand command.	RW[13]
1	TPS	Transmit Process Stopped This bit is set when the transmission is stopped.	RW[14]
0	TI	Transmit Interrupt	RW[15]

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		This bit indicates that the frame transmission is complete. When transmission is complete, Bit 31 (OWN) of TDES0 is reset, and the specific frame status information is updated in the descriptor.	

Note:

1. Only support RMII mode
2. [1]~[15]:This bits will operate with Self set, read clear function.

27.7.2.7 DMA Operation Mode Register(DMA_OMR,0x1018)

	DMA_OMR																															Base + 0x1018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					DT	RSF	DFF	Reserved		TSF	FTF	Reserved				TTC		ST	RFD		RFA		EFC	FEF	FUF	DGF	RTC		OSF	SR	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:27	Reserved	Writing has no effect, read as zero.	R
26	DT	Disable Dropping of TCP/IP Checksum Error Frames When this bit is set, the MAC does not drop the frames which only have errors detected by the Receive Checksum Offload engine. Such frames do not have any errors (including FCS error) in the Ethernet frame received by the MAC but have errors only in the encapsulated payload. When this bit is reset, all error frames are dropped if the FEF bit is reset. If the IPC Full Checksum Offload Engine (Type 2) is disabled, this bit is reserved (RO with value 1'b0).	RW
25	RSF	Receive Store and Forward When this bit is set, the MTL reads a frame from the Rx FIFO only after the complete frame has been written to it, ignoring the RTC bits. When this bit is reset, the Rx FIFO operates in the cut-through mode, subject to the threshold specified by the RTC bits.	RW
24	DFF	Disable Flushing of Received Frames When this bit is set, the Rx DMA does not flush any frames because of the unavailability of receive descriptors or buffers as it does normally when this bit is reset.	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21	TSF	Transmit Store and Forward When this bit is set, transmission starts when a full frame resides in the MTL Transmit FIFO. When this bit is set, the TTC values	RW

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		specified in Bits [16:14] are ignored. This bit should be changed only when the transmission is stopped.	
20	FTF	Flush Transmit FIFO When this bit is set, the transmit FIFO controller logic is reset to its default values and thus all data in the Tx FIFO is lost or flushed. This bit is cleared internally when the flushing operation is complete. The Operation Mode register should not be written to until this bit is cleared. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt frame transmission. Note: The flush operation is complete only when the Tx FIFO is emptied of its contents and all the pending Transmit Status of the transmitted frames are accepted by the host. In order to complete this flush operation, the PHY transmit clock is required to be active.	RW[1]
19:17	Reserved	Writing has no effect, read as zero.	R
16:14	TTC	Transmit Threshold Control These bits control the threshold level of the MTL Transmit FIFO. Transmission starts when the frame size within the MTL Transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. These bits are used only when Bit 21 (TSF) is reset. ▪ 000: 64 ▪ 001: 128 ▪ 010: 192 ▪ 011: 256 ▪ 100: 40 ▪ 101: 32 ▪ 110: 24 ▪ 111: 16	RW
13	ST	Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state, and the DMA checks the Transmit List at the current position for a frame to be transmitted. Descriptor acquisition is attempted either from the current position in the list, which is the Transmit List Base Address set by Register 4 (Transmit Descriptor List Address Register), or from the position retained when transmission was stopped previously. If the DMA does not own the current descriptor, transmission enters the Suspended state and Bit 2 (Transmit Buffer Unavailable) of Register 5 (Status Register) is set. The Start Transmission command is effective only when transmission is stopped. If the command is issued before setting Register 4 (Transmit Descriptor	RW

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		List Address Register), then the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current frame. The Next Descriptor position in the Transmit List is saved, and it becomes the current position when transmission is restarted. To change the list address, you need to program Register 4 (Transmit Descriptor List Address Register) with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current frame is complete or the transmission is in the Suspended state.	
12:11	RFD	Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (Fill-level of Rx FIFO) at which the flow control is de-asserted after activation. ▪00: Full minus 1 KB, that is, FULL — 1 KB ■ 01: Full minus 2 KB, that is, FULL — 2 KB ■ 10: Full minus 3 KB, that is, FULL — 3 KB ■ 11: Full minus 4 KB, that is, FULL — 4 KB The de-assertion is effective only after flow control is asserted. If the Rx FIFO is 8 KB or more, an additional Bit (RFD_2) is used for more threshold levels as described in Bit 22. These bits are reserved and read-only when the Rx FIFO depth is less than 4 KB.	RW
10:9	RFA	Threshold for Activating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (Fill level of Rx FIFO) at which the flow control is activated. ▪00: Full minus 1 KB, that is, FULL—1KB. ▪01: Full minus 2 KB, that is, FULL—2KB. ▪10: Full minus 3 KB, that is, FULL—3KB. ▪11: Full minus 4 KB, that is, FULL—4KB. These values are applicable only to Rx FIFOs of 4 KB or more and when Bit 8 (EFC) is set high. If the Rx FIFO is 8 KB or more, an additional Bit (RFA_2) is used for more threshold levels as described in Bit 23. These bits are reserved and read-only when the depth of Rx FIFO is less than 4 KB.	RW
8	EFC	Enable HW Flow Control When this bit is set, the flow control signal operation based on the fill-level of Rx FIFO is enabled. When reset, the flow control operation is disabled. This bit is not used (reserved and always reset) when the Rx FIFO is less than 4 KB.	RW
7	FEF	Forward Error Frames When this bit is reset, the Rx FIFO drops frames with error status (CRC error, collision error, GMII_ER, giant frame, watchdog timeout, or overflow). However, if the start byte (write) pointer of a frame is already transferred to the read controller side (in Threshold mode), then the frame is not dropped. When the FEF bit is set, all frames except runt error frames are forwarded to the DMA. If the Bit 25 (RSF) is set and the Rx FIFO	RW

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		overflows when a partial frame is written, then the frame is dropped irrespective of the FEF bit setting. However, if the Bit 25 (RSF) is reset and the Rx FIFO overflows when a partial frame is written, then a partial frame may be forwarded to the DMA. **Note:** When FEF bit is reset, the giant frames are dropped if the giant frame status is given in Rx Status in the following configurations: The IP checksum engine (Type 1) and full checksum offload engine (Type 2) are not selected.	
6	FUF	Forward Undersized Good Frames When set, the Rx FIFO forwards Undersized frames (that is, frames with no Error and length less than 64 bytes) including pad-bytes and CRC. When reset, the Rx FIFO drops all frames of less than 64 bytes, unless a frame is already transferred because of the lower value of Receive Threshold, for example, RTC = 01.	RW
5	DGF	Drop Giant Frames When set, the MAC drops the received giant frames in the Rx FIFO, that is, frames that are larger than the computed giant frame limit. When reset, the MAC does not drop the giant frames in the Rx FIFO.	RW
4:3	RTC	Receive Threshold Control These two bits control the threshold level of the MTL Receive FIFO. Transfer (request) to DMA starts when the frame size within the MTL Receive FIFO is larger than the threshold. In addition, full frames with length less than the threshold are automatically transferred. The value of 11 is not applicable if the configured Receive FIFO size is 128 bytes. These bits are valid only when the RSF bit is zero, and are ignored when the RSF bit is set to 1. ▪ 00: 64 ▪ 01: 32 ▪ 10: 96 ▪ 11: 128	RW
2	OSF	Operate on Second Frame When this bit is set, it instructs the DMA to process the second frame of the Transmit data even before the status for the first frame is obtained.	RW
1	SR	Start or Stop Receive When this bit is set, the Receive process is placed in the Running state. The DMA attempts to acquire the descriptor from the Receive list and processes the incoming frames. The descriptor acquisition is attempted from the current position in the list, which is the	RW

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		address set by the Register 3 (Receive Descriptor List Address Register) or the position retained when the Receive process was previously stopped. If the DMA does not own the descriptor, reception is suspended and Bit 7 (Receive Buffer Unavailable) of Register 5 (Status Register) is set. The Start Receive command is effective only when the reception has stopped. If the command is issued before setting Register 3 (Receive Descriptor List Address Register), the DMA behavior is unpredictable. When this bit is cleared, the Rx DMA operation is stopped after the transfer of the current frame. The next descriptor position in the Receive list is saved and becomes the current position after the Receive process is restarted. The Stop Receive command is effective only when the Receive process is in either the Running (waiting for receive packet) or in the Suspended state. **Note:** For information about how to pause the transmission, see "Stopping and Starting Transmission".	
0	-	Reserved	R

Note:

Only support RMII mode

27.7.2.8 DMA Interrupt Enable Register(DMA_IER,0x101C)

	DMA_IER																															Base + 0x101C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															NIE	AIE	ERE	FBEE	Reserved		ETE	RWE	RSE	RUE	RIE	UNE	OVE	TJE	TUE	TSE	TIE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:17	Reserved	Writing has no effect, read as zero.	R
16	NIE	Normal Interrupt Summary Enable When this bit is set, normal interrupt summary is enabled. When this bit is reset, normal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): ▪ Register 5[0]: Transmit Interrupt ▪ Register 5[2]: Transmit Buffer Unavailable ▪ Register 5[6]: Receive Interrupt ▪ Register 5[14]: Early Receive Interrupt	RW
15	AIE	Abnormal Interrupt Summary Enable	RW

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		When this bit is set, abnormal interrupt summary is enabled. When this bit is reset, the abnormal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): ▪ Register 5[1]: Transmit Process Stopped ▪ Register 5[3]: Transmit Jabber Timeout ▪ Register 5[4]: Receive Overflow ▪ Register 5[5]: Transmit Underflow ▪ Register 5[7]: Receive Buffer Unavailable ▪ Register 5[8]: Receive Process Stopped ▪ Register 5[9]: Receive Watchdog Timeout ▪ Register 5[10]: Early Transmit Interrupt ▪ Register 5[13]: Fatal Bus Error	
14	ERE	Early Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Early Receive Interrupt is enabled. When this bit is reset, the Early Receive Interrupt is disabled.	RW
13	FBEE	Fatal Bus Error Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Fatal Bus Error Interrupt is enabled. When this bit is reset, the Fatal Bus Error Enable Interrupt is disabled.	RW
12:11	Reserved	Writing has no effect, read as zero.	R
10	ETE	Early Transmit Interrupt Enable When this bit is set with an Abnormal Interrupt Summary Enable (Bit 15), the Early Transmit Interrupt is enabled. When this bit is reset, the Early Transmit Interrupt is disabled.	RW
9	RWE	Receive Watchdog Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Watchdog Timeout Interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout Interrupt is disabled.	RW
8	RSE	Receive Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped Interrupt is disabled.	RW
7	RUE	Receive Buffer Unavailable Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable Interrupt is disabled.	RW
6	RIE	Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.	RW
5	UNE	Underflow Interrupt Enable	RW

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		When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Underflow Interrupt is enabled. When this bit is reset, the Underflow Interrupt is disabled.	
4	OVE	Overflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Overflow Interrupt is enabled. When this bit is reset, the Overflow Interrupt is disabled.	RW
3	TJE	Transmit Jabber Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Jabber Timeout Interrupt is enabled. When this bit is reset, the Transmit Jabber Timeout Interrupt is disabled.	RW
2	TUE	Transmit Buffer Unavailable Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable Interrupt is disabled.	RW
1	TSE	Transmit Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmission Stopped Interrupt is enabled. When this bit is reset, the Transmission Stopped Interrupt is disabled.	RW
0	TIE	Transmit Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled.	RW

Note:

Only support RMII mode

27.7.2.9 DMA Missed Frame and Buffer Overflow Counter Register(DMA_MFOCR,0x1020)

	DMA_MFOCR																															Base + 0x1020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			OVFCNTOVF	MISCNTOVF											MISCNTOVF	MISFRMCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:29	Reserved	Writing has no effect, read as zero.	R
28	OVFCNTOVF	Overflow Bit for FIFO Overflow Counter This bit is set every time the Overflow Frame Counter (Bits[27:17])	RC[1]

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		overflows, that is, the Rx FIFO overflows with the overflow frame counter at maximum value. In such a scenario, the overflow frame counter is reset to all-zeros and this bit indicates that the rollover happened.	
27:17	OVFFRMCNT	Overflow Frame Counter This Bits indicates the number of frames missed by the application. This counter is incremented each time the MTL FIFO overflows. The counter is cleared when this register is read with mci_be_i[2] at 1'b1.	RC[2]
16	MISCNTOVF	Overflow Bit for Missed Frame Counter This bit is set every time Missed Frame Counter (Bits[15:0]) overflows, that is, the DMA discards an incoming frame because of the Host Receive Buffer being unavailable with the missed frame counter at maximum value. In such a scenario, the Missed frame counter is reset to all-zeros and this bit indicates that the rollover happened.	RC[3]
15:0	MISFRMCNT	Missed Frame Counter This Bits indicates the number of frames missed by the controller because of the Host Receive Buffer being unavailable. This counter is incremented each time the DMA discards an incoming frame. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.	RC[4]

Note:1. Only support RMII mode

2. [1]~[4]:This bits will operate with Self set, read clear function.

27.7.2.10 DMA Receive Interrupt Watchdog Timer Register(DMA_RIWTR,0x1024)

	DMA_BMR																															Base + 0x1024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								RIWT							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	RIWT	RI Watchdog Timer Count This bit indicates the number of system clock cycles multiplied by 256 for which the watchdog timer is set. The watchdog timer gets triggered with the programmed value after the Rx DMA completes	RW

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		the transfer of a frame for which the RI status bit is not set because of the setting in the corresponding descriptor RDES1[31]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per RDES1[31] of any received frame.	

Note:Only support RMII mode

27.7.2.11 DMA AHB State Register(DMA_AHBSR,0x102C)

	DMA_AHBSR																															Base + 0x102C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															AXWHSTS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	AXWHSTS	AHB Master Status	R

Note:Only support RMII mode

27.7.2.12 MAC Configuration Register(MAC_CR,0x0000)

	MAC_CR																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SARC			TWOKPE	Reserved	CST	TC	WD	JD	BE	JE	IFG			DCRS	PS	FES	DO	LM	DM	IPC	DR	LUD	ACS	BL		DC	TE	RE	PRELEN	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	Reserved	Writing has no effect, read as zero.	R
30:28	SARC	Source Address Insertion or Replacement Control This Bits controls the source address insertion or replacement for all transmitted frames. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits [29:28]:	RW

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		2'b0*x*: The input signals mti_sa_ctrl_i and ati_sa_ctrl_i control the SA Bits generation. 2'b10: If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers (registers 16 and 17) in the SA Bits of all transmitted frames. If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected during core configuration, the MAC inserts the content of the MAC Address 1 registers (registers 18 and 19) in the SA Bits of all transmitted frames. 2'b11: If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers (registers 16 and 17) in the SA Bits of all transmitted frames. If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected during core configuration, the MAC replaces the content of the MAC Address 1 registers (registers 18 and 19) in the SA Bits of all transmitted frames. **Note:** Changes to this Bits take effect only on the start of a frame. If you write this register Bits when a frame is being transmitted, only the subsequent frame can use the updated value, that is, the current frame does not use the updated value. These bits are reserved and RO when the Enable SA, VLAN, and CRC Insertion on TX feature is not selected during core configuration.	
27	TWOKPE	IEEE 802.3as Support for 2K Packets When set, the MAC considers all frames, with up to 2,000 bytes length, as normal packets. When Bit 20 (JE) is not set, the MAC considers all received frames of size more than 2K bytes as Giant frames. When this bit is reset and Bit 20 (JE) is not set, the MAC considers all received frames of size more than 1,518 bytes (1,522 bytes for tagged) as Giant frames. When Bit 20 is set, setting this bit has no effect on Giant Frame status. For more information about how the setting of this bit and Bit 20 impact the Giant frame status.	RW
26	Reserved	Writing has no effect, read as zero.	RW
25	CST	CRC Stripping for Type Frames When this bit is set, the last 4 bytes (FCS) of all frames of Ether type (Length/Type Bits greater than or equal to 1,536) are stripped and dropped before forwarding the frame to the application. This function is not valid when the IP Checksum Engine (Type 1) is enabled in the MAC receiver. This function is valid when Type 2 Checksum Offload Engine is enabled. **Note:** For information about how the settings of Bit 7 (ACS) and this	RW

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		bit impact the frame length.	
24	TC	Transmit Configuration in RGMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMI port. When this bit is reset, no such information is driven to the PHY.	RW
23	WD	Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive frames of up to 16,384 bytes. When this bit is reset, the MAC does not allow a receive frame which more than 2,048 bytes (10,240 if JE is set high) or the value programmed in Register 55 (Watchdog Timeout Register). The MAC cuts off any bytes received after the watchdog limit number of bytes.	RW
22	JD	Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer frames of up to 16,384 bytes. When this bit is reset, the MAC cuts off the transmitter if the application sends out more than 2,048 bytes of data (10,240 if JE is set high) during transmission.	RW
21	BE	Frame Burst Enable When this bit is set, the MAC allows frame bursting during transmission in the GMII half-duplex mode. This bit is reserved (and RO) in the 10/100 Mbps only or full-duplex-only configurations.	RW
20	JE	Jumbo Frame Enable When this bit is set, the MAC allows Jumbo frames of 9,018 bytes (9,022 bytes for VLAN tagged frames) without reporting a giant frame error in the receive frame status.	RW
19:17	IFG	Inter-Frame Gap These bits control the minimum IFG between frames during transmission. 000: 96 bit times 001: 88 bit times 010: 80 bit times ... 111: 40 bit times In the half-duplex mode, the minimum IFG can be configured only for 64 bit times (IFG = 100). Lower values are not considered. In the 1000-Mbps mode, the minimum IFG supported is 80 bit times.	RW
16	DCRS	Disable Carrier Sense During Transmission When set high, this bit makes the MAC transmitter ignore the (G)MII CRS signal during frame transmission in the half-duplex mode. This request results in no errors generated because of Loss of Carrier or No Carrier during such transmission. When this bit is low, the MAC	RW

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		transmitter generates such errors because of Carrier Sense and can even abort the transmissions. This bit is reserved (and RO) in the full-duplex-only configurations.	
15	PS	Port Select This bit selects the Ethernet line speed. 0: For 1000 Mbps operations 1: For 10 or 100 Mbps operations In 10 or 100 Mbps operations, this bit, along with FES bit, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only with the appropriate value. In default 10/100/1000 Mbps configuration, this bit is R_W.	RW
14	FES	Speed This bit selects the speed in the MII, RMII, RGMII or GMII interface: 0: 10 Mbps 1: 100 Mbps	RW
13	DO	Disable Receive Own When this bit is set, the MAC disables the reception of frames when the TXEN is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets that are given by the PHY while transmitting. This bit is not applicable if the MAC is operating in the full-duplex mode. This bit is reserved (RO with default value) if the MAC is configured for the full-duplex-only operation.	RW
12	LM	Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Receive clock input (RX_CLK) is required for the loopback to work properly, because the Transmit clock is not looped-back internally.	RW
11	DM	Duplex Mode When this bit is set, the MAC operates in the full-duplex mode where it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configuration.	RW
10	IPC	Checksum Offload When this bit is set, the MAC calculates the 16-bit one's complement of the one's complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 Header checksum (assumed to be bytes 25-26 or 29-30 (VLAN- tagged) of the received Ethernet frame) is correct for the received frame and gives the status in the receive status word. The MAC also appends the 16-bit checksum calculated for the IP header datagram payload (bytes after the IPv4 header) and appends it to the Ethernet frame transferred to the application (when Type 2 COE is deselected).	RW

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		When this bit is reset, this function is disabled. When Type 2 COE is selected, this bit, when set, enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled and the corresponding PCE and IP HCE status bits are always cleared.	
9	DR	Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current frame transmission and reports a Frame Abort with excessive collision error in the transmit frame status. When this bit is reset, the MAC attempts retries based on the settings of the BL Bits (Bits [6:5]). This bit is applicable only in the half-duplex mode and is reserved (RO with default value) in the full-duplex-only configuration.	RW
8	LUD	Link Up or Down This bit indicates whether the link is up or down during the transmission of configuration in the RGMI: 0: Link Down 1: Link Up	RW
7	ACS	Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS Bits on the incoming frames only if the value of the length Bits is less than 1,536 bytes. All received frames with length Bits greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS Bits. When this bit is reset, the MAC passes all incoming frames, without modifying them, to the Host. **Note:** For information about how the settings of Bit 23 (CST) and this bit impact the frame length.	RW
6:5	BL	Back-Off Limit The Back-Off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps and 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. This bit is applicable only in the half-duplex mode and is reserved (RO) in the full-duplex-only configuration. 00: k= min (n, 10) 01: k = min (n, 8) 10: k = min (n, 4) 11: k = min (n, 1) where n = retransmission attempt. The random integer r takes the value in the range $0 \leq r < 2^k$	RW

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4	DC	Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Frame Abort status, along with the excessive deferral error bit set in the transmit frame status, when the transmit state machine is deferred for more than 24,288 bit times in the 10 or 100 Mbps mode. If the MAC is configured for 1000 Mbps operation or if the Jumbo frame mode is enabled in the 10 or 100 Mbps mode, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and then the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0 and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode and is reserved (RO) in the full-duplex-only configuration.	RW
3	TE	Transmitter Enable When this bit is set, the transmit state machine of the MAC is enabled for transmission on the GMII or MII. When this bit is reset, the MAC transmit state machine is disabled after the completion of the transmission of the current frame, and does not transmit any further frames.	RW
2	RE	Receiver Enable When this bit is set, the receiver state machine of the MAC is enabled for receiving frames from the GMII or MII. When this bit is reset, the MAC receive state machine is disabled after the completion of the reception of the current frame, and does not receive any further frames from the GMII or MII.	RW
1:0	PRELEN	Preamble Length for Transmit frames These bits control the number of preamble bytes that are added to the beginning of every Transmit frame. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 2'b00: 7 bytes of preamble 2'b01: 5 bytes of preamble 2'b10: 3 bytes of preamble 2'b11: Reserved	RW

Note:Only support RMII mode

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27.7.2.13 MAC Frame Filter Register(MAC_FFR,0x0004)

	MAC_FFR																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RA	Reserved														VTFE	Reserved					HPF	SAF	SAIF	PCF		DBF	PM	DAIF	HMC	HUC	PR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	RA	Receive All When this bit is set, the MAC Receiver module passes all received frames, irrespective of whether they pass the address filter or not, to the Application. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word. When this bit is reset, the Receiver module passes only those frames to the Application that pass the SA or DA address filter.	RW
30:17	Reserved	Writing has no effect, read as zero.	R
16	VTFE	VLAN Tag Filter Enable When set, this bit enables the MAC to drop VLAN tagged frames that do not match the VLAN Tag comparison. When reset, the MAC forwards all frames irrespective of the match status of the VLAN Tag.	RW
15:11	Reserved	Writing has no effect, read as zero.	RW
10	HPF	Hash or Perfect Filter When this bit is set, it configures the address filter to pass a frame if it matches either the perfect filtering or the hash filtering as set by the HMC or HUC bits. When this bit is low and the HUC or HMC bit is set, the frame is passed only if it matches the Hash filter.	RW
9	SAF	Source Address Filter Enable When this bit is set, the MAC compares the SA Bits of the received frames with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the frame. When this bit is reset, the MAC forwards the received frame to the application with updated SAF bit of the Rx Status depending on the SA address comparison. **Note:** According to the IEEE specification, Bit 47 of the SA is reserved and set to 0. However, in gmac, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA.	RW
8	SAIF	SA Inverse Filtering	RW

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		When this bit is set, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers are marked as failing the SA Address filter. When this bit is reset, frames whose SA does not match the SA registers are marked as failing the SA Address filter.	
7:6	PCF	Pass Control Frames These bits control the forwarding of all control frames (including unicast and multicast Pause frames). 00: MAC filters all control frames from reaching the application. 01: MAC forwards all control frames except Pause frames to application even if they fail the Address filter. 10: MAC forwards all control frames to application even if they fail the Address Filter. 11: MAC forwards control frames that pass the Address Filter. The following conditions should be true for the Pause frames processing: Condition 1: The MAC is in the full-duplex mode and flow control is enabled by setting Bit 2 (RFE) of Register 6 (Flow Control Register) to 1. Condition 2: The destination address (DA) of the received frame matches the special multicast address or the MAC Address 0 when Bit 3 (UP) of the Register 6 (Flow Control Register) is set. Condition 3: The Type Bits of the received frame is 0x8808 and the OPCODE Bits is 0x0001. **Note:** This Bits should be set to 01 only when the Condition 1 is true, that is, the MAC is programmed to operate in the full-duplex mode and the RFE bit is enabled. Otherwise, the Pause frame filtering may be inconsistent. When Condition 1 is false, the Pause frames are considered as generic control frames. Therefore, to pass all control frames (including Pause frames) when the full-duplex mode and flow control is not enabled, you should set the PCF Bits to 10 or 11 (as required by the application).	RW
5	DBF	Disable Broadcast Frames When this bit is set, the AFM module blocks all incoming broadcast frames. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast frames.	RW
4	PM	Pass All Multicast When set, this bit indicates that all received frames with a multicast destination address (first bit in the destination address Bits is '1') are passed. When reset, filtering of multicast frame depends on HMC bit.	RW
3	DAIF	DA Inverse Filtering	RW

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		When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast frames. When reset, normal filtering of frames is performed.	
2	HMC	Hash Multicast When set, MAC performs destination address filtering of received multicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for multicast frames, that is, it compares the DA Bits with the values programmed in DA registers.	RW
1	HUC	Hash Unicast When set, MAC performs destination address filtering of unicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for unicast frames, that is, it compares the DA Bits with the values programmed in DA registers.	RW
0	PR	Promiscuous Mode When this bit is set, the Address Filter module passes all incoming frames irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Receive Status Word are always cleared when PR is set.	RW

Note:

Only support RMII mode

27.7.2.14 MAC Hash Table High Register(MAC_HTHR,0x0008)

	MAC_HTHR																																Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HTH																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	HTH	Hash Table High This Bits contains the upper 32 bits of the Hash table.	RW

Note:

Only support RMII mode

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27.7.2.15 MAC Hash Table Low Register(MAC_HTLR,0x000C)

	MAC_HTLR																															Base + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HTL																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	HTL	Hash Table Low This Bits contains the lower 32 bits of the Hash table.	RW

Note:

Only support RMII mode

27.7.2.16 GMII Address Register(GMII_AR,0x0010)

	GMII_AR																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PA					GR					CR				GW	GB
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:11	PA	Physical Layer Address This Bits indicates which of the 32 possible PHY devices are being accessed.	RW
10:6	GR	GMII Register These bits select the desired GMII register in the selected PHY device.	RW
5:2	CR	CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design. The suggested range of CSR clock frequency applicable for each value (when Bit[5] = 0) ensures that the MDC clock is approximately between the frequency range	RW

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		1.0 MHz-2.5 MHz. 0000: The CSR clock frequency is 60-100 MHz and the MDC clock frequency is CSR clock/42. 0001: The CSR clock frequency is 100-150 MHz and the MDC clock frequency is CSR clock/62. 0010: The CSR clock frequency is 20-35 MHz and the MDC clock frequency is CSR clock/16. 0011: The CSR clock frequency is 35-60 MHz and the MDC clock frequency is CSR clock/26. 0100: The CSR clock frequency is 150-250 MHz and the MDC clock frequency is CSR clock/102. 0101: The CSR clock frequency is 250-300 MHz and the MDC clock is CSR clock/124. 0110, 0111: Reserved When Bit 5 is set, you can achieve higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE Std 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, then the resultant MDC clock is of 12.5 MHz which is outside the limit of IEEE 802.3 specified range. Program the following values only if the interfacing chips support faster MDC clocks. 1000: CSR clock/4 1001: CSR clock/6 1010: CSR clock/8 1011: CSR clock/10 1100: CSR clock/12 1101: CSR clock/14 1110: CSR clock/16 1111: CSR clock/18	
1	GW	GMII Write When set, this bit indicates to the PHY that this is a Write operation using the GMII Data register. If this bit is not set, it indicates that this is a Read operation, that is, placing the data in the GMII Data register.	RW
0	GB	GMII Busy This bit should read logic 0 before writing to Register 4 and Register 5. During a PHY or RevMII register access, the software sets this bit to 1'b1 to indicate that a Read or Write access is in progress. Register 5 is invalid until this bit is cleared by the MAC. Therefore, Register 5 (GMII Data) should be kept valid until the MAC clears this bit during a PHY Write operation. Similarly for a read	RW[1]

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		operation, the contents of Register 5 are not valid until this bit is cleared. The subsequent read or write operation should happen only after the previous operation is complete. Because there is no acknowledgment from the PHY to MAC after a read or write operation is completed, there is no change in the functionality of this bit even when the PHY is not present.	

Note:1. Only support RMII mode

2. [1]:This bits will operate with Write set, read clear function.

27.7.2.17 GMII Data Register(GMII_DR,0x0014)

	GNII_DR																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																GD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	GD	GMII Data This Bits contains the 16-bit data value read from the PHY after a Management Read operation or the 16-bit data value to be written to the PHY before a Management Write operation.	RW

Note:

Only support RMII mode

27.7.2.18 MAC Flow Control Register(MAC_FCR,0x0018)

	MAC_FCR																															Base+ 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PT																Reserved								DZPQ	Reserved	PLT		UP	RFE	TFE	FCP/PBA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	PT	Pause Time	RW

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6		This Bits holds the value to be used in the Pause Time Bits in the transmit control frame. If the Pause Time bits is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.	
15:8	Reserved	Writing has no effect, read as zero.	R
7	DZPQ	Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the Zero-Quanta Pause frames on the de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i/mti_flowctrl_i). When this bit is reset, normal operation with automatic Zero-Quanta Pause frame generation is enabled.	RW
6	Reserved	Writing has no effect, read as zero.	R
5:4	PLT	Pause Low Threshold This Bits configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause frame. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot-times), and PLT = 01, then a second Pause frame is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256 - 28) slot times after the first Pause frame is transmitted. The following list provides the threshold values for different values: 00: The threshold is Pause time minus 4 slot times (PT - 4 slot times). 01: The threshold is Pause time minus 28 slot times (PT - 28 slot times). 10: The threshold is Pause time minus 144 slot times (PT - 144 slot times). 11: The threshold is Pause time minus 256 slot times (PT - 256 slot times). The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface.	RW
3	UP	Unicast Pause Frame Detect A pause frame is processed when it has the unique multicast address specified in the IEEE Std 802.3. When this bit is set, the MAC can also detect Pause frames with unicast address of the station. This unicast address should be as specified in the MAC Address0 High Register and MAC Address0 Low Register.	RW

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		When this bit is reset, the MAC only detects Pause frames with unique multicast address. **Note:** The MAC does not process a Pause frame if the multicast address of received frame is different from the unique multicast address.	
2	RFE	Receive Flow Control Enable When this bit is set, the MAC decodes the received Pause frame and disables its transmitter for a specified (Pause) time. When this bit is reset, the decode function of the Pause frame is disabled.	RW
1	TFE	Transmit Flow Control Enable In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to transmit Pause frames. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause frames. In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled.	RW
0	FCB_BPA	Flow Control Busy or Backpressure Activate This bit initiates a Pause frame in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. In the full-duplex mode, this bit should be read as 1'b0 before writing to the Flow Control register. To initiate a Pause frame, the Application must set this bit to 1'b1. During a transfer of the Control Frame, this bit continues to be set to signify that a frame transmission is in progress. After the completion of Pause frame transmission, the MAC resets this bit to 1'b0. The Flow Control register should not be written to until this bit is cleared. In the half-duplex mode, when this bit is set (and TFE is set), then backpressure is asserted by the MAC. During backpressure, when the MAC receives a new frame, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled.	RW

Note:

Only support RMII mode

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27.7.2.19 MAC VLAN Tag Register(MAC_VTR,0x001C)

	MAC_VTR																															Base + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												VTHM	ESVL	VTIM	ETV	VL															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	Reserved	Writing has no effect, read as zero.	R
19	VTHM	VLAN Tag Hash Table Match Enable When set, the most significant four bits of the VLAN tag's CRC are used to index the content of Register 354 (VLAN Hash Table Register). A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the frame matched the VLAN hash table. When Bit 16 (ETV) is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison whereas when ETV is reset, the CRC of the 16-bit VLAN tag is used for comparison. When reset, the VLAN Hash Match operation is not performed.	RW
18	ESVL	nable S-VLAN When this bit is set, the MAC transmitter and receiver also consider the S-VLAN (Type = 0x88A8) frames as valid VLAN tagged frames.	RW
17	VTIM	VLAN Tag Inverse Match Enable When set, this bit enables the VLAN Tag inverse matching. The frames that do not have matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The frames with matched VLAN Tag are marked as matched.	RW
16	ETV	Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding Bits in the received VLAN-tagged frame. Similarly, when enabled, only 12 bits of the VLAN tag in the received frame are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN frame are used for comparison and VLAN hash filtering.	RW

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15:0	VL	VLAN Tag Identifier for Receive Frames This Bits contains the 802.1Q VLAN tag to identify the VLAN frames and is compared to the 15th and 16th bytes of the frames being received for VLAN frames. The following list describes the bits of this Bits: Bits [15:13]: User Priority Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) Bits[11:0]: VLAN tag's VLAN Identifier (VID) Bits When the ETV bit is set, only the VID (Bits[11:0]) is used for comparison. If VL (VL[11:0] if ETV is set) is all zeros, the MAC does not check the fifteenth and 16th bytes for VLAN tag comparison, and declares all frames with a Type Bits value of 0x8100 or 0x88a8 as VLAN frames.	RW

Note:Only support RMII mode

27.7.2.20 MAC Debug Register(MAC_DR,0x0024)

	MAC_DR																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							TXFSTS	Reserved	TWCST	TRCSTS		TXPAUSED	TFCSTS		TPESTS	Reserved						RXFSTS		Reserved	RPCSTS		RWCSTS	Reserved	RFCFCSTS	RPESTS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:25	Reserved	Writing has no effect, read as zero.	R
24	TXFSTS	MTL Tx FIFO Not Empty Status When high, this bit indicates that the MTL Tx FIFO is not empty and some data is left for transmission.	R
23	Reserved	Writing has no effect, read as zero.	R
22	TWCSTS	MTL Tx FIFO Write Controller Status When high, this bit indicates that the MTL Tx FIFO Write Controller is active and is transferring data to the Tx FIFO.	R
21:20	TRCSTS	MTL Tx FIFO Read Controller Status This Bits indicates the state of the Tx FIFO Read Controller: ▪ 00: IDLE state ▪ 01: READ state (transferring data to the MAC transmitter) ▪ 10: Waiting for Tx Status from the MAC transmitter	R

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		▪ 11: Writing the received Tx Status or flushing the Tx FIFO	
19	TXPAUSED	MAC Transmitter in Pause When high, this bit indicates that the MAC transmitter is in the Pause condition (in the full-duplex-only mode) and hence does not schedule any frame for transmission.	R
18:17	TFCSTS	MAC Transmit Frame Controller Status This Bits indicates the state of the MAC Transmit Frame Controller module: 00: IDLE state 01: Waiting for status of previous frame or IFG or backoff period to be over 10: Generating and transmitting a Pause frame (in the full-duplex mode) 11: Transferring input frame for transmission	R
16	TPESTS	MAC GMII or MII Transmit Protocol Engine Status When high, this bit indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data and is not in the IDLE state.	R
15:10	Reserved	Writing has no effect, read as zero.	R
9:8	RXFSTS	MTL Rx FIFO Fill-Level Status This Bits gives the status of the fill-level of the Rx FIFO: ▪ 00: Rx FIFO Empty ▪ 01: Rx FIFO fill-level below flow-control deactivate threshold ▪ 10: Rx FIFO fill-level above flow-control activate threshold ▪ 11: Rx FIFO Full	R
7	Reserved	Writing has no effect, read as zero.	R
6:5	RRCSTS	MTL Rx FIFO Read Controller State This Bits gives the state of the Rx FIFO read Controller: ▪ 00: IDLE state ▪ 01: Reading frame data ▪ 10: Reading frame status ▪ 11: Flushing the frame data and status	R
4	RWCSTS	MTL Rx FIFO Write Controller Active Status When high, this bit indicates that the MTL Rx FIFO Write Controller is active and is transferring a received frame to the FIFO.	R
3	Reserved	Writing has no effect, read as zero.	R
2:1	RFCFCSTS	MAC Receive Frame FIFO Controller Status When high, this Bits indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Frame Controller Module.	R
0	RPESTS	MAC GMII or MII Receive Protocol Engine Status When high, this bit indicates that the MAC GMII or MII receive	R

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		protocol engine is actively receiving data and not in IDLE state.	

Note:

Only support RMII mode

27.7.2.21 LPI Control and Status Register(LPI_CSR,0x0030)

	LPI_CSR																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												LPITXA	PLSEN	PLS	LPIEN	Reserved						RLPIST	TLPIST	Reserved				RLPIES	RLPIEN	TLPIES	TLPIEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	Reserved	Writing has no effect, read as zero.	R
19	LPITXA	LPI TX Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the transmit side. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding frames (in the core) and pending frames (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any frame for transmission or the application issues a TX FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If TX FIFO Flush is set in Bit 20 of Register 6 (Operation Mode Register), when the MAC is in the LPI mode, the MAC exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode.	R
18	PLSEN	PHY Link Status Enable This bit enables the link status received on the RGMII receive paths to be used for activating the LPILS TIMER. When set, the MAC uses the link-status bits of Register 54 (RGMII Control and Status Register) and Bit 17 (PLS) for the LPI LS Timer trigger. When cleared, the MAC ignores the link-status bits of Register 54 and takes only the PLS bit.	RW
17	PLS	PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (okay) at least for the time indicated by the LPI LS TIMER.	RW

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		When set, the link is considered to be okay (up) and when reset, the link is considered to be down.	
16	LPIEN	LPI Enable When set, this bit instructs the MAC Transmitter to enter the LPI state. When reset, this bit instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission.	RW[1]
15:10	Reserved	Writing has no effect, read as zero.	R
9	RLPIST	Receive LPI State When set, this bit indicates that the MAC is receiving the LPI pattern on the GMII or MII interface.	R
8	TLPIST	Transmit LPI State When set, this bit indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface.	R
7:4	Reserved	Writing has no effect, read as zero.	R
3	RLPIEX	Receive LPI Exit When set, this bit indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register. **Note:** This bit may not get set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than 3 clock cycles of HCLK clock.	R[2]
2	RLPIEN	Receive LPI Entry When set, this bit indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register. **Note:** This bit may not get set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than 3 clock cycles of HCLK clock.	R[3]
1	TLPIEX	Transmit LPI Exit When set, this bit indicates that the MAC transmitter has exited the LPI state after the user has cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register.	R[4]
0	TLPIEN	Transmit LPI Entry When set, this bit indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register.	R[5]

Note:

1. Only support RMII mode
2. [1]:This bits will operate with Self clear function.

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3. [2]~[5]: This bits will operate with Self set , read clear function.

27.7.2.22 LPI Timers Control Register(LPI_TCR,0x0034)

	LPI_TCR																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						LST										TWT															
RST	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	LST	LPI LS TIMER This Bits specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.	RW
15:0	TWT	LPI TW TIMER This Bits specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.	RW

Note:

Only support RMII mode

27.7.2.23 MAC Interrupt Status Register(MAC_ISR,0x0038)

	MAC_ISR																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				GPIIS	LPIIS	Reserved		MMCRXIPIS	MMCTXIS	MMCRXIS	MMCIS	PMTIS	Reserved		RGMII
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11	GPIIS	GPI Interrupt Status When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS Bits (Bits [3:0]) of Register 56 (General Purpose IO Register) and the corresponding GPIE bit is enabled. This bit is cleared on reading lane 0 (GPIS) of Register 56 (General Purpose IO Register). When the GPIO feature is not enabled, this bit is reserved.	R
10	LPIIS	LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared on reading Bit 0 of Register 12 (LPI Control and Status Register). In all other modes, this bit is reserved.	R
9:8	Reserved	Writing has no effect, read as zero.	R
7	MMCRXIPIS	MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.	R
6	MMCTXIS	MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.	R
5	MMCRXIS	MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.	R
4	MMCIS	MMC Interrupt Status This bit is set high when any of the Bits [7:5] is set high and cleared only when all of these bits are low.	R
3	PMTIS	PMT Interrupt Status This bit is set when a magic packet or remote wake-up frame is received in the power-down mode (see Bits 5 and 6 in the PMT Control and Status Register). This bit is cleared when both Bits[6:5] are cleared because of a read operation to the PMT Control and Status register.	R
2:1	Reserved	Writing has no effect, read as zero.	R
0	RGMII	RGMII Interrupt Status This bit is set because of any change in value of the Link	R

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		Status of RGMII interface.	

Note:

Only support RMII mode

27.7.2.24 MAC Interrupt Mask Register(MAC_IMR,0x003C)

	MAC_IMR																															Base + 0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					LPIIM	Reserved						PMTIM	PCSANCIM	PCSLCHGIM	RGMII
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:11	Reserved	Writing has no effect, read as zero.	R
10	LPIIM	LPI Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the LPI Interrupt Status bit in Register 14 (Interrupt Status Register).	RW
9:4	Reserved	Writing has no effect, read as zero.	R
3	PMTIM	PMT Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PMT Interrupt Status bit in Register 14 (Interrupt Status Register).	RW
2	PCSANCIM	PCS AN Completion Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PCS Auto-negotiation complete bit in Register 14 (Interrupt Status Register).	RW
1	PCSLCHGIM	PCS Link Status Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the PCS Link-status changed bit in Register 14 (Interrupt Status Register).	RW
0	RGMII	RGMII Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the RGMII Interrupt Status bit in Register 14 (Interrupt Status Register).	RW

27.7.2.25 MAC Address0 High Register(MAC_A0HR,0x0040)

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	MAC_A0HR																															Base + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AE	Reserved															ADDRHI															
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31	AE	Address Enable This bit is always set to 1.	R
30:16	Reserved	Writing has no effect, read as zero.	R
15:0	ADDRHI	MAC Address0 [47:32] This Bits contains the upper 16 bits (47:32) of the first 6-byte MAC address. The MAC uses this Bits for filtering the received frames and inserting the MAC address in the Transmit Flow Control (Pause) Frames.	RW

Note:

Only support RMII mode

27.7.2.26 MAC Address0 LOW Register(MAC_A0LR,0x0044)

	MAC_A0LR																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDRLO																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31:0	ADDRLO	MAC Address0 [31:0] This Bits contains the lower 32 bits of the first 6-byte MAC address. This is used by the MAC for filtering the received frames and inserting the MAC address in the Transmit Flow Control (Pause) Frames.	RW

Note:

Only support RMII mode

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27.7.2.27 MAC Address1 High Register(MAC_A1HR,0x0048)

	MAC_A1HR																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AE	SA	MBC						Reserved								ADDRHI															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31	AE	Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.	RW
30	SA	Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA bits of the received frame. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA Bits of the received frame.	RW
29:24	MBC	Mask Byte Control These bits are mask control bits for comparison of each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29: Register 18[15:8] Bit 28: Register 18[7:0] Bit 27: Register 19[31:24] ... Bit 24: Register 19[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.	RW
23:16	Reserved	Writing has no effect, read as zero.	R
15:0	ADDRHI	MAC Address1 [47:32] This Bits contains the upper 16 bits (47:32) of the second 6-byte MAC address.	RW

Note:

Only support RMII mode

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27.7.2.28 MAC Address1 LOW Register(MAC_A1LR,0x004C)

	MAC_A1LR																															Base + 0x004C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDRLO																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31:0	ADDRLO	MAC Address1 [31:0] This Bits contains the lower 32 bits of the second 6-byte MAC address. The content of this Bits is undefined until loaded by the Application after the initialization process.	RW

Note: Only support RMII mode

27.7.2.29 MAC Watchdog Timeout Register(MAC_WTR,0x00DC)

	MAC_WTR																															Base + 0x00DC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															PWE	Reserved		WTO													
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:17	Reserved	Writing has no effect, read as zero.	R
16	PWE	Programmable Watchdog Enable When this bit is set and Bit 23 (WD) of Register 0 (MAC Configuration Register) is reset, the WTO Bits (Bits[13:0]) is used as watchdog timeout for a received frame. When this bit is cleared, the watchdog timeout for a received frame is controlled by the setting of Bit 23 (WD) and Bit 20 (JE) in Register 0 (MAC Configuration Register).	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:0	WTO	Watchdog Timeout When Bit 16 (PWE) is set and Bit 23 (WD) of Register 0 (MAC Configuration Register) is reset, this Bits is used as watchdog	RW

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		timeout for a received frame. If the length of a received frame exceeds the value of this Bits, such frame is terminated and declared as an error frame. **Note:** When Bit 16 (PWE) is set, the value in this Bits should be more than 1,522 (0x05F2). Otherwise, the IEEE Std 802.3-specified valid tagged frames are declared as error frames and are dropped.	

Note:

Only support RMII mode

27.8 Operation Flow

Figure 27-2 GMAC configure flow

Note: Only support RMII mode

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28 MIPI_CSI Interface

28.1 Overview

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 Specification, providing an interface between the System and the MIPI D-PHY, allowing the communication with a MIPI CSI-2 compliant Camera Sensor.

28.2 Features

- Support up to 2 D-PHY Rx Data Lanes
- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2)
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- 32-bit Image Data
- Support all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
- Error detection and correction
- Support up to 2 LVDS serial output lanes
- Support 6 multiplex pads with dvp

28.3 Block Diagram

Figure 28-1 MIPI_CSI Block Diagram

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28.4 Functional Description

The MIPI CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 Specification, providing an interface between the System and the MIPI D-PHY, allowing the communication with a MIPI CSI-2 compliant Camera Sensor.

28.5 Output Data Format Description

- RAW8

The RAW8 data format follows the generic CSI-2 rule. It is described in Table 28-1.

Table 28-1 RAW8 Data Format Reception

MSB																															LSB
P4								P3								P2								P1							
d7	d6	d5	d4	d3	d2	d1	d0	c7	c6	c5	c4	c3	c2	c1	c0	b7	b6	b5	b4	b3	b2	b1	b0	a7	a6	a5	a4	a3	a2	a1	a0

- RAW10

The RAW10 data format follows the generic CSI-2 rule. It is described in Table 28-2.

Table 28-2 RAW10 Data Format Reception

MSB																															LSB
P4[9:2]								P3[9:2]								P2[9:2]								P1[9:2]							
c8	c7	c6	c6	c5	c4	c3	c2	c9	c8	c7	c6	c5	c4	c3	c2	b9	b8	b7	b6	b5	b4	b3	b2	a9	a8	a7	a6	a5	a4	a3	a2
P7[9:2]								P6[9:2]								P5[9:2]								P4[1:0]		P3[1:0]		P2[1:0]		P1[1:0]	
g9	g8	g7	g6	g5	g4	g3	g2	f9	f8	f7	f6	f5	f4	f3	f2	e9	e8	e7	e6	e5	e4	e3	e2	d1	d0	c1	c0	b1	b0	a1	a0

- RAW12

The RAW12 data format follows the generic CSI-2 rule. It is described in Table 28-3.

Table 28-3 RAW12 Data Format Reception

MSB																															LSB
P3[11:4]								P2[3:0]				P1[3:0]				P2[11:4]								P1[11:4]							
c11	c10	c9	c8	c7	c6	c5	c4	b3	b2	b1	b0	a3	a2	a1	a0	b11	b10	b9	b8	b7	b6	b5	b4	a11	a10	a9	a8	a7	a6	a5	a4
P6[11:4]								P5[11:4]								P4[3:0]				P3[3:0]				P4[11:4]							
f11	f10	f9	f8	f7	f6	f5	f4	e11	e10	e9	e8	e7	e6	e5	e4	d3	d2	d1	d0	c3	c2	c1	c0	d11	d10	d9	d8	d7	d6	d5	d4

- RGB888

The RGB888 data format follows the generic CSI-2 rule. It is described in Table 28-4.

Table 28-4 RGB888 Data Format Reception

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MSB																																LSB
B2[7:0]								R1[7:0]								G1[7:0]								B1[7:0]							
d7	d6	d5	d4	d3	d2	d1	d0	c7	c6	c5	c4	c3	c2	c1	c0	b7	b6	b5	b4	b3	b2	b1	b0	a7	a6	a5	a4	a3	a2	a1	a0
G3[7:0]								B3[7:0]								R2[7:0]								G2[7:0]							
f11	f10	f9	f8	f7	f6	f5	f4	g7	g6	g5	g4	g3	g2	g1	g0	f7	f6	f5	f4	f3	f2	f1	f0	e7	e6	e5	e4	e3	e2	e1	e0

- RGB565

The RGB565 data format follows the generic CSI-2 rule. It is described in Table 28-5.

Table 28-5 RGB565 Data Format Reception

MSB																																LSB
R2[4:0]					G2[5:0]						B2[4:0]						R1[4:0]					G1[5:0]						B1[4:0]			
f4	f3	f2	f1	f0	e5	e4	e3	e2	e1	e0	d4	d3	d2	d1	d0	c4	c3	c2	c1	c0	b5	b4	b3	b2	b1	b0	a4	a3	a2	a1	a0

- RGB555

The RGB555 data format follows the generic CSI-2 rule. It is described in Table 28-6.

Table 28-6 RGB555 Data Format Reception

MSB																																LSB
R2[4:0]						G2[4:0]					B2[4:0]						R1[4:0]						G1[4:0]					B1[4:0]			
f4	f3	f2	f1	f0	0	e4	e3	e2	e1	e0	d4	d3	d2	d1	d0	c4	c3	c2	c1	c0	0	b4	b3	b2	b1	b0	a4	a3	a2	a1	a0

- YUV422 8-bit

The YUV422 8bit data format follows the generic CSI-2 rule. It is described in Table 28-7.

Table 28-7 YUV422 Data Format Reception

MSB																																LSB
U1								Y1								V1								Y2							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0	c7	c6	c5	c4	c3	c2	c1	c0	d7	d6	d5	d4	d3	d2	d1	d0

28.6 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R- Read only

   W- Write only

   RW- Read and Write

   RCW- Read and Write, but Clear to 0 by Read

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RSW- Read and Write, but Set to 1 by Read
RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
RC- Read only, and Clear to 0 by read
RS- Read only, and Set to 1 by read

3. Reset Value
1 - reset to 1
0 - reset to 0
? - value unknown after reset

28.6.1 Register Memory Map

Table 28-8 Registers Memory Map Base Address

Name	Base	Description
MIPI_CSI	0x10040000	Base Address of MIPI_CSI
MIPI_PHY	0x10022000	Base Address of MIPI_PHY

The MIPI_CSI is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 28-9 MIPI_CSI Registers Map

Name	RW	Reset Value	Address Offset	Access Size
VERSION	R	0x3130_322A	0x0000	32
N_LANES	RW	0x0000_0001	0x0004	32
PHY_SHUTDOWNZ	RW	0x0000_0000	0x0008	32
DPHY_RSTZ	RW	0x0000_0000	0x000C	32
CSI2_RESETN	RW	0x0000_0000	0x0010	32
PHY_STATE	R	0x0000_0000	0x0014	32
DATA_IDS_1	RW	0x0000_0000	0x0018	32
DATA_IDS_2	RW	0x0000_0000	0x001C	32
ERR1	R	0x0000_0000	0x0020	32
ERR2	R	0x0000_0000	0x0024	32
MASK1	RW	0x0000_0000	0x0028	32
MASK2	RW	0x0000_0000	0x002C	32
PHY_TST_CRTL0	RW	0x0000_0000	0x0030	32
PHY_TST_CRTL1	RW	0x0000_0000	0x0034	32

Table 28-10 MIPI_PHY Registers Map

Name	RW	Reset Value	Address Offset	Access Size
PHY_ENABLE	RW	0x0000_0001	0x0000	8

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PHY_LVDS_TTL_BANKENB	RW	0x0000_001F	0x0080	8
PHY_CK_LANE_SETTLE_TIME	RW	0x0000_008B	0x0100	8
PHY_CK_LANE_CON	RW	0x0000_001F	0x0128	8
PHY_DT0_LANE_SETTLE_TIME	RW	0x0000_008B	0x0180	8
PHY_DT1_LANE_SETTLE_TIME	RW	0x0000_008B	0x0200	8
PHY_MODEL_SWITCH	RW	0x0000_0002	0x02CC	8
PHY_LVDS_MODE	RW	0x0000_001F	0x0300	8

28.6.2 MIPI_CSI_HOST Register and Fields Description

28.6.2.1 VERSION Register(VERSION, 0x0000)

The VERSION register is the Controller Version Identification

	VERSION																															MIPI_CSI + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VERSION																															
RST	0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	1	0	1	0

Bits	Name	Description	RW
31:0	VERSION	Version of the CSI-2 Host Controller	R

28.6.2.2 N_LANES Register(N_LANES, 0x0004)

The N_LANES register is used to set the number of active data lanes.

	N_LANES																															MIPI_CSI + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														N_LANES	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect. Read as zero.	R
1:0	N_LANES	Number of active data lanes	RW

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28.6.2.3 PHY_SHUTDOWNZ Register(PHY_SHUTDOWNZ, 0x0008)

The PHY_SHUTDOWNZ register is used to control PHY shutdown

	PHY_SHUTDOWNZ																															MIPI_CSI + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															PHY_SHUTDOWNZ
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	PHY_SHUTDOWNZ	Shutdown input. This line is used to place the complete macro in power down. All analog blocks are in power down mode and digital logic is cleared. Active Low.	RW

28.6.2.4 DPHY_RSTZ Register(DPHY_RSTZ, 0x000C)

The IN_FM_GS register is used to control DPHY reset.

	DPHY_RSTZ																															MIPI_CSI + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															DPHY_RSTZ
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	DPHY_RSTZ	DPHY reset output. Active Low	RW

28.6.2.5 CSI2_RESETN Register(CSI2_RESETN, 0x0010)

The IN_FM_GS register is used to control the reset of CSI-2 controller.

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	CSI2_RESETN																																MIPI_CSI + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CSI2_RESETN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CSI2_RESETN	CSI-2 controller reset output. Active Low	RW

28.6.2.6 PHY_STATE Register(PHY_STATE, 0x0014)

The PHY_STATE register is the general settings for all blocks.

	PHY_STATE																																MIPI_CSI + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				bypass_2eccc_tst	phy_stopstateclk	phy_rxulpssclknot	phy_rxclkaactivehs	phy_stopstateddata_3	phy_stopstateddata_2	phy_stopstateddata_1	phy_stopstateddata_0	phy_rxulpsessc_3	phy_rxulpsessc_2	phy_rxulpsessc_1	phy_rxulpsessc_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect. Read as zero.	R
11	bypass_2ecc_tst	Payload Bypass test mode for double ECC errors	RW
10	phy_stopstateclk	Clock Lane in Stop state	R
9	phy_rxulpsclknot	Active Low. This signal indicates that the Clock Lane module has entered the Ultra Low Power state	R
8	phy_rxclkactivehs	Indicates that the clock lane is actively receiving a DDR clock	R
7	phy_stopstatedata_3	Data Lane 3 in Stop state	R
6	phy_stopstatedata_2	Data Lane 2 in Stop state	R
5	phy_stopstatedata_1	Data Lane 1 in Stop state	R
4	phy_stopstatedata_0	Data Lane 0 in Stop state	R
3	phy_rxulpsesc_3	Lane module 3 has entered the Ultra Low Power mode	R
2	phy_rxulpsesc_2	Lane module 2 has entered the Ultra Low Power mode	R
1	phy_rxulpsesc_1	Lane module 1 has entered the Ultra Low Power mode	R
0	phy_rxulpsesc_0	Lane module 0 has entered the Ultra Low Power mode	R

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28.6.2.7 DATA_IDS_1 Register(DATA_IDS_1, 0x0018)

The IN_FM_GS register is used to indicate the list of Data Ids for which IDI reports line boundary matching errors.

	DATA_IDS_1																															MIPI_CSI + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	di3_vc		di3_dt						di2_vc		di2_dt						di1_vc		di1_dt						di0_vc		di0_dt					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	di3_vc	Data ID 3 Virtual channel	RW
29:24	di3_dt	Data ID 3 Data Type	RW
23:22	di2_vc	Data ID 2 Virtual channel	RW
21:16	di2_dt	Data ID 2 Data Type	RW
15:14	di1_vc	Data ID 1 Virtual channel	RW
13:8	di1_dt	Data ID 1 Data Type	RW
7:6	di0_vc	Data ID 0 Virtual channel	RW
5:0	di0_dt	Data ID 0 Data Type	RW

28.6.2.8 DATA_IDS_2 Register(DATA_IDS_2, 0x001C)

The DATA_IDS_2 register is used to indicate the list of Data Ids for which IDI reports line boundary matching errors.

	DATA_IDS_1																															MIPI_CSI + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	di7_vc		di7_dt						di6_vc		di6_dt						di5_vc		di5_dt						di4_vc		di4_dt					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	di7_vc	Data ID 7 Virtual channel	RW
29:24	di7_dt	Data ID 7 Data Type	RW
23:22	di6_vc	Data ID 6 Virtual channel	RW
21:16	di6_dt	Data ID 6 Data Type	RW
15:14	di5_vc	Data ID 5 Virtual channel	RW

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13:8	di5_dt	Data ID 5 Data Type	RW
7:6	di4_vc	Data ID 4 Virtual channel	RW
5:0	di4_dt	Data ID 4 Data Type	RW

28.6.2.9 ERR1 Register(ERR1, 0x0020)

The ERR1 register is used to indicate the error status.

	ERR1																															MIPI_CSI + 0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			err_ecc_double	vc3_err_crc	vc2_err_crc	vc1_err_crc	vc0_err_crc	err_l_seq_di3	err_l_seq_di2	err_l_seq_di1	err_l_seq_di0	err_l_bndry_match_di3	err_l_bndry_match_di2	err_l_bndry_match_di1	err_l_bndry_match_di0	err_frame_data_vc3	err_frame_data_vc2	err_frame_data_vc1	err_frame_data_vc0	err_f_seq_vc3	err_f_seq_vc2	err_f_seq_vc1	err_f_seq_vc0	err_f_bndry_match_vc3	err_f_bndry_match_vc2	err_f_bndry_match_vc1	err_f_bndry_match_vc0	phy_errsotsynchs_3	phy_errsotsynchs_2	phy_errsotsynchs_1	phy_errsotsynchs_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect. Read as zero.	R
28	err_ecc_double	Header ECC contains 2 errors. Unrecoverable	R
27	vc3_err_crc	Checksum Error detected on Virtual Channel 3	R
26	vc2_err_crc	Checksum Error detected on Virtual Channel 2	R
25	vc1_err_crc	Checksum Error detected on Virtual Channel 1	R
24	vc0_err_crc	Checksum Error detected on Virtual Channel 0	R
23	err_l_seq_di3	Error in the sequence of lines for vc0 and dt3	R
22	err_l_seq_di2	Error in the sequence of lines for vc0 and dt2	R
21	err_l_seq_di1	Error in the sequence of lines for vc0 and dt1	R
20	err_l_seq_di0	Error in the sequence of lines for vc0 and dt0	R
19	err_l_bndry_match_di3	Error matching Line Start with Line End for vc3 and dt	R
18	err_l_bndry_match_di2	Error matching Line Start with Line End for vc2 and dt	R
17	err_l_bndry_match_di1	Error matching Line Start with Line End for vc1 and dt	R
16	err_l_bndry_match_di0	Error matching Line Start with Line End for vc0 and dt	R
15	err_frame_data_vc3	Last received frame, in Virtual Channel 3, had at least one CRC error	R
14	err_frame_data_vc2	Last received frame, in Virtual Channel 2, had at least one CRC error	R
13	err_frame_data_vc1	Last received frame, in Virtual Channel 1, had at least one CRC error	R
12	err_frame_data_vc0	Last received frame, in Virtual Channel 0, had at least one CRC error	R
11	err_f_seq_vc3	Incorrect Frame Sequence detected in Virtual Channel 3	R

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10	err_f_seq_vc2	Incorrect Frame Sequence detected in Virtual Channel 2	R
9	err_f_seq_vc1	Incorrect Frame Sequence detected in Virtual Channel 1	R
8	err_f_seq_vc0	Incorrect Frame Sequence detected in Virtual Channel 0	R
7	err_f_bndry_match_vc3	Error matching Frame Start with Frame End for Virtual Channel 3	R
6	err_f_bndry_match_vc2	Error matching Frame Start with Frame End for Virtual Channel 2	R
5	err_f_bndry_match_vc1	Error matching Frame Start with Frame End for Virtual Channel 1	R
4	err_f_bndry_match_vc0	Error matching Frame Start with Frame End for Virtual Channel 0	R
3	phy_errsotsynchs_3	Start of Transmission Error on data lane 3 (no synchronization achieved)	R
2	phy_errsotsynchs_2	Start of Transmission Error on data lane 2 (no synchronization achieved)	R
1	phy_errsotsynchs_1	Start of Transmission Error on data lane 1 (no synchronization achieved)	R
0	phy_errsotsynchs_0	Start of Transmission Error on data lane 0 (no synchronization achieved)	R

28.6.2.10 ERR2 Register(ERR2, 0x0024)

The ERR2 register is used to indicate the error status.

	ERR2																															MIPI_CSI + 0x024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								err_l_seq_di7	err_l_seq_di6	err_l_seq_di5	err_l_seq_di4	err_l_bndry_match_di7	err_l_bndry_match_di6	err_l_bndry_match_di5	err_l_bndry_mastch_di4	err_id_vc3	err_id_vc2	err_id_vc1	err_id_vc0	Vc3_err_ecc_corrected	Vc2_err_ecc_corrected	Vc1_err_ecc_corrected	vc0_err_ecc_corrected	phy_errsoths_3	phy_errsoths_2	phy_errsoths_1	phy_errsoths_0	phy_ erresc 3	phy_ erresc_2	phy_ erresc_1	phy_erresc_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect. Read as zero.	R
23	err_l_seq_di7	Error in the sequence of lines for vc0 and dt7	R
22	err_l_seq_di6	Error in the sequence of lines for vc0 and dt6	R
21	err_l_seq_di5	Error in the sequence of lines for vc0 and dt5	R
20	err_l_seq_di4	Error in the sequence of lines for vc0 and dt4	R
19	err_l_bndry_match_di7	Error matching Line Start with Line End for vc7 and dt7	R
18	err_l_bndry_match_di6	Error matching Line Start with Line End for vc6 and dt6	R

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17	err_l_bndry_match_di5	Error matching Line Start with Line End for vc5 and dt5	R
16	err_l_bndry_match_di4	Error matching Line Start with Line End for vc4 and dt4	R
15	err_id_vc3	Unrecognized or unimplemented data type detected in Virtual Channel 3	R
14	err_id_vc2	Unrecognized or unimplemented data type detected in Virtual Channel 2	R
13	err_id_vc1	Unrecognized or unimplemented data type detected in Virtual Channel 1	R
12	err_id_vc0	Unrecognized or unimplemented data type detected in Virtual Channel 0	R
11	vc3_err_ecc_corrected	Header error detected and corrected on Virtual Channel 3	R
10	vc2_err_ecc_corrected	Header error detected and corrected on Virtual Channel 2	R
9	vc1_err_ecc_corrected	Header error detected and corrected on Virtual Channel 1	R
8	vc0_err_ecc_corrected	Header error detected and corrected on Virtual Channel 0	R
7	phy_errsoths_3	Start of Transmission Error on data lane 3(synchronization can still be achieved)	R
6	phy_errsoths_2	Start of Transmission Error on data lane 2(synchronization can still be achieved)	R
5	phy_errsoths_1	Start of Transmission Error on data lane 1(synchronization can still be achieved)	R
4	phy_errsoths_0	Start of Transmission Error on data lane 0(synchronization can still be achieved)	R
3	phy_ erresc _3	Escape Entry Error (ULPM) on data lane 3	R
2	phy_ erresc _2	Escape Entry Error (ULPM) on data lane 2	R
1	phy_ erresc _1	Escape Entry Error (ULPM) on data lane 1	R
0	phy_erresc_0	Escape Entry Error (ULPM) on data lane 0	R

28.6.2.11 MASK1 Register(MASK1, 0x0028)

The ERR1 register is used to set masks for every error status bit.

	MASK1																															MIPI_CSI + 0x028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			mask_err_ecc_double	mask_vc3_err_crc	mask_vc2_err_crc	mask_vc1_err_crc	mask_vc0_err_crc	mask_err_l_seq_di3	mask_err_l_seq_di2	mask_err_l_seq_di1	mask_err_l_seq_di0	mask_err_l_bndry_match_di3	mask_err_l_bndry_match_di2	mask_err_l_bndry_match_di1	mask_err_l_bndry_match_di0	mask_err_frame_data_vc3	mask_err_frame_data_vc2	mask_err_frame_data_vc1	mask_err_frame_data_vc0	mask_err_f_seq_vc3	mask_err_f_seq_vc2	mask_err_f_seq_vc1	mask_err_f_seq_vc0	mask_err_f_bndry_match_vc3	mask_err_f_bndry_match_vc2	mask_err_f_bndry_match_vc1	mask_err_f_bndry_match_vc0	mask_phy_errsotsynchs_3	mask_phy_errsotsynchs_2	mask_phy_errsotsynchs_1	mask_phy_errsotsynchs_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:29	Reserved	Writing has no effect. Read as zero.	R
28	mask_err_ecc_double	Mask for err_ecc_double	RW
27	mask_vc3_err_crc	Mask for vc3_err_crc	RW
26	mask_vc2_err_crc	Mask for vc2_err_crc	RW
25	mask_vc1_err_crc	Mask for vc1_err_crc	RW
24	mask_vc0_err_crc	Mask for vc0_err_crc	RW
23	mask_err_l_seq_di3	Mask for err_l_seq_di3	RW
22	mask_err_l_seq_di2	Mask for err_l_seq_di2	RW
21	mask_err_l_seq_di1	Mask for err_l_seq_di1	RW
20	mask_err_l_seq_di0	Mask for err_l_seq_di0	RW
19	mask_err_l_bndry_match_di3	Mask for err_l_bndry_match_di3	RW
18	mask_err_l_bndry_match_di2	Mask for err_l_bndry_match_di2	RW
17	mask_err_l_bndry_match_di1	Mask for err_l_bndry_match_di1	RW
16	mask_err_l_bndry_match_di0	Mask for err_l_bndry_match_di0	RW
15	mask_err_frame_data_vc3	Mask for err_frame_data_vc3	RW
14	mask_err_frame_data_vc2	Mask for err_frame_data_vc2	RW
13	mask_err_frame_data_vc1	Mask for err_frame_data_vc1	RW
12	mask_err_frame_data_vc0	Mask for err_frame_data_vc0	RW
11	mask_err_f_seq_vc3	Mask for err_f_seq_vc3	RW
10	mask_err_f_seq_vc2	Mask for err_f_seq_vc2	RW
9	mask_err_f_seq_vc1	Mask for err_f_seq_vc1	RW
8	mask_err_f_seq_vc0	Mask for err_f_seq_vc0	RW
7	mask_err_f_bndry_match_vc3	Mask for err_f_bndry_match_vc3	RW
6	mask_err_f_bndry_match_vc2	Mask for err_f_bndry_match_vc2	RW
5	mask_err_f_bndry_match_vc1	Mask for err_f_bndry_match_vc1	RW
4	mask_err_f_bndry_match_vc0	Mask for err_f_bndry_match_vc0	RW
3	mask_phy_errsotsynchs_3	Mask for phy_errsotsynchs_3	RW
2	mask_phy_errsotsync	Mask for phy_errsotsynchs_2	RW

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	hs_2		
1	mask_phy_errsotsyncs hs_1	Mask for phy_errsotsynchs_1	RW
0	mask_phy_errsotsyncs hs_0	Mask for phy_errsotsynchs_0	RW

28.6.2.12 MASK2 register(MASK2, 0x002C)

The ERR2 register is used to indicate the error status.

	MASK2																															MIPI_CSI + 0x02C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								mask_err_l_seq_di7	mask_err_l_seq_di6	mask_err_l_seq_di5	mask_err_l_seq_di4	mask_err_l_bndry_match_di7	mask_err_l_bndry_match_di6	mask_err_l_bndry_match_di5	mask_err_l_bndry_mastch_di4	mask_err_id_vc3	mask_err_id_vc2	mask_err_id_vc1	mask_err_id_vc0	mask_vc3_err_ecc_corrected	mask_vc2_err_ecc_corrected	mask_vc1_err_ecc_corrected	mask_vc0_err_ecc_corrected	mask_phy_errsoths_3	mask_phy_errsoths_2	mask_phy_errsoths_1	mask_phy_errsoths_0	mask_phy_ erresc 3	mask_phy_ erresc _2	mask_phy_ erresc _1	mask_phy_erresc_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect. Read as zero.	R
23	mask_err_l_seq_di7	Mask for err_l_seq_di7	RW
22	mask_err_l_seq_di6	Mask for err_l_seq_di6	RW
21	mask_err_l_seq_di5	Mask for err_l_seq_di5	RW
20	mask_err_l_seq_di4	Mask for err_l_seq_di4	RW
19	mask_err_l_bndry_match_di7	Mask for err_l_bndry_match_di7	RW
18	mask_err_l_bndry_match_di6	Mask for err_l_bndry_match_di6	RW
17	mask_err_l_bndry_match_di5	Mask for err_l_bndry_match_di5	RW
16	mask_err_l_bndry_match_di4	Mask for err_l_bndry_match_di4	RW
15	mask_err_id_vc3	Mask for err_id_vc3	RW
14	mask_err_id_vc2	Mask for err_id_vc2	RW
13	mask_err_id_vc1	Mask for err_id_vc1	RW
12	mask_err_id_vc0	Mask for err_id_vc0	RW
11	mask_vc3_err_ecc_corrected	Mask for vc3_err_ecc_corrected	RW
10	mask_vc2_err_ecc_corrected	Mask for vc2_err_ecc_corrected	RW
9	mask_vc1_err_ecc_corrected	Mask for vc1_err_ecc_corrected	RW
8	mask_vc0_err_ecc_corrected	Mask for vc0_err_ecc_corrected	RW
7	mask_phy_errsoths_3	Mask for phy_errsoths_3	RW

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6	mask_phy_errsoths_2	Mask for phy_errsoths_2	RW
5	mask_phy_errsoths_1	Mask for phy_errsoths_1	RW
4	mask_phy_errsoths_0	Mask for phy_errsoths_0	RW
3	mask_phy_ erresc _3	Mask for phy_erresc_3	RW
2	mask_phy_ erresc _2	Mask for phy_erresc_2	RW
1	mask_phy_ erresc _1	Mask for phy_erresc_1	RW
0	mask_phy_erresc_0	Mask for phy_erresc_0	RW

28.6.2.13 PHY_TST_CRTL0 Register(PHY_TST_CRTL0, 0x0030)

The PHY_TST_CRTL0 register is used to set D-PHY Test interface control 0.

	PHY_TST_CRTL0																															MIPI_CSI + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														phy_testcclk	phy_testclr
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect. Read as zero.	R
1	phy_testclk	PHY test interface strobe signal. Used to clock TESTDIN bus into the DPHY. In conjunction with TESTEN signal controls the operation selection.	RW
0	phy_testclr	PHY test interface clear. Used when active performs vendor specific interface initialization (Active High).	RW

28.6.2.14 PHY_TST_CRTL1 Register(PHY_TST_CRTL1, 0x0034)

The PHY_TST_CRTL0 register is used to set D-PHY Test interface control 1.

	PHY_TST_CRTL1																															MIPI_CSI + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															phy_testen	phy_testdout								phy_testdin							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:17	Reserved	Writing has no effect. Read as zero.	R
16	phy_testen	PHY test interface operation selector: 1: Configures address write operation on the falling edge of TESTCLK 0: Configures a data write operation on the rising edge of TESTCLK	RW
8:15	phy_testdout	PHY output 8-bit data bus for read-back and internal probing functionalities.	R
0:7	phy_testdin	PHY test interface input 8-bit data bus for internal register programming and test functionalities access	RW

28.6.3 MIPI_PHY Register and Fields Description

28.6.3.1 PHY_ENABLE Register(PHY_ENABLE, 0x0000)

	PHY_CRTL0																															MIPI_PHY + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									lane_en_ck	lane_en_3	lane_en_2	lane_en_1	lane_en_0	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6	lane_en_ck	1:enable 0:disable	RW
5	lane_en_3	1:enable 0:disable	RW
4	lane_en_2	1:enable 0:disable	RW
3	lane_en_1	1:enable 0:disable	RW
2	lane_en_0	1:enable 0:disable	RW
1:0	Reserved	Should always be 2'b01	R

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28.6.3.2 PHY_LVDS_TTL BANK ENABLE Register(PHY_LVDS_TTL_BANKENB, 0x0080)

	PHY_STATE																															MIPI_PHY + 0x0080
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										LVDS/TTL Switch	Reserved				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect. Read as zero.	R
5	LVDS/TTL Switch	Switch to LVDS/TTL register bank enable 0:disable 1:enable	RW
4:0	Reserved	Should always be 4'hf.	R

28.6.3.3 PHY_CK_LANE SETTLE TIME Register(PHY_CK_LANE_SETTLE_TIME, 0x0100)

	PHY_CK_LANE_SETTLE_TIME																															MIPI_PHY + 0x0100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												settle_time			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1

Bits	Name	Description	RW
31:4	Reserved	Should always be 28'h8.	R
3:0	settle_time	Configure the count time of the THS-SETTLE by protocol for clock lane. After the count done, D-PHY will begin to receive the high speed data.(can be configured from 4'h0 to 4'hd) 4'b0000:80-110Mhz 4'b0001:110-150Mhz 4'b0010:150-200Mhz 4'b0011:200-250Mhz 4'b0100:250-300Mhz 4'b0101:300-400Mhz 4'b0110:400-500Mhz	RW

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		4'b0111:500-600Mhz 4'b1000:600-700Mhz 4'b1001:700-800Mhz 4'b1010:800-1000Mhz 4'b1011:additional adjust 4'b1100:additional adjust 4'b1101:additional adjust 4'b1110:additional adjust	

28.6.3.4 PHY_CK_LANE CONFIG Register(PHY_CK_LANE_CON, 0x0128)

	PHY_STATE																												MIPI_PHY + 0x0014					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										clk_continuous_cfg	Reserved				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect. Read as zero.	R
5	clk_continuous_cfg	1:enable continuous clock mode 0:disable continuous clock mode	RW
4:0	Reserved	Should always be 4'hf.	R

28.6.3.5 PHY_DT0_LANE_SETTLE_TIME Register(PHY_DT0_LANE_SETTLE_TIME, 0x0180)

	DT0_LANE_SETTLE_TIME																												MIPI_PHY + 0x0180					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												settle_time					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1

Bits	Name	Description	RW
31:4	Reserved	Should always be 28'h8.	R
3:0	settle_time	Configure the count time of the THS-SETTLE by protocol for data0	RW

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		lane. After the count done, D-PHY will begin to receive the high speed data.(can be configured from 4'h0 to 4'hd) 4'b0000:80-110Mhz 4'b0001:110-150Mhz 4'b0010:150-200Mhz 4'b0011:200-250Mhz 4'b0100:250-300Mhz 4'b0101:300-400Mhz 4'b0110:400-500Mhz 4'b0111:500-600Mhz 4'b1000:600-700Mhz 4'b1001:700-800Mhz 4'b1010:800-1000Mhz 4'b1011:additional adjust 4'b1100:additional adjust 4'b1101:additional adjust 4'b1110:additional adjust	

28.6.3.6 PHY_DT1_LANE_SETTLE_TIME Register(PHY_DT1_LANE_SETTLE_TIME, 0x0200)

	DT1_LANE_SETTLE_TIME																MIPI_PHY + 0x0200															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												settle_time			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1

Bits	Name	Description	RW
31:4	Reserved	Should always be 28'h8.	R
3:0	settle_time	Configure the count time of the THS-SETTLE by protocol for data0 lane. After the count done, D-PHY will begin to receive the high speed data.(can be configured from 4'h0 to 4'hd) 4'b0000:80-110Mhz 4'b0001:110-150Mhz 4'b0010:150-200Mhz 4'b0011:200-250Mhz 4'b0100:250-300Mhz 4'b0101:300-400Mhz 4'b0110:400-500Mhz	RW

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		4'b0111:500-600Mhz 4'b1000:600-700Mhz 4'b1001:700-800Mhz 4'b1010:800-1000Mhz 4'b1011:additional adjust 4'b1100:additional adjust 4'b1101:additional adjust 4'b1110:additional adjust	

28.6.3.7 PHY_MODEL_SWITCH Register(PHY_MODEL_SWITCH, 0x02CC)

	PHY_MODEL_SWITCH																															MIPI_PHY + 0x02CC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													LVDS MODEL	MIPI MODE;	TTL MODEL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect. Read as zero.	R
2	LVDS MODEL	LVDS model enable 0:disable 1:enable	RW
1	MIPI MODEL	MIPI model enable 0:disable 1:enable	RW
0	TTL MODEL	TTL model enable 0:disable 1: enable	RW

28.6.3.8 PHY_LVDS_MODE Register(PHY_LVDS_MODE, 0x0300)

	PHY_LVDS_MODE																															MIPI_PHY + 0x0300
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											LVDS 10bit/12bit mode	Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

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Bits	Name	Description	RW
31:6	Reserved	Writing has no effect. Read as zero.	R
5:4	LVDS width setting	LVDS 10bit/12bit mode enable 10:8 bit mode 00:10bit mode 01:12bit mode	RW
3:0	Reserved	Should always be 4'hf.	R

28.7 Operation Flow

The following sections describe the MIPI_CSI operations of configuration.

The Initialization steps are as follows:

1. De-assert CSI-2 presetn signal (global reset)
2. Set number of Lanes(register N_LANES)
3. De-assert PHY shutdown (register PHY_SHUTDOWNZ)
4. De-assert PHY reset (register PHY_RSTZ),and configure PHY as flows 28.8
5. De-assert CSI reset (register CSI2-RESETN)
6. Wait for 200us, read the PHY status register (PHY_STATE) to confirm that all data and clock lanes of the D-PHY are in Stop State
7. Configure the camera sensor to start transmitting a clock on the D-PHY clock lane
8. Read the PHY status register(PHY_STATE) to confirm that the D-PHY is receiving a clock on the D-PHY clock lane
9. Meting the steps above, configure the camera sensor to start transmitting packages

28.8 PHY configure Flow

MIPI INITIATION

1. send 8'h7d to PHY_ENABLE register , enable analog lanes.
2. send 8'h3f to PHY_LVDS_TTL_BANK ENABLE register , switch to lvds/ttl bank
3. send 8'h1e to PHY_LVDS_MODE register , disable lvds internal logic
4. send 8'h1f to PHY_LVDS_TTL_BANK ENABLE register , switch to mipi bank
5. initiation completed

LVDS INITIATION

1. send 8'h7d to PHY_ENABLE register , enable analog lanes.
2. send 8'h3e to PHY_LVDS_TTL BANK ENABLE register , switch to lvds/ttl bank
3. send 8'h04 to PHY_MODEL_SWITCH register , enable LVDS mode
4. send 8'h2f to PHY_LVDS_MODE register, enable 8bit mode
   or send 8'h0f to PHY_LVDS_MODE register, enable 10 bit mode
   or send 8'h1f to PHY_LVDS_MODE register, enable 12 bit mode
5. initiation completed

TTL INITIATION

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1. send 8'h7d to PHY_ENABLE register , enable analog lanes.
2. send 8'h3e to PHY_LVDS_TTL BANK ENABLE register , switch to lvds/ttl bank
3. send 8'h1e to PHY_LVDS_MODE register , disable lvds internal logic
4. send 8'h01 to PHY_MODEL_SWITCH register , enable TTL mode
5. initiation completed

28.9 Index

Table 28-11 Description of Proprietary Vocabulary

Name	Description
PHY	A functional block that implements the features necessary to communicate over the Lane Interconnect.
MIPI	Mobile Industry Processor Interface
CSI-2	Camera Serial Interface 2

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29 Advanced Encryption Standard(AES)

29.1 Overview

- Advanced Encryption Standard
- Fully referring to *Rijdael_fips_197* standard
- AES Engine: AES-128
- 128-bit AES Encryption and Decryption supported
- ECB and CBC mode supported
- CPU and DMA mode supported
- Clear bit supported to clear keys, data and IV for security concern

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30 Data Encryption Standard(DES)

30.1 Overview

The Data Encryption Standard (DES) module encrypts and decrypts a 64-bit data according to the "DATA ENCRYPTION STANDARD (DES)". Two modes are supported: ECB (Electronic Code Book) and CBC (Cipher Block Chaining) modes.

In each mode, the two algorithms are selectable: the simple DES algorithm with a 64-bit key (termed Single DES, or SDES), and the triple DES algorithm with a 192-bit key (termed Triple DES, or TDES). In TDES algorithm, a 64-bit data is encrypted as following: (1) encrypted with the first 64-bit key, (2) decrypted with the second 64-bit key, (3) encrypted with the third 64-bit key.

30.2 Features

- Supports ECB and CBC modes.
- Encrypts and decrypts a 64-bit data within 4 cycles for SDES or 12 cycles for TDES.
- A 16-word input FIFO and a 16-word output FIFO.
- Simply software operation: CPU polling and DMA operations are supported.
- Hardware security: the input data and keys are not readable; keys and other internal registers can be cleaned automatically when module is in stop state.

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31 Digital True Random Number Generator （DTRNG）

31.1 Overview

DTRNG(Digital True Random Number Generator) is used to provide true random number encryption seed for system.

31.2 Features

- Pure digital logic circuits
- True random number
- APB bus configure Register
- Interupt mode and no interupt mode

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Section 7

BOOT

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32 Boot Read Only Memory(BOOTROM)

32.1 Overview

This chapter describes the startup bootrom ways, including SFC MSC0 NOR USB start modes and boot procedure.

The X1830 contains an internal 16KB bootrom. The CPU boots from the bootrom after reset.

32.2 Features

- SPL
- Startup methods including MSC0 NOR SFC USB boot
- An internal 16KB bootrom

32.3 Block Diagram

Figure 32-1 Boot sequence diagram of X1830

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As shown in boot sequence Block Diagram，After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[1:0] to determine the boot method.
2 There 26KB backup reading failed, the 26KB backup at 128th, 256 th , …, and finally 1024th page will be tried in consecutive order.
3 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC0_D0 is used.
4 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.
5 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE, SFC_DR,SFC_DT, SFC_WP,SFC_HOLD are initialized,the boot program loads the 12kB code from SPI NAND/NOR flash to cache and jump to it.
6 If it is boot from NOR Flash, the boot program jump to nor and run directory.

32.4 Functional Description

The boot sequence of the X1830 is controlled by boot_sel[1:0]. The configuration is shown as follow:

Table 32-1 Boot Configuration of X1830

boot_sel[1:0]	Boot method
00	MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B. MSC1 use GPIO Port C)
01	SFC boot @ CS4 (SPI boot)
10	NOR boot @ CS2 (just for FPGA testing)
11	USB boot @ USB 2.0 device, EXTCLK=24MHz

Note:

1. When SFC boot start failure, the program in bootrom will go into MSC0 boot, If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used.
2. When MSC0 boot start failure, the program in bootrom will go into MSC1 boot，If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used.If MSC1 boot start failure, jump to USB boot.

32.4.1 SPL

1.SPL Structure

For some special requirement, SPL(Second Program Loader) data needs to contain different information according to the different boot modes. The basic structure as shown below. SPL signature is used to store some information for kinds of boot (512B), and SPL.text (not more than 24K,and 512

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byte aligned) is real code segment. he first 4k bytes of address space is used for stack and data space. Except NOR boot , all the boot model must jump to 0x80001800 to execute SPL code and all the boot model contains the this SPL structure show as Figure 32-2. Every boot model has its unique SPL signature, Introduces the SPL signature structure behind.

Figure 32-2 The basic SPL structure diagram

32.4.2 MSC0 boot

All cards can boot from SD/MMC Boot from MSC0, the boot program will load 26KB code starting at address 0x4400 from SD/MMC card to cache. First the boot program initializes MSC0_D0, MSC0_CLK, MSC0_CMD as function pins. Only one data pin MSC0_D0 is used. Then the boot program sends CMD55 to test if it's SD or MMC card and initializes the card. At last it loads 26KB code from the card to cache and branches to execute the code in cache.

When initializing the card, the clock of EXTCLK/64 is used(EXTCLK = 24MHZ). And then reading data, the clock of EXTCLK/4 is used.

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32.4.3 NOR boot

When boot_sel[1:0] is selected as NOR boot(boot_sel = 2'b10), the boot grogram is for FPGA testing. The NOR boot is not used for product.

32.4.4 SFC boot

When boot_sel[1:0] is selected as SFC boot(boot_sel = 2'b01), the program in bootrom will goes into SFC boot，at first the program in bootrom fetch 16 bytes flag information table(The first 16 bytes is SPL signature) from the SPI FLASH. the program in bootrom check the flag table to decide the SPI address length, SPI device type(SPI_NOR flash or SPI_NAND flash), receive code length and the crc7 check data.

32.4.5 USB boot

When boot_sel[1:0] is selected as USB boot(boot_sel = 2'b11), the program in bootrom downloads user program from the USB port to internal SRAM and branches to the internal SRAM to execute the program.

X1830 supports the external main crystal whose frequencys are 12MHz,19.2M,24M,26M,48M.

The boot program supports both high-speed (480MHz) and full-speed (12MHz) transfer modes. The boot program uses the following two transfer types.

Table 32-2 Transfer Types Used by the Boot Program

Transfer Type	Description
Control Transfer	Used for transmitting standard requests and vendor requests.
Bulk Transfer	Used for responding to vendor requests and transmitting a user program.

32.5 X1830's bootrom Description

The X1830’s bootrom is 16KB, its mapped address is from 0x1fc0_0000 to 0x1fc0_3FFF.

32.6 Operation Flow

The following sections describe the bootrom operations that include flow of SFC MSC0 NOR USB start modes.

32.6.1 MSC0 boot

The procedure of the X1830 MMC/SD boot is shown as follow:

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Figure 32-3 X1830 MSC0 Boot Procedure

32.6.2 SFC boot

SFC_boot detailed process shown “SFC Boot Procedure”.

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Figure 32-4 X1830 SFC Boot Procedure

Note: Any irregularity in boot steps, SPI_boot will disable SSI controller and jump to MSC0 boot.

SPI-NOR BOOT:

When SPI NOR flash by General-Purpose I/O Port-A 1,2,3,4 pin. In SPI NOR flash address 0x0~0xF, this space will store 16 bytes that agreed SPI boot flag.

The SPI boot flag information table and procedure of the X1830 SPI NOR boot is shown as follow:

Table 32-3 SPI NOR flash boot flag informations(in spl signature)

Addr	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
Detail	0x06	0x05	0x04	0x03	0x02	0x55	0xaa	0x55

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Addr	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
Detail	0xaa	Crc7	0x00	0x00	Len(LSB)	Len	Len	Len(MSB)

Explain:

0x00~0x04 :Must store 0x06,0x05,0x04,0x03,0x02

These part is used for the program in bootrom to decide the spi address length

0X05~0X08 :Must not be 0x55,0xAA,0x55,0xAA.

Magic code，device use this code decided whether is spi-nor flash boot

0x09 :The copy code's crc7 value .

0x0a ~0x0b :0x00

0x0C~0x0F :The length of copy data.

SPI-NAND BOOT:

When SPI NAND flash by General-Purpose I/O Port-A 1,2,3,4 pin. Like spi nor flash, in spi NAND flash address 0x0~0xF, this space will store 16 bytes that agreed SPI_boot flag.

The SPI_boot flag information table and procedure of the X1830 SPI NAND boot is shown as follow:

Table 32-4 SPI NAND flash boot flag informations(in spl signature)

Addr	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
Detail	0x06	0x05	0x04	0x03	0x02	0x55	0xaa	0x55
Addr	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
Detail	0x00	Crc7	ppb	bpp	Len(LSB)	Len	Len	Len(MSB)

Explain:

0x00~0x04 :Must store 0x06,0x05,0x04,0x03,0x02

These part is used for the program in bootrom to decide the spi address length

0X05~0X08 :Must not be 0x55,0xAA,0x55,0x00.

Magic code，device use this code decided whether is spi-nand flash boot

0x09 :The copy code's crc7 value .

0x0a :The pages per block of SPI Nand, the value is X/32, for example, the pages per block is 64, then

ppb is 64/32=2.

0x0b :The bytes per page of SPI Nand, the value is X/1024, for example, the bytes per page is 2048, then bpp is 2048/1024=2.

0x0C~0x0F :The length of copy data..

32.6.3 USB boot

The following figure shows an overview of the USB communication flow.

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Figure 32-5 USB Communication Flow

The vendor ID and product ID for the USB boot device are 0xa108 and 0x4785 respectively. The Configuration for USB is for Control Endpoint 0 with Max Packet Size equals 64 bytes, Bulk IN at Endpoint 1 with Max Packet Size equals 512 bytes in high-speed and 64 bytes in full-speed, Bulk OUT at Endpoint 1 with Max Packet Size equals 512 bytes in high-speed and 64 bytes in full-speed.

The USB boot program provides six vendor requests through control endpoint for user to download/upload data to/from device, and to branch to a target address to execute user program. The six vendor requests are VR_GET_CPU_INFO (0x00), VR_SET_DATA_ADDRESS (0x01), VR_SET_DATA_LENGTH (0x02), VR_FLUSH_CACHES (0x03), VR_PROGRAM_START1 (0x04) and VR_PROGRAM_START2 (0x05). User program is transferred through Bulk IN or Bulk OUT endpoint.

When X1830 is reset with boot_sel[1:0] equals 2'b11b ,the internal boot ROM will switch to USB boot mode and wait for USB requests from host. After connecting the USB device port to host, host will recognize the connection of a USB device, and start device enumeration. After finishing the device

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enumeration, user can send VR_GET_CPU_INFO (0x00) to query the device the program in bootrom information. If user wants to download/upload a program to/from device, two vendor requests VR_SET_DATA_ADDRESS (0x01) and VR_SET_DATA_LENGTH (0x02) should be sent first to tell the device the address and length in byte of the subsequent transferring data. Then data can be transferred through bulk-out/bulk-in endpoint. After this first stage program has been transferred to device, user can send vendor request VR_PROGRAM_START1 (0x04) to let the the program in bootrom to execute the program. This first stage program must not greater than 26KB and is normally used to init GPIO and SDRAM of the target board. At the end of the first stage program, it can return back to the internal boot ROM by jumping to ra ($31) register. Thus user can download a new program to the SDRAM of the target board like the first stage, and send vendor request VR_FLUSH_CACHES (0x03) and VR_PROGRAM_START2 (0x05) to let the the program in bootrom to execute the new program. Next figure is the typical procedure of USB boot.

Figure 32-6 Typical Procedure of USB Boot

Following tables list all the vendor requests that USB boot program supports:

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Table 32-5 Vendor Request 0 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	00H	VR_GET_CPU_INFO: get CPU information.
2	wValue	2	0000H	Not in used.
4	wIndex	2	0000H	Not in used.
6	wLength	2	0008H	8 bytes.

Table 32-6 Vendor Request 1 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	01H	VR_SET_DATA_ADDRESS: set address for next bulk-in/bulk-out transfer.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the data address.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the data address.
6	wLength	2	0000H	Not in used.

Table 32-7 Vendor Request 2 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	02H	VR_SET_DATA_LENGTH: set length in byte for next bulk-in/bulk-out transfer.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the data length.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the data length.
6	wLength	2	0000H	Not in used.

Table 32-8 Vendor Request 3 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	03H	VR_FLUSH_CACHES: flush I-Cache and D-Cache.
2	wValue	2	0000H	Not in used.
4	wIndex	2	0000H	Not in used.

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6	wLength	2	0000H	Not in used.

Table 32-9 Vendor Request 4 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	04H	VR_PROGRAM_START1: transfer data from D-Cache to I-Cache and branch to address in I-Cache. **NOTE:** After downloading program from host to device for the first time, you can only use this request to start the program. Since the USB boot program will download data to D-Cache after reset. This request will transfer data from D-Cache to I-Cache and execute the program in I-Cache.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the program entry point.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the program entry point.
6	wLength	2	0000H	Not in used.

Table 32-10 Vendor Request 5 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	05H	VR_PROGRAM_START2: branch to target address directly.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the program entry point.
4	WIndex	2	xxxxH	LSB (bit[15:0]) of the program entry point.
6	WLength	2	0000H	Not in used.

32.7 Index

Table 32-11 Description of Proprietary Vocabulary

Name	Description
ROM	Read only memory
SPL	Second Program Loader

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